Zewail City of Science and Technology
Computer Architecture
(CIE 439)
(NANENG 433)

Single-Cycle Processor Lab

- **Lab task:**
  - Implement and simulate the HDL of the following modules:
    1. Extender
    2. Register file
    3. Datapath (**integration in top-level module**)
    4. Conditional Check
- **Lab assignment:**
  - Implement and simulate the HDL of the following modules:
    1. Main decoder (inside decoder module)
    2. Data memory
    3. Top module
  - Simulate the single-cycle processor using the provided testbench. If needed, debug till simulation succeeds.