Tarek Eldeeb *December 8, 1983*

tarekeldeeb@gmail.com • +20 100 147 2345 • linkedin.com/in/tarekeldeeb
Eldeeb's Villa • Third Northern District • 6 October City • 12591 • Egypt

Summary

Creative geek with roots in electronics engineering, an entrepreneurial mindset and a passion for building and integrating systems on chips.

My experience is built up in a relatively broad spectrum of engineering know-how; covering computer architecture, embedded software programming and automotive systems.

As an electronics digital design engineer, I design system architectures, code RTL, do static timing analysis, tailor designs to vendor-specific FPGAs and integrate subsystems into an SoC. I'm familiar with several technologies and buses including: PCIe, Ethernet, WiFi, AXI, HDMI, Multi-Gigabit Transceivers (MGT) and many Microblaze-centered systems. Additionally, I code low-level C drivers, build testing environments and benchmarks tools.

Since 2011, I play leadership and management roles; I follow 'Agile Project Management' with a coach mindset. People management skills enabled me to lead multi-site projects successfully.

Experience

Valeo — Principal Engineer, SW Manager

Valeo is a tier-1 multinational automotive supplier, with annual sales exceeding €15B and 75,000 employees. Valeo's largest software R&D center is located in Egypt.

HIL Testbench Development for Automotive SW Validation *July '13 – today*

Design, develop and Implement state-of-the-art test benches for automotive hardware-in-loop (HIL) SW validation.

- Lead and grow a team from 5 to 15 engineers
- Manage multiple projects, resource planning and billability, purchasing, training and enhancing customer satisfaction
- Successfully deliver a HIL test bench to 20+ projects at more than 3 production sites
- Implement HD video streams, high-performance ultrasonic sensors simulation, Ethernet, Flexray and CAN bus communication using FPGA IPs in VHDL/Verilog
- Implement test boards; PCB design and testing activities
- Develop and maintain an RT kernel with firmware and drivers
- Develop and maintain Java-based Test-Automation Environment
- Enable Automotive SW Validation for automatic self-parking cars, Laser Radars, Video surround views and many advanced driver assistance systems

SilMinds — Co-founder and Sr. Digital Design Engineer

A six year entrepreneurial journey with other enthusiastic innovative engineers who started the company from the ground up.

Out-sourced Consultant at Silicon Vision *Nov '12 – Jan '13*

Implement a verilog digital communication bit-chain, and a test system. Silicon Vision provides design services for analog/mixed signal of wireless/optics communication chips.

- Implement the digital communication bit chain; FEC, CRC, SERDES and interleaver blocks. This chain integrates to an analog RF chip
- Develop a Microblaze-based SoC to build a configurable dynamic testing environment for their next generation chip

DFP Stream Co-processor *Oct '10 – Oct '12*

Design and build a completely new stream processor architecture to efficiently utilize SilMinds Decimal Floating-Point (DFP) IP library.

- Manage and lead a team of 5 engieers
- Build an architecture with a configurable number of DFP units

- Ensure a powerful instruction-level parallelism capabilities
- Build a run-time configurable Network-on-chip for dynamic routing
- Support semaphores for thread synchronization with the host PC
- Productize the coprocessor: Integration within a Xilinx PCIe (X8 Gen-2) card, managing DMA streams, low-level PC drivers with adding GCC backend support
- Benchmark the coprocessor; showed 10X speed-up on a 50MHz build over a 3 GHz CPU
- Publish technical papers and apply for patents (USPTO)

Decimal Floating-Point IPs *Nov '07 – Sep '10*

Design and implement of decimal floating-point (DFP) arithmetic cores comforting the IEEE 754-2008 standard. This is the core technology for SilMinds.

- Work closely to our CTO, Hossam Fahmy, and an IEEE floating-point standard committee member with a Stanford Ph.D. Basing our design on IEEE draft versions gave us a market lead at that time
- System level design, VHDL implementation, data path optimization, static timing analysis, FPGA tailoring and writing automation scripts for EDA tools
- Implement Basic ($\pm, \times, /$and $\sqrt{}$) and Elementary functions (Log,Ln,X^Y ...etc.) in VHDL to complete a robust arithmetic library of IP cores for monetary applications
- Technical Presenter in a 10-day business trip: On August '08, SilMinds Sponsored Hot Chips 20 Conference at Stanford University
- Publish several papers and apply for patents, listed below

Consultant at Varkon Semiconductors *Nov '08 – Feb '09*

Build an on-chip testing environment for their DVB-C IP core.

- Build an FPGA microblaze-based SoC with PC controls
- Directly integrate with a mutiport DDR-II memory controller to serve high-throughput requirements

Matlab FPGA Accelerator *May '07 – Sep '07*

Develop a HW accelerator for Matlab. A business failure at the beginning of the start-up experience.

- Override Matlab's underlying math engine, ATLAS BLAS, to accelerate common arithmetic functions.
- Design and build an FPGA-based accelerators for parallel matrix operations

SysDSoft (Acquired by Intel) Testing Lab Engineer

IEEE 802.11 (Wifi) Controller Testing *Aug '06 – April '07*

Test and report Wifi controller using Hardware-in-loop technique. SysDsoft provides design services for PHY and MAC wireless communication layers.

- Contribute to the testing team of a Wifi project for NewLogic (Acquired by Wipro).
- Bug reporting, verification and evaluation of advanced IEEE 802.11 features; Station roaming, link rate adaptation, U-APSD, WMM and low power stations

Education

Faculty of Engineering, Cairo University, Egypt Computer Networks Department

Graduate Classes *2007 – 2011*

I passed several graduate classes including: Advanced Computer Networks, Computer Architecture, Computer Arithmetic, Advanced Math and Technical Writing.

Faculty of Engineering, Cairo University, Egypt Electronics and Communications Department

Bachelor of Science degree *2001 – 2006*

Graduated with grade *Good*. As a student, I co-founded 'Tafra Scientific Magazine', issued by Cairo University, and was its Chief Editor. My graduation project is "MPEG-2 Decoder using HW/SW Co-design". Supervised by Prof. Serag Habib, the project was graded *Excellent*. On the IEEE's annual event, Egyptian Engineering Day, the project was awarded as *EED's Best Project*.

Skills

Digital Electronics

- ●VHDL / Verilog
- ●MGC Questa
- ●Xilinx XPS/EDK and Vivado flows
- ●Multicore Microblaze
- ●AXI4-based SoC Integration
- ◐Interfacing DSP, LVDS and MGT
- ●RAW Video Signalling

Programming

- ●Embedded C
- ●IEEE 754-2008
- ●Matlab
- ◐C++
- ◐C#
- ◐Java / eclipse
- ◐TCL and Bash

Automotive Systems

- ●BroadR-Reach Ethernet
- ●Flexray, CAN and LIN
- ●Vector Tools: Canoe, ..
- ◐ISO 26262
- ◐MISRA-C
- ◐Rational DOORS

Natural Languages

- ●Arabic: Mother tongue
- ●English: Fluently written and well spoken. I had my primary and preparatory education at Misr Language Schools.

Others

- ●Agile Project Mgt
- ●CVS/SVN/GIT
- ●Makefiles
- ◐IEEE 802.11
- ●Computer Networks
- ●Video Compression
- ◐Linux Power User
- ◐LaTeX

Publications

by date: "A decimal fully parallel and pipelined floating point multiplier," *in Forty-Second Asilomar Conference on Signals, Systems, and Computers, Asilomar, California, USA, Oct. 2008.*

"Energy and Delay Improvement via Decimal Floating Point Units," *arith, pp.221-224, 2009 19th IEEE Symposium on Computer Arithmetic, 2009*

"A Decimal Floating-point Fused-Multiply-Add Unit," *Circuits and Systems (MWSCAS), 53rd IEEE International Midwest Symposium on, 2010*

"Algorithm and architecture for on-line decimal powering computation," *Forty-Fourth Asilomar Conference on Signals, Systems, and Computers, 2010*

"Decimal Floating Point for future processors ," *Microelectronics (ICM), International Conference on , 2010*

"Massively Parallelized DNA Motif Search on FPGA," *Book Chapter from "Bioinformatics - Trends and Methodologies", Mahmood A. Mahdavi, ISBN 978-953-307-282-1, InTech, 2011*

Patents

by date: "Decimal Floating-Point Processor", *Dec '12*
"DPD/BCD To BID Converters", *Oct '12*
"Decimal Elementary Functions Computation", *Jul '14*
"Parallel Redundant Decimal Fused-Multiply-Add Circuit", *Aug '14*
"Rounding Unit for Decimal Floating-Point Division", *Jun '14*
"Decimal Floating-Point Square-Root Unit Using Newton-Raphson iterations", *Aug '14*
"Decimal Floating-Point Fused-Multiply-Add Unit", *Apr '14*

Training Courses

by date: "Project Management Program", *Feb '09*, RS Management Consulting House
"Agile Project Management", *Mar '2010*, The International Consortium for Agile [Certeficate]
"Business Writing", *Oct '13*, Top Business Group for HR
"Train the Trainer", *Nov '13*, Brilliance Business School [Certeficate]
"Advanced Time Management", *Feb '14*, Brilliance Business School [Certeficate]
"Flexray, automotive network bus", *Mar '14*, Valeo, internal
"Linux Kernel Driver Programming with Embedded Devices", *Jul '17*, Udemy [Certificate]
"Leadership Program", *Oct '16 – Nov '17*, Redrock International [Certeficate]