Tarek **Eldeeb**

R&D Manager · FPGA Expert

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"Servant leader, lecturer, creative geek with roots in electronics engineering, and an entrepreneurial mindset."

Scan to Update

Education

Executive Masters of Business Administration
Nile University

Graduated with GPA 3.78 (48 credit hours)
2018 - 2020

- The EMBA program is designed in collaboration with IESE Business School, University of Navarra, Spain.

B.Sc. in Electronics and Communications Engineering
Cairo University

Graduated with grade Good
2001 - 2006

- Graduation project was graded Excellent. On the IEEE's annual EED event, the project was awarded as 'Best Project'.
- Passed several post-graduate classes including: Advanced Computer Networks, Computer Architecture, Computer Arithmetic, and Advanced Mathematics.

Skills

Management	Business development, Budgeting, Agile Project Management, Visionary Leadership
Electronics	VHDL/Verilog, AXI-based SoC, Xilinx flows, Microblaze, MGC Questa, PCB
Programming	ANSI C, RTOS, Linux drivers, Java, Matlab, Tensorflow, Bash, TCL, CI/CD, Git
Languages	Arabic, English

Experience

FPGA Expert 📄
Valeo

A business group level secondary title
Apr. 2019 - Current

- Provides consultations and training to several product lines.
- Architect, Lead engineer and product owner of Valeo's internal SW validation Hardware In then Loop 'HIL' Test bench.

Senior SW R&D Manager
Valeo

Comfort & Driving Assistance Business Group
Oct. 2016 - Current

- Put the strategy for Valeo's SW validation test bench, securing funds, and aligning plans execution across different sites.
- Conduct a frequent analysis exercise to assess our rivals, enhance our quality and secure the supply chain.
- Lead and manage a test bench service-line serving 700 engineer worldwide.
- Parallel Agile Projects Management, do resource planning and enhance customer satisfaction.
- Successfully deliver HIL test benches to 50+ projects at 6 R&D sites and 3 production sites.

Senior Team Lead
Valeo

Comfort & Driving Assistance Business Group
July. 2013 - Sep. 2016

- Implement HD video streams, high-performance ultrasonic sensors simulation, Ethernet, Flexray and CAN bus communication using FPGA IPs in VHDL/Verilog
- Design test boards; PCB schematics design and layout
- Develop and maintain an RT kernel with firmware and drivers, in addition to a Java-based Test-Automation Environment
- Enable Automotive SW Validation for automatic self-parking cars, Laser Radars, Video surround views and many advanced driver assistance systems

Cofounder and Digital Design Engineer
SilMinds

A 6-year startup journey
May 2007 - Jun. 2013

- Design and implement decimal floating-point arithmetic IP cores comforting the IEEE754-2008 standard 🔗.
- VHDL implementation, data path optimization, static timing analysis, FPGA tailoring, and writing automation scripts for EDA tools.
- Consultant at two VLSI companies (Si-Vision 🔗 and VarkonSemi 🔗) to develop a configurable dynamic testing environment for their next generation chips using FPGAs.

Testing Lab Engineer *SysDSoft*

WiFi Data Link Layer Controller *Aug 2006 - May 2007*

- Executed test scripts to automate hardware-in-loop validation for our wireless 802.11 a/b/g/q chips.
- SysDSoft was acquired by Intel (2011) ↗, then sold to Apple (2019) ↗.

Publications

2022	**Research Article,** "On-line Hybrid Perceptual and Cryptographic Image Hashing System"	*ISEEIE, Thai*
2018	**Research Article,** "Dynamic Code Loading to a Bare-metal Embedded Target"	*ICSIE, Cairo*
2014	**Patent,** "Decimal Floating-Point Fused-Multiply-Add Unit"	*USPTO, US*
2014	**Patent,** "Decimal Floating-Point Square-Root Unit Using Newton-Raphson iterations"	*USPTO, US*
2014	**Patent,** "Rounding Unit for Decimal Floating-Point Division"	*USPTO, US*
2014	**Patent,** "Parallel Redundant Decimal Fused-Multiply-Add Circuit"	*USPTO, US*
2014	**Patent,** "Decimal Elementary Functions Computation"	*USPTO, US*
2012	**Patent,** "DPD/BCD To BID Converters"	*USPTO, US*
2012	**Patent,** "Decimal Floating-Point Processor"	*USPTO, US*
2011	**Book Chapter,** "Massively Parallelized DNA Motif Search on FPGA"	*IntechOpen, UK*
2010	**Research Article,** "Decimal Floating Point for future processors "	*ICM, Cairo*
2010	**Research Article,** "Algorithm and architecture for on-line decimal powering computation"	*ASILOMAR, CA, US*
2010	**Research Article,** "A Decimal Floating-point Fused-Multiply-Add Unit"	*MWSCAS, WA, US*
2009	**Research Article,** "Energy and Delay Improvement via Decimal Floating Point Units"	*Comp. Arith., OR, US*
2008	**Research Article,** "A decimal fully parallel and pipelined floating point multiplier"	*ASILOMAR, CA, US*

According to Google Scholar Profile ↗, there are 150 citation to my work.

Training

2022	**Change Management,** Logic Training	*Certificate* 🗎
2021	**Embedded Linux,** Linux Hotel	*Certificate* 🗎
2020	**Managing Remotely,** Impact Learning and Development	*Certificate* 🗎
2019	**Certified KPI Professional,** KPI Institute	*Certificate* 🗎
2018	**Deep Learning Specialization,** DeepLearning.ai (coursera)	*Certificate* ↗
2018	**Develop Collaborative Management - Hofstede Model Approach,** Hostede Insights	*Certificate* 🗎
2017	**Leadership Program,** Redrock International	*Certificate* 🗎
2017	**Linux Kernel Driver Programming with Embedded Devices,** Udemy	*Certificate* ↗
2014	**Advanced Time Management,** Brilliance Business School	*Certificate* 🗎
2013	**Train the Trainer,** Brilliance Business School	*Certificate* 🗎
2010	**Agile Project Management,** The International Consortium for Agile	*Certificate* 🗎
2009	**Project Management Program,** RS Management Consulting House	—

All references are embedded in this PDF file, please click 🗎 or ↗ above.