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EE102-02

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LAB 3: COMBINATIONAL LOGIC CIRCUIT

A) PURPOSE

The purpose of this experiment is to understand and implement logical gates and practice functions with them. Creating different input sequences by using 74HC163 is significant in this lab.

B) METHODOLOGY

74 LS/HC 163 (Synchronous 4-Bit Binary Counter):

To use this IC component, 5V must be given to the MR, CEP, CET, PE, and VCC pins, and the desired signal be given to the CP pin. By doing these steps, four different signals can be captured from Q0-Q3 pins. Those signals are generated by positive edge counting of the input clock and feedback counting of the first signal. In this experiment, signals from Q0 and Q3 are used.

74 LS/HC 04 (Hex Inverter):

74HC04 is an integrated circuit consisting of 6 independent not gates, a GND, and a VCC pin. In this experiment, two signals have been inverted for implementing the XOR gate. VCC pin has connected to 5V voltage.

74 LS/HC 08 (Quad 2-Input And Gate):

74HC08 is an integrated circuit consisting of 4 independents and gates, a GND, and a VCC pin. In this experiment, six signals have given to IC as inputs. VCC pin has connected to 5V voltage.

74 LS/HC 32 (Quad 2-Input Or Gate):

74HC32 is an integrated circuit consisting of 4 independents or gates, a GND, and a VCC pin. In this experiment, two signals have been given to 74HC32 as inputs. VCC pin has connected to 5V voltage.

A classical half adder is selected for the experiment and built using one 74HC08, one 74HC32, one 74HC04, and lastly, one 74HC163.

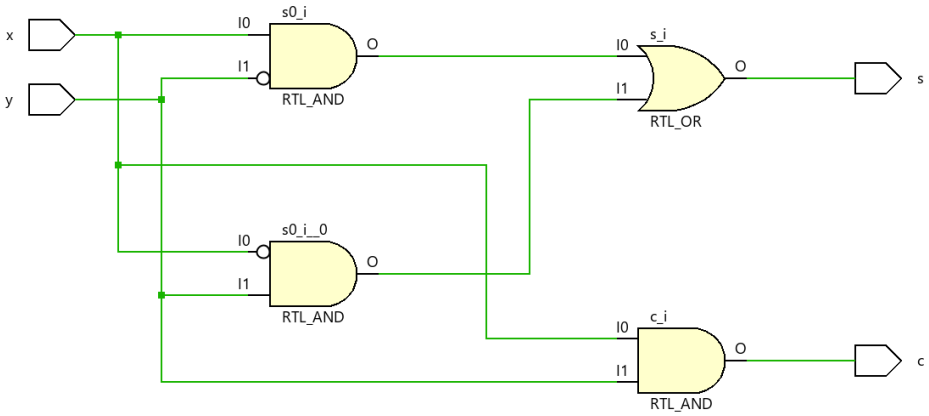
The clock signal has been given to the counter by the signal generator. A square wave with 4 V pp and 5 Hz frequency has been sent to the clock input of the counter. The outputs, Q0 used as x, and Q2 is used as y.

Designing and investigating the outputs of a Half Adder was the goal of this experiment.

Schematic of the half adder and logic design can be seen below

x	y	s	c
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

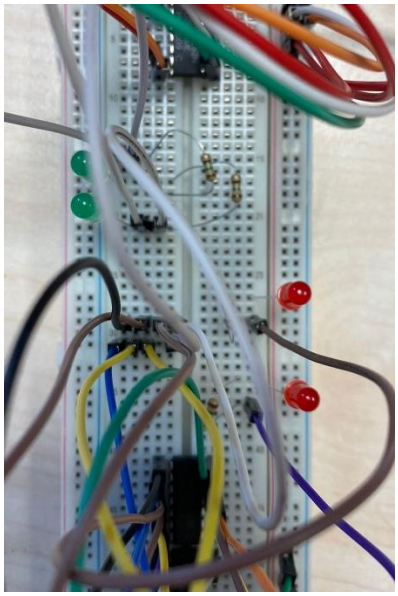
(Table 1: Truth Table of $s = \bar{x}y + x\bar{y}, c = xy$ *also known as half adder*)



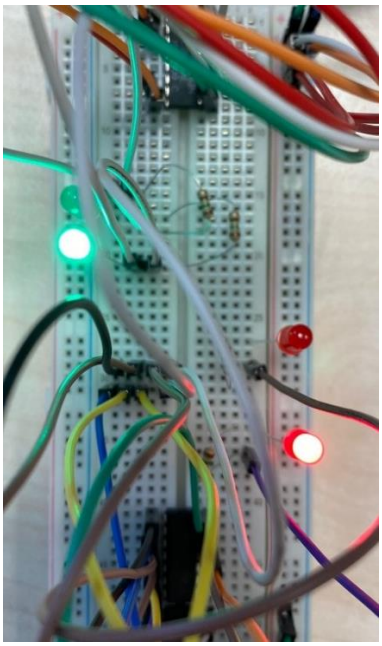
(Image 1: Schematic of the half adder design)

C) RESULTS

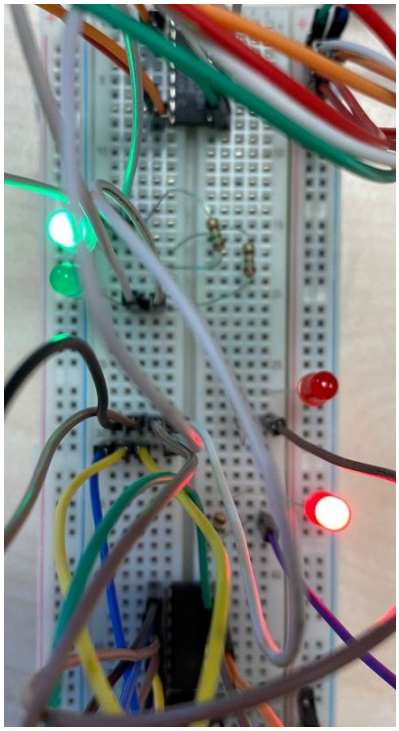
After building, the designed circuit voltage source was turned on, and the following results were observed. Green LEDs stand for x and y input signals, while red ones stand for the output signals s (sum) and c (carry).



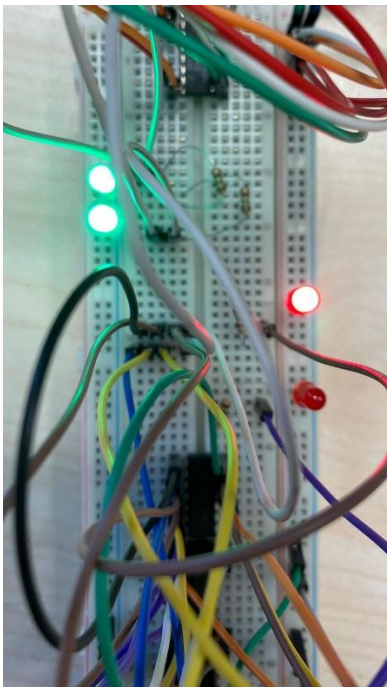
(Image 2: s = 0, c = 0 for x = 0 and y = 0)



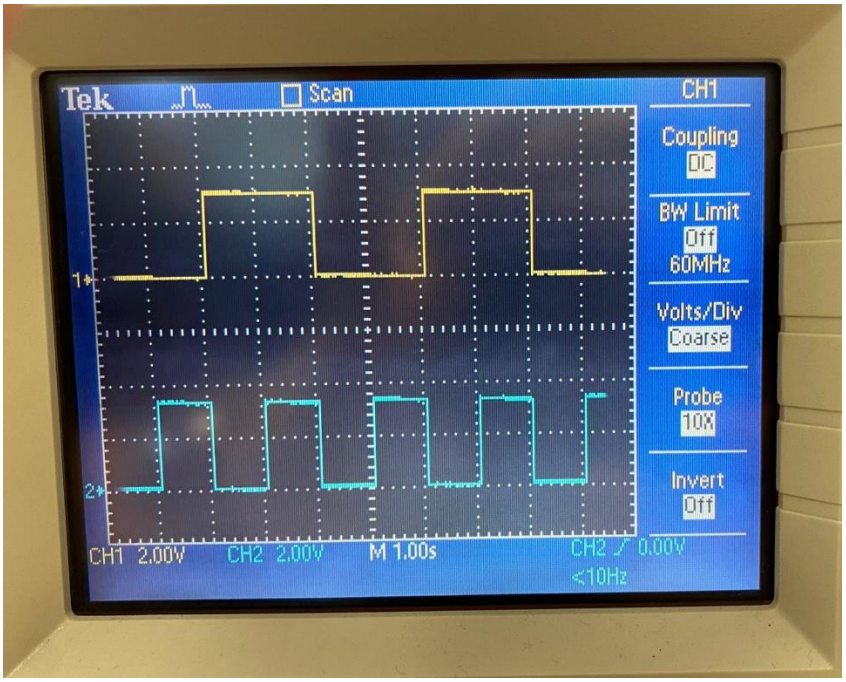
(Image 3: s = 1, c = 0 for x = 0 and y = 1)



(Image 4: s = 1, c = 0 for x = 1 and y = 0)

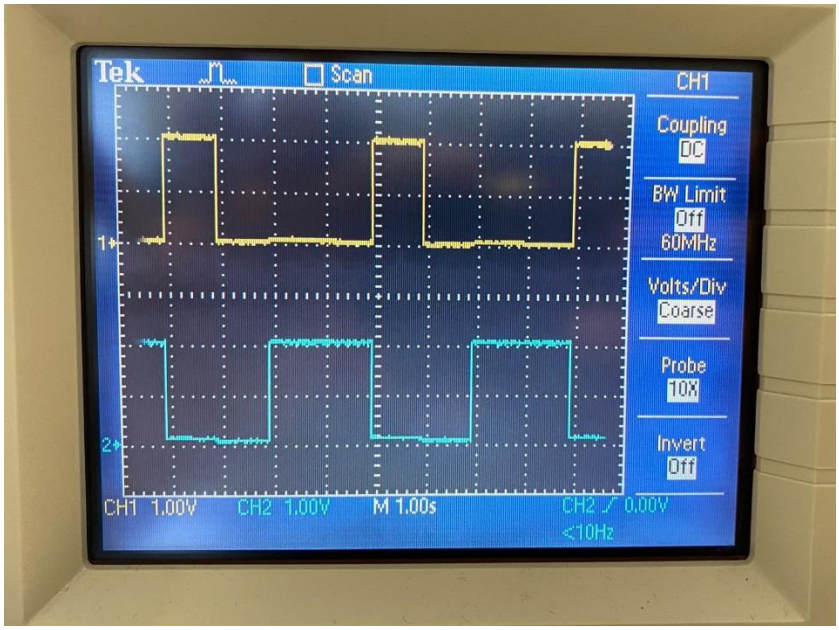


(Image 5: s = 0, c = 1 for x = 1 and y = 1)



(Image 6: Inputs x and y)

It can be seen that values of the inputs x and y take 00, 01, 10, 11 between -1 to 3 seconds.



(Image 7: outputs s and c; 2 seconds phase difference with the input graph)

Between -3 to -1 seconds, the s and c take 00, 10, 10, and 01, corresponding to the period -1 to 3 in Image 6. It also matches with the theoretical results represented in Table 1.

D) CONCLUSION

There were many defective components in this lab experiment; therefore, debugging was necessary all through the process. The counter has changed several times to observe a proper result. It was instructive to experience the solid implementations of the gates that we have learned for half of the semester.