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EE102-02

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LAB 7: FINITE STATE MACHINE

A) PURPOSE

Purpose of this experiment is to implent the usage of flip flops by creating finite machines. A 2 bit counter will be made in this lab. Being able to create state machines that has been used in both vhdl and also in the lectures with solid components will be helpful to improve visualization of sequential circuits that are created with state machine techniques.

B) METHODOLOGY

In this lab a 2 bit counter will be made by using 2 D-flipflops, 1 XOR gate, several leds and resistances to be able to see the states easily. Components will be connected by using a breadboard and copper cables. The outputs Q1 and Q0 will be represented with the leds. Type of the components that will be used will be described below.

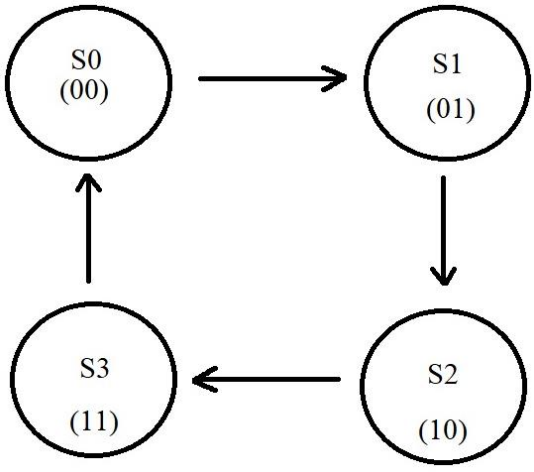
74 LS/HC 86 Quad 2-Input XOR Gate

This component has been used to generate the D1 of the second clock by inputing Q1 and Q0 of the flip flops.

74 LS/HC 74 Dual D Flip−Flop

This component consists of 2 D flip flops and both of them will be used to generate the necessary states. Since there will be 4 states to make a 2 bit counter. 2 D flip flops will be enough to complete this.

Design of the State Machine



(Image 1: State diagram of the 2-bit counter)

Flip Flop Inputs / State Descriptions	Q1	Q0
S0: $00_2 = 0$	0	0
S1: $01_2 = 1$	0	1
S2: $10_2 = 2$	1	0
S3: $11_2 = 3$	1	1

(Table 1: Inputs of the Flip Flops, State assignment table)

Q1	Q0	Q1*	Q0*
0	0	0	1
0	1	1	0
1	0	1	1
1	1	0	0

(Table 2: State Exictation and Next State Table)

Q1/Q0	0	1
0	1	1

1	0	0

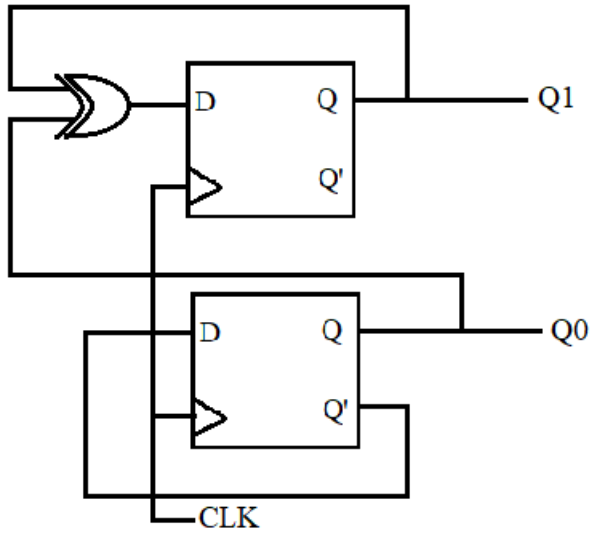
(Table 3: K-Map of Q0* which is the D of the first FF)

Q0* = D0 = Q0’

Q1/Q0	0	1
0	0	1
1	1	0

(Table 4: K-Map of Q0* which is the D of the first FF)

Q1* = D1 = $Q0 \oplus Q1$



(Image 2: Schematic of the 2-bit counter)

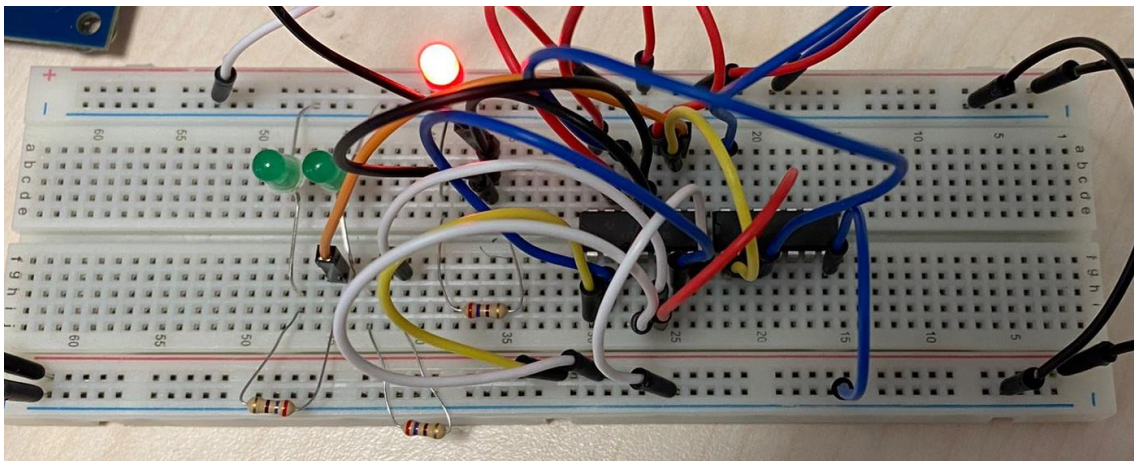
Outputs of the D flip flops will be connected to two green leds which indicate the results of the 2-bit counters.

Also a red led will be connected to the clock to show the rising and falling edges. The clock frequency will be 1 Hz.

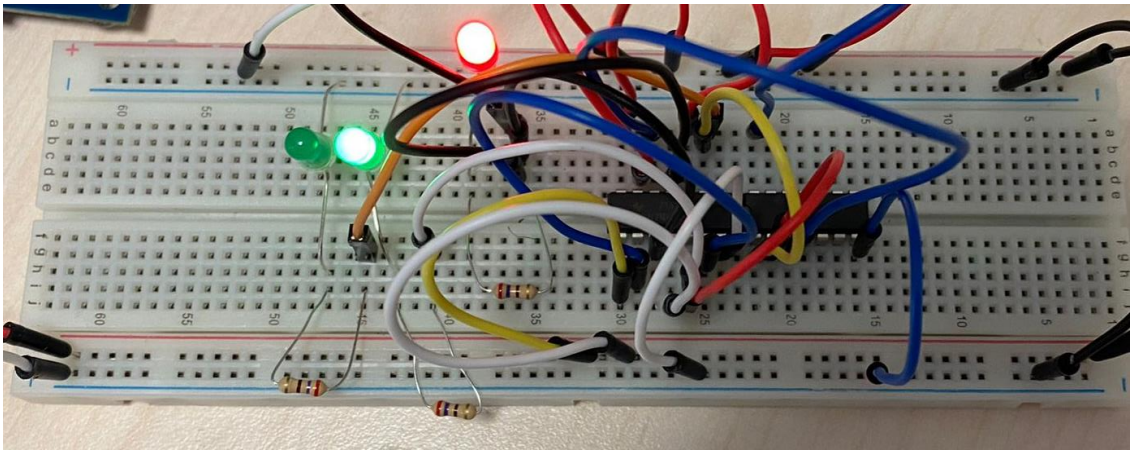
C) RESULTS

The VCC and the GND pins of the components has connected to the 5V and GND connections of the power supply. A square wave with 1Hz frequency has been created with the signal generator and connected to the CLK pin of the flipflops.

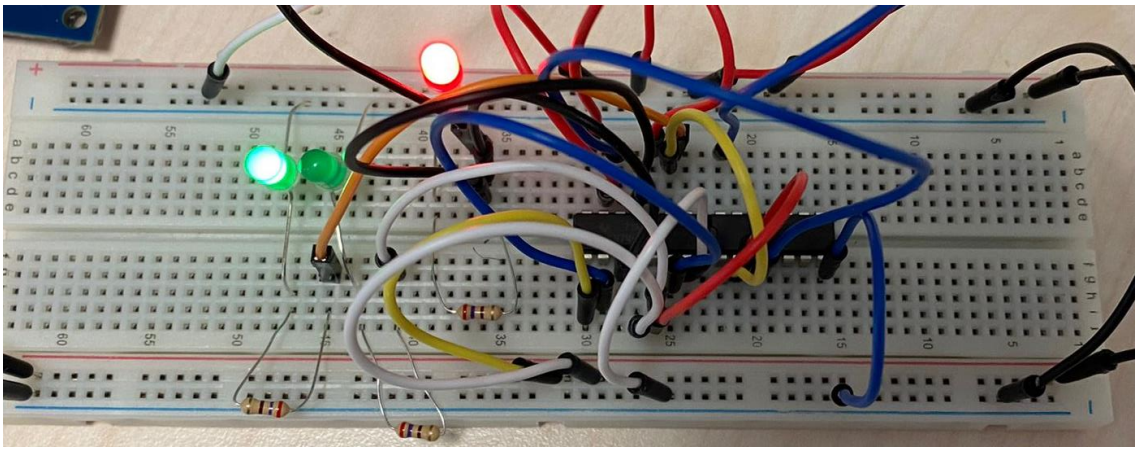
Results can be seen from the images of the experiment below.



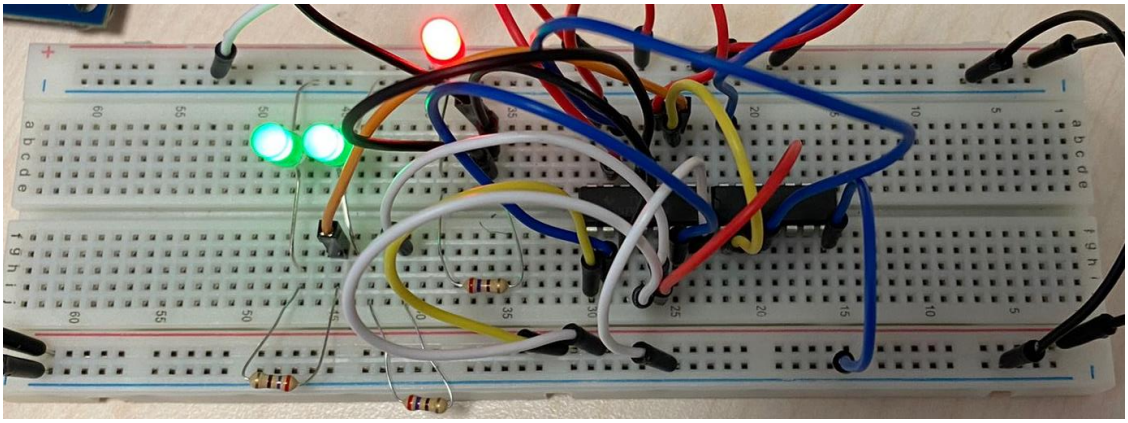
(Image 3: State =S0 , Q1 = 0 , Q0 = 0)



(Image 4: State =S1, Q1 = 0 , Q0 = 1)



(Image 5: State =S2, Q1 = 1 , Q0 = 0)



(Image 6: State =S3, Q1 = 1 , Q0 = 1)

D) CONCLUSION

This lab was helpful for understanding how to build a finite state machine with real components and implementing a 2 bit counter with this state machine.