

Vendor	Tools	Chip	Implementation	Fmax (MHz)	LUT	FF	Distributed RAM	Carry Cells	BSRAM	DSP	DMIPS/MHz	DMIPS	Pnormalised/DMIPS
Xilinx	Vivado v2024.1	Artix-7 XC7A35T-ICPG236C	<i>PicoRV32 (SSRAM RF, LUT_ALU)</i>	193.000	966	424	48	-	-	-	0.112	21.616	8.625
			<i>eduBOS5 (SSRAM RF, LUT_ALU) - 2stage</i>	130.500	810	450	48	-	-	-	0.39	50.895	2.076923077
Lattice	Lattice Diamond	ECP5 LF5U-12F-6BG381C	<i>PicoRV32 (SSRAM RF, LUT_ALU)</i>	94.060	1013	428	96	129	-	-	0.112	10.534	9.045261059
			<i>eduBOS5 (SSRAM RF, LUT_ALU)</i>	71.669	929	458	96	94	-	-	0.39	27.951	2.382043612
Gowin	Gowin FPGA Designer 1.9.9.03	GW2AR-18C C8/I7	<i>PicoRV32 (SSRAM RF, LUT_ALU)</i>	118.316	1340	414	32	-	-	-	0.112	13.251	11.96463965
			<i>eduBOS5 (SSRAM RF, LUT_ALU) - 2stage</i>	88.081	1022	450	32	-	-	-	0.39	34.340	2.621397263
			<i>PicoRV32 (SSRAM RF, DSP_ALU) N/A</i>	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
			<i>eduBOS5 (SSRAM RF, DSP_ALU) - 2stage</i>	113.610	902	385	32	-	-	2	0.39	44.308	2.312815293
			<i>PicoRV32 (BSRAM RF, LUT_ALU)</i>	116.327	1353	458	-	-	2 (32 kbits -	0.112	13.029	12.08000852	
			<i>eduBOS5 pipelined (BSRAM RF, LUT_ALU) WIP, forecasted:</i>	70.000	1000	450	-	-	1 (16 kbits -	0.8	56.000	1.25	
		GW1NR-9C C6/I5	<i>PicoRV32 (SSRAM RF, LUT_ALU)</i>	63.324	1340	414	32	-	-	-	0.112	7.092	11.96477157
			<i>eduBOS5 (SSRAM RF, LUT_ALU) - 2stage</i>	50.819	1022	450	32	-	-	-	0.39	19.819	2.620567032
			<i>PicoRV32 (SSRAM RF, DSP_ALU) N/A</i>	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
			<i>eduBOS5 (SSRAM RF, DSP_ALU) - 2stage</i>	56.052	902	385	32	-	-	2	0.39	21.860	2.312850137
			<i>PicoRV32 (BSRAM RF, LUT_ALU)</i>	55.815	1353	458	-	-	2 (32 kbits -	0.112	6.251	12.08089826	
			<i>eduBOS5 pipelined (BSRAM RF, LUT_ALU) WIP, forecasted:</i>	45.000	1000	450	-	-	1 (16 kbits -	0.8	36.000	1.25	