Yıldız Technical University
Computer Engineering
2023-2024 Spring
BLM2022 Computer Organization
Homework 5

Question)

Implement a direct mapped cache with the following properties:

- cache size is 256 bytes
- block size is 4 bytes
- write through on memory write with cache hit (both the cache and the memory are updated)
- write allocate on memory write with cache miss (the block is first loaded from the memory and put in the cache, and then the data word is written to the cache)

Using the single cycle architecture test your implementation on:

- memory read hit
- memory read miss
- memory write hit
- memory write miss

Upload your answer as [StudentNo].zip file structured with the Verilog code [StudentNo].v, testbench code [StudentNo]_tb.v and a video [StudentNo].mkv follows with a maximum of 5 minutes explaining your design and testbench results.