SECOND EDITION

Electronic Circuit Analysis

K. Lal Kishore

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Second Edition

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Sri *Saraswati*

the goddess of learning

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PREFACE TO SECOND EDITION

Since publishing first edition of this book three years back, there are few additions in the subject and also as a result of receiving some feedback, it has become imperative to bring another edition to cover the lapses and bring the text more useful to students.

In the second edition, I have reorganised the chapters and also added few subchapters like High Frequency Amplifiers, Stability Considerations, UPS and SMPS in the respective chapters.

The author is indebted to Sri. M.V. Ramanaiah, Associate Professor in the Department of ECE, Gokaraju Rangaraju Institute of Engineering and Technology, Hyderabad for his efforts in going through the book and making the symbols etc. more perfect which were cropped up at the time of typing the text.

I am also thankful to Mr. Nikhil Shah and Mr. Manoj Jha of BS Publications for their persuasion and bringing the second edition of this book in record time.

-Author

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PREFACE TO FIRST EDITION

Foundations for Electronics Engineering were laid as far back as 18th Century when H.A. Lorentz postulated the existence of negatively charged particles called as Electrons. Since then the field of electronics engineering has developed rapidly. Advancement in this area was more rapid since 1970s, with Digital Electronics dominating over Analog Electronics, as was done by Solid State Devices in 1960s over Vacuum Tubes. After the Industrial Revolution, it is Computer Revolution which is the astonishing phenomenon, at the fag end of the 21st Century. The next striking development could be computer communications. The research and development work done in the field of Semiconductor Devices and Technology contributed significantly for the miniaturisation taking place in electronic systems and computers. Thus Electronics Engineering is a fascinnating subject.

Electronic Circuit Analysis is an important component of the broad area of Electronics and Communications Engineering. Electronic Circuit Design and Analysis aspects are dealt with in this book. Learning these topics is very essential for any electronics engineer. A student must study the subject, not just for the sake of passing the examination, but to learn the concepts. In this competitive world, to secure a job or to learn the concepts, proper effort must be made. This book is written with that motive. Any book written just for the sake of enabling the student to pass the examination will not fullfil its complete objective. Electronic Circuit Analysis is one of the fundamental subjects, which helps in I.C design, VLSI design etc.

This textbook can also be used for M.Sc (Electronics), AMIETE, AMIE (Electronics) B.Sc (Electronics), Diploma courses in Electronics, Instrumentation Engineering and other courses where Electronics is one subject. So students from Universities, Engineering Colleges and Polytechnics can use this book.

Though efforts are made to minimize typing errors, printing mistakes and other topographical errors, still, there could be some omissions. The author and publisher will be thankful if such errors brought to notice for necessary correction.

Many Textbooks are referred while writing this book. The author is thankful for them and their publishers.

The author is thankful to Mr. Nikhil Shah for the encouragement given to write this book. The author is also thankful to Mr. Naresh, Mr. Prashanth, Mr. J. Das, Shri Raju and other staff of M/S. B.S. Publications. The author is highly grateful to Prof. D. S. Murthy Head, ECE Dept., Gayatri Vidya Parishad College of Engineering, Vizag, for his valuable suggestions. The author is also thankful to Mrs. Mangala Gowari Assoc. Prof. Dept. of ECE, JNTU, Hyderabad Mr. P. Penchalaiah Assoc. Prof. Dept of ECE, Vignan Inst. of Science and Technology, Hyderabad and Mr. P. Ramana Reddy, APECE, JNTU CE, Hyderabad. Author is particularly thankful to Mr. P. Penchalaiah for his effort in minimizing printing mistakes. The author is also thankful to Ms. U.N.S. Sravanthi and Ms. Srujana for the proof reading work.

For a task like writing textbook, there is always scope for improvement and corrections. Suggestions are welcome.

ज्ञानम संम्यक वीश्रणम : Looking in right perspective is wisdom.

बिद्धथाविंदते अमृतम : Education gives prosperity.

Knowledge shows the path – Wisdom lights it up.

-Author

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SYMBOLS

$g_{b'e}$	:	Input Conductance of BJT in C.E configuration between fictitious base terminal B' and emitter terminal E.
h_{ie}	:	Input impedance (resistance) of BJT in C.E configuration
h_{fe}	:	Forward short circuit current gain in C.E configuration
h_{re}	:	Reverse voltage gain in C.E. configuration
h_{oe}	:	Output admittance in C.E. configuration
$r_{bb'}$	:	Base spread resistance between base terminal B and fictitious base terminal B'.
C_e	:	Emitter junction capacitance
C_C	:	Collector junction capacitance
g_m	:	Transconductance or Mutual conductance
V_T	:	Volt equivalent of temperature $\frac{KT}{e} = \frac{T}{11,600}$
η	:	Diode constant $\eta = 1$ for G_e; $\eta = 2$ for S_i
$g_{b'c}$	:	Feedback conductance between B' and collector terminal C
g_{ce}	:	Output conductance between Collector and Emitter terminals.
C_D	:	Diffusion capacitance
Q	:	Charge
D_B	:	Diffusion constant for minority carriers in Base region
n	:	constant (= 1/2 for abrupt junctions)
W	:	Base width
ω	:	Angular frequency = $2\pi f$
f_T	:	Frequency at which C.E. short circuit current gain becomes unity
f_β	:	Frequency at which h_{fe} becomes 0.707 $h_{fe\,max}$. Frequency range upto f_β is referred as the B.W of the transistor circuit.

C_π	:	Incremental capacitance in hybrid - π model
r_π	:	Incremental resistance in hybrid - π model
A_{V_1}	:	Voltage gain of I stage amplifier circuit
A_{I_1}	:	Current gain of I stage amplifier circuit
B.W	:	Band width of the amplifier circuit.
f_C	:	Cut-off frequency
$f_L = f_1$	:	Lower cutoff frequency or Lower 3-db point or Lower half power frequency
$f_H = f_2$	:	Upper cutoff frequency or upper 3-db point or upper half power frequency
f_0	:	Mid Band Frequency $f_O = \sqrt{f_1\ f_2}$.
R_E	:	Emitter Resistor
C_E	:	Emitter Capacitor
A_V(L.F)	:	A_{V_L} = Voltage gain in the Low frequency range
A_V(H.F)	:	A_{V_H} = Voltage gain in the High frequency range
A_V(M.F)	:	A_{V_M} = Voltage gain in the Mid frequency range
P_O	:	Output Power
P_I	:	Input Power
A_P	:	Power Gain
ϕ	:	Phase angle
V_y	:	RMS value of voltage
I_y	:	RMS value of current
I_m	:	$(I_{Max} - I_{Min})$
V_m	:	$(V_{Max} - V_{Min})$
I_{P-P}	:	Peak to Peak value of current
P_{ac}	:	A.C. Output power
P_{DC}	:	DC Input power
η	:	Conversion Efficiency of the power amplifier circuit.
n	:	Transformer turns ratio (N_2/N_1)
N_2	:	Number of turns of transformer Secondary winding
N_1	:	Number of turns of transformer Primary winding
V_1	:	Primary voltage of Transformer
V_2	:	Secondary voltage of Transformer
R_t	:	Resistance of Tuned Circuit
R_P	:	Parallel resistance associated with the tuning coil (Inductor)
V_{be}	:	A.C voltage between base and emitter leads of transistor (BJT)
V_{BE}	:	D.C voltage between base and emitter leads of transistor (BJT)
		Small subscripts are used for a.c. quantities.
		Capital subscripts are used for a d.c. quantities.

Q_e	:	Effective Q factor of coil
δ	:	Fractional Frequency Variation
R_{tt}	:	Resistance of tapped tuned Circuit
Q_O	:	Quality factor of output circuit
M	:	Mutual Inductance
K_C	:	Critical value of the coefficient of coupling
M_C	:	Critical value of Mutual Inductance
R_S	:	Series Resistance in Voltage Regulators
S	:	Stability factor
S_T	:	Temperature coefficient in Voltage Regulator
R_O	:	Output Resistance
R_Z	:	Zener Diode Resistance
V_γ	:	Cut in voltage of junction diode
$V_O'{}_{(P-P)}$	:	Output ripple voltage
$V_i'{}_{(P-P)}$	:	Input ripple voltage

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Brief History of Electronics

In science, we study about the laws of nature and verification and in technology, we study the applications of these laws to human needs.

Electronics is the science and technology of the passage of charged particles, in a gas or vacuum or semiconductor.

Before electronic engineering came into existence, electrical engineering flourished. Electrical engineering mainly deals with motion of electrons in metals only, where as Electronic engineering deals with motion of charged particles (electrons and holes) in metals, semiconductors and also in vacuum. Another difference is, in electrical engineering, the voltages and currents are very high KV, and Amperes, where as in electronic engineering one deals with few volts and mA. Yet another difference is, in electrical engineering; the frequencies of operation are 50 Hzs/60Hzs. In electronics it is KHzs, MHz, GHzs, (high frequency).

The beginning for Electronics was made in 1895 when H.A. Lorentz postulated the existence of discrete charges called *electrons*. Two years later, *J.J.Thomson* proved the same experimentally in 1897.

In the same year that is in 1897, Braun built the first tube based on the motion of electrons, the Cathode ray tube (CRT).

In 1904 Fleming invented the Vacuum diode called '*valve*'.

In 1906 a semiconductor diode was fabricated but they could not succeed, in making it work. So semiconductor technology met with premature death and vacuum tubes flourished.

In 1906 it self, De Forest put a third electrode into Fleming's diode and he called it Triode. A small change in grid voltage produces large change in plate voltage, in this device.

In 1912 Institute of Radio Engineering (IRE) was set up in USA to take care of the technical interests of electronic engineers. Before that in 1884 Institute of Electrical Engineers was formed and in 1963 both have merged into one association called IEEE (Institute of Electrical and Electronic Engineers).

The first radio broadcasting station was built in 1920 in USA.

In 1930 black and white television transmission started in USA.

In 1950 Colour television broadcasting was started.

The electronics Industry can be divided into 4 categories :

Components	:	Transistors, ICs, R, L, C components
Communications	:	Radio, TV, Telephones, wireless, landline communications
Control	:	Industrial electronics, control systems
Computation	:	Computers

Vacuum Tubes ruled the electronic field till the invention of transistors. The difficuty with vacuum tubes is with its excess generated heat. The filaments get heated to > 2000^0 K so that electronic emission takes place. The filaments get burnt and tubes occupy large space. So in 1945 Solid State Physics group was formed to invent semiconductor devices in Bell labs, USA.

1895 : H. A. Lorentz - Postulated existence of Electrons

1897 : J.J. Thomson - Proved the same

1904 : Fleming - Vacuum Diode

1906 : De. Forest - Triode

1920 : Radio Broadcasting in USA

1930 : Black and White TV USA

1947 : Shockley invented the junction transistor. (BJT)

1947 : Schokley BJT Invention

1950 : Colour Television

1959 : Integrated Circuit concept was announced by Kilby at an IRE convention.

1959 : KILBY etc. anounced ICs.

1969 : LSI, IC : Large Scale Integration, with more than 1000 but < 10,000 components per chip (integrated or joined together), device was announced.

1969 : SSI 10 - 100 comp/chip. LOGIC GATES, FFs.

1970 : Intel People, 9 months, chip with 1000 Transistors (4004μp)

1971 : μP - 4 bit INTEL

1971 : 4 bit Microprocessor was made by Intel group.

1975 : VLSI : Very large scale integration > 10,000 components per chip. ICs were made.

1975 : CHMOS - Complimentary High Metal Oxide Semiconductor ICs were announced by Intel.

1975 : MSI (Multiplenum, Address) 100 - 1000 comp/chip

1978 : LSI 8 bit μPs, ROM, RAM 1000 - 10,000 comp/chip

1980 : VLSI > 1,00,000 components/ser 16, 32 bit μPs

1981 : 16 bit μP > 1,00,000 components/ser 16, 32 bit μPs

1982 : 100,000 Transistors, 80286 Processor

1984 : CHMOS > 2,00,000 components/ser 16, 32 bit μPs

1985 : 32 bit μ p > 4,50,000 components/ser 16, 32 bit μPs

1986 : 64 bit μ p > 10,00,000 components/ser 16, 32 bit μPs

1987 : MMICS Monolithic Microwave Integrated Circuits

1989 : 1860 Intel's 64 bit CPU

1990 : ULSI > 500,000 Transistors ultra large scale

1992 : GSI > 10,00,000 Transistors Giant scale

100, 3 million Transistors, Pentium

1998 : 2 Million Gates/Die

2001 : 5 Million Gates / Die

2002 : 1000, 150 Million Transistors.

1 Gigabit Memory Chips

Nature is more SUPERIOR

2003 : 10 n.m. patterns, line width

2004 : Commercial Super Comp. 10TRILLION Flip Flops

2010 : Neoro - Computer Using Logic Structure Based on Human Brain

There are 10^7 cells/cm^3 in human brain

VLSI Technology Development :

3 μ Technology

↓

0.5 μ Technology

↓

0.12 μ Technology

ASICs (Application Specific Integrated Circuits)

HYBRID ICs

BI CMOS

MCMs (Multi Chip Modules)

3-D packages

Table 1

Table showing VLSI technology development predictions made in 1995.

	1995	1998	2001	2004	2007
Lithography (μ)	0.35	0.25	0.18	0.12	0.1
No. Gates/Die :	800K	2 M	5 M	10 M	20M
No. Bits/Die					
DRAM	64 M	256 M	1 G	4 G	16G
SRAM	16 M	64 M	256 M	1G	4G
Wafer Dia (mm)	200	200-400	400	400	400
Power (μW/Die)	15	30	40	40-120	40-200
Power Supply. (V)	3.3	2.2	2.2	1.5	1.5
Frequency (MHz)	100	175	250	350	500

UNIT - 1

Single Stage Amplifiers

In this Unit,

- Single stage amplifiers in the three configurations of C.E, C.B, C.C, with design aspects are given.
- Using the design formulae for A_V, A_I, R_i, R_o etc, the design of single stage amplifier circuits is to be studied.
- Single stage JFET amplifiers in C.D, C.S and C.G configurations are also given.
- The Hybrid - π equivalent circuit of BJT, expressions for Transistor conductances and capacitances are derived.
- Miller's theorem, definitions for f_β and f_T are also given.
- Numerical examples, with design emphasis are given.

1.1 Introduction

An electronic amplifier circuit is one, which modifies the characteristics of the input signal, when delivered the output side. The modification in the characteristics of the input signal can be with respect to voltage, current, power or phase. Any one or all these characteristics power, or phase may be changed by the amplifier circuit.

1.1.1 Classification of Amplifiers

Amplifier circuits are classified in different ways as indicated below :

Types of Classification

(a) Based on Frequency range

(b) Based on Type of coupling

(c) Based on Power delivered/conduction angle

(d) Based on Signal handled.

(a) Frequency Range

AF (Audio Freq.)	:	40 Hzs – 15/20 KHz
RF (Radio Freq.)	:	> 20 KHz
Video Frequency	:	5 – 8 MHz
VLF (Very Low Freq.)	:	10 – 30 KHz
LF (Low Frequency)	:	30 – 300 KHz
Medium Frequency	:	300 – 3000 KHz
High Frequency	:	3 – 30 MHz
VHF (Very High Freq.)	:	30 – 300 MHz
UHF (Ultra High Freq.)	:	300 – 3000 MHz
SHF (Super High Freq.)	:	3000 – 30,000 MHz

(b) Types of Coupling

1. Direct coupled
2. RC coupled
3. Transformer coupled
4. LC Tuned Amplifiers
5. Series fed.

(c) Output power delivered/conduction angle

1. Low power (tens of mW or less).
2. Medium power (hundreds of mW).
3. High power (Watts).

Class A	360°
Class B	180°
Class AB	180 – 360°
Class C	< 180°
Class D	Switching type.
Class S	Switching type.

(d) Type of signal handled

1. Large signal 2. Small signal

In addition to voltage amplification A_V, current amplification A_I or power amplification A_P is expected from an amplifier circuit. The amplifier circuit must also have other characteristics like High input impedance (Z_i or R_i), Low output impedance (Z_0 or R_0), Large Band Width (BW), High signal to Noise Ratio (S/N), and large *Figure of Merit (Gain BW product)*.

In order that the amplified signal is coupled to the load R_L or Z_L, for all frequencies of the input signal range, so that maximum power is transferred to the load, (the condition required for maximum power transfer is $|Z_0| = |Z_L|$ or $R_0 = R_L$) coupling the output of amplifier V_0 to load R_L or Z_L is important. When reactive elements are used in the amplifier circuit, and due to internal junction capacitances of the active device, the Z_i and Z_0 of the amplifier circuit change with frequency. As the input signal frequency varies over a wide range, and for all these signals amplification and impedance matching have to be achieved, coupling of the output of the amplifier to the load is important.

Since the gain A_V, A_I or A_P that can be obtained from a single stage amplifier circuit where only one active device (BJT, JFET or MOSFET) is used, the amplifier circuits are cascaded to get large gain. Multistage amplifier circuits are discussed in the next chapter.

When the frequency of the input signal is high (greater than A.F. range) due to internal junction capacitances of the actual device, the equivalent circuit of the BJT used earlier is not valid. So another model of BJT valid for high frequencies, proposed by Giacoletto is studied in this chapter.

1.2 Small Signal Analysis of Junction Transistor

Small Signal Analysis means, we assume that the input AC signal peak to peak to amplitude is very small around the operating point Q as shown in Fig. 1.1. The swing of the signal always lies in the active region, and so the output is not distorted. In the *Large Signal Analysis,* the swing of the input signal is over a wide range around the operating point. The magnitude of the input signal is very large. Because of this the operating region will extend into the cutoff region and also saturation region.

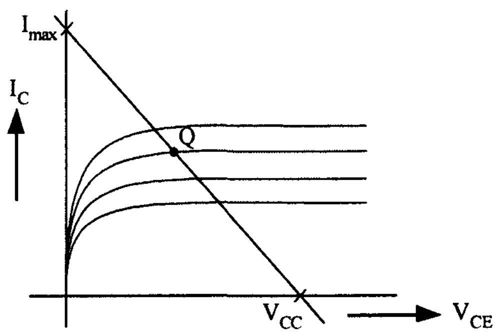


Fig. 1.1 Output Characteristics of BJT

1.3 Common Emitter Amplifier

Common Emitter Circuit is as shown in the Fig. 1.2. The DC supply, biasing resistors and coupling capacitors are not shown since we are performing an *AC analysis*.

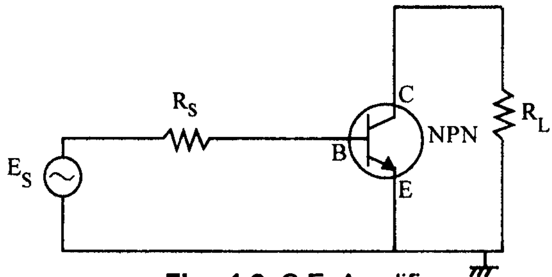


Fig. 1.2 C.E. Amplifier

E_S is the input signal source and R_S is its resistance. The *h-parameter* equivalent for the above circuit is as shown in Fig. 1.3.

$$h_{ie} = \left.\frac{V_{be}}{I_b}\right|_{V_{ce}=0} \qquad h_{re} = \left.\frac{V_{be}}{V_{ce}}\right|_{I_b=0}$$

$$h_{oe} = \left.\frac{I_c}{V_{ce}}\right|_{I_b=0} \qquad h_{fe} = \left.\frac{I_c}{I_b}\right|_{V_{ce}=0}$$

The typical values of the *h-parameter* for a transistor in Common Emitter Configuration are,

$$h_{ie} = 4\ K\Omega,$$

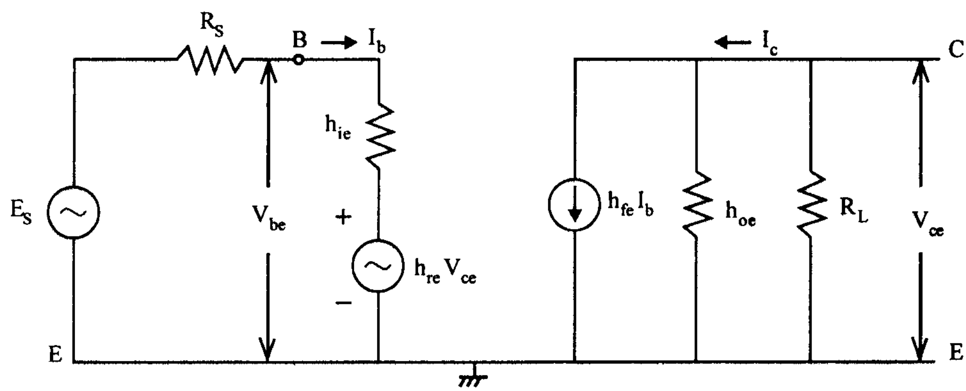


Fig. 1.3 h-parameter Equivalent Circuit

Since, $$h_{ie} = \frac{V_{be}}{I_b}$$

V_{be} is a fraction of volt 0.2V, I_b in μA, 100 μA and so on.

$$\therefore \qquad h_{ie} = \frac{0.2V}{50 \times 10^{-6}} = 4K\Omega$$

$$h_{fe} = I_c/I_b \simeq 100\,.$$

I_C is in mA and I_B in μA.

$\therefore \qquad h_{fe} >> 1 \simeq \beta$

$h_{re} = 0.2 \times 10^{-3}$. Because, it is the *Reverse* Voltage Gain.

$$h_{re} = \frac{V_{be}}{V_{ce}}$$

and $\qquad V_{ce} > V_{be};$

$$h_{re} = \frac{\text{Input}}{\text{Output}}$$

Output is >> input, because amplification takes place. Therefore $h_{re} << 1$.

$$h_{oe} = 8\ \mu\mho \quad \text{and} \quad h_{oe} = \frac{I_c}{V_{ce}}.$$

1.3.1 Input Resistance of the Amplifier Circuit (R_i)

The general expression for R_i in the case of Common Emitter Transistor Circuit is

$$R_i = h_{ie} - \frac{h_{fe}h_{re}}{h_{oe} + \frac{1}{R_L}} \qquad .....(1.1)$$

For Common Emitter Configuration,

$$R_i = h_{ie} - \frac{h_{fe}h_{re}}{h_{oe} + \frac{1}{R_L}} \qquad .....(1.2)$$

R_i depends on R_L. If R_L is very small, $\frac{1}{R_L}$ is large, therefore the denominator in the second term is large or it can be neglected.

$\therefore \qquad R_i \cong h_{ie}$

If R_L increases, the second term cannot be neglected.

$$R_i = h_{ie} - (\text{finite value})$$

Therefore, R_i decreases as R_L increases. If R_L is very large, $\frac{1}{R_L}$ will be negligible compared to h_{oe}. Therefore, R_i remains constant . The graph showing R_i versus R_L is indicated in Fig. 1.4. R_i is not affected by R_L if R_L < 1 KΩ and R_L > 1 MΩ as shown in Fig. 1.4.

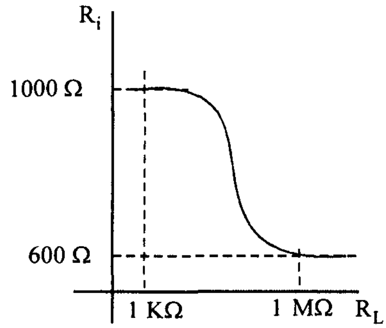


Fig. 1.4 Variation of R_i with R_L

R_i varies with frequency f because h-parameters will vary with frequency. h_{fe}, h_{re} will change with frequency f of the input signal.

1.3.2 Output Resistance of an Amplifier Circuit (R_0)

For Common Emitter Configuration,

$$R_o = \frac{1}{h_{oe} - \left(\frac{h_{re}h_{fe}}{h_{ie} + R_s}\right)} \quad \text{.....(1.3)}$$

R_s is the resistance of the source. It is of the order of few hundred Ω.
R_o depends on R_s. If R_s is very small compared to h_{ie},

$$R_o = \frac{1}{h_{oe} - \frac{h_{re}h_{fe}}{h_{ie}}} \text{ (independent of } R_s \text{)} \quad \text{.....(1.4)}$$

Then, R_o will be large of the order of few hundred KΩ. If R_s is very large, then

$$R_o \simeq \frac{1}{h_{oe}} \simeq 150 \text{ K}\Omega.$$

The graph is as shown in Fig. 1.5.

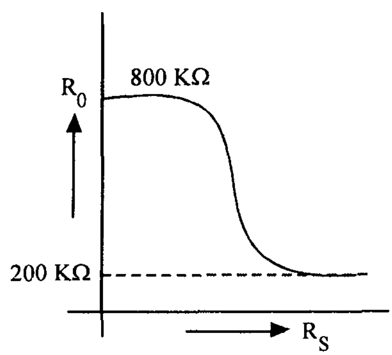


Fig. 1.5 Variation of R_0 with R_S

1.3.3 Current Gain (A_i)

$$A_I = \frac{-h_{fe}}{1+h_{oe}R_L} \qquad .....(1.5)$$

If R_L is very small, $A_i \simeq h_{fe} \simeq 100$. So, Current Gain is large for Common Emitter Configuration. As R_L increases, A_I drops and when $R_L = \infty$, $A_i = 0$. Because, when $R_L = \infty$, output current I_0 or load current $I_L = 0$. Therefore, $A_I = 0$. Variation of A_i with R_L is shown in Fig. 1.6.

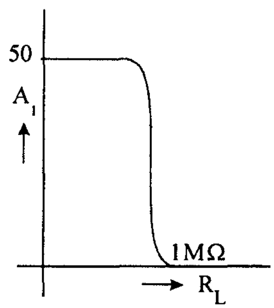


Fig 1.6 Variation of A_I with R_L

1.3.4 Voltage Gain (A_V)

$$A_V = \frac{-h_{fe}R_L}{h_{ie}+R_L(h_{ie}h_{oe}-h_{fe}h_{re})} \qquad .....(1.6)$$

If R_L is low, most of the output current flows through R_L. As R_L increases, output voltage increases and hence A_V increases. But if $R_L >> \frac{1}{h_{oe}}$, then the current from the current generator in the ***h-parameters*** equivalent circuit flows through h_{oe} and not R_L.

Then the, Output Voltage $= h_{fe} \cdot I_b \cdot \frac{1}{h_{oe}}$

(R_L is in parallel with h_{oe}. So voltage across h_{oe}= voltage across R_L). Therefore, V_0 remains constant as output voltage remains constant (Fig.1.7).

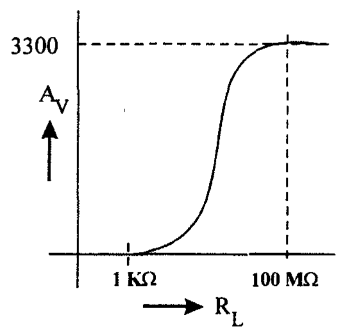


Fig. 1.7 Variation of A_V with R_L

1.3.5 Power Gain

As R_L increases, A_I decreases. As R_L increases, A_V also increases.

Therefore, Power Gain which is the product of the two, A_V and A_I varies as shown in Fig. 1.8.

$$A_P = A_V A_I$$

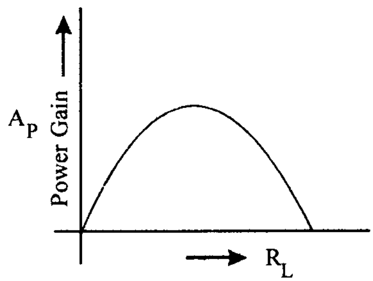


Fig. 1.8 Variation of A_P with R_L

Power Gain is maximum when R_L is in the range 100 KΩ – 1 MΩ i.e., when R_L is equal to the output resistance of the transistor. Maximum power will be delivered, under such conditions.

Therefore, it can be summarised as, Common Emitter Transistor Amplifier Circuit will have,

1. *Low to Moderate Input Resistance (300Ω – 5KΩ).*
2. *Moderately High Output Resistance (10KΩ – 100KΩ).*
3. *Large Current Amplification.*
4. *Large Voltage Amplification.*
5. *Large Power Gain.*
6. *180^0 phase-shift between input and output voltages.*

As the input current I_B, increases, I_C increases therefore drop across R_C increases and $V_0 = V_{CC} - V_I$ drop across R_C. Therefore, there is a phase shift of 180^0.

The amplifier circuit is shown in Fig.1.9.

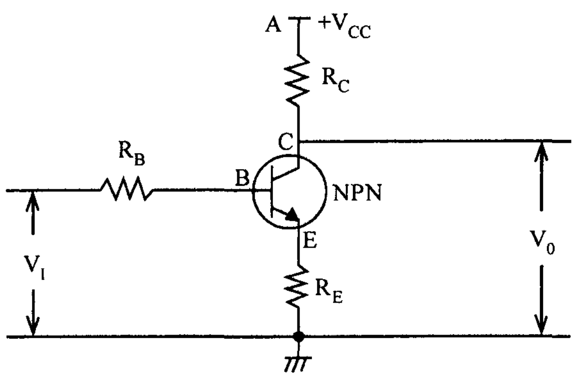


Fig. 1.9 CE Amplifier Circuit

1.4 Common Base Amplifier

The circuit diagram considering ***only AC*** is shown in Fig. 1.10.

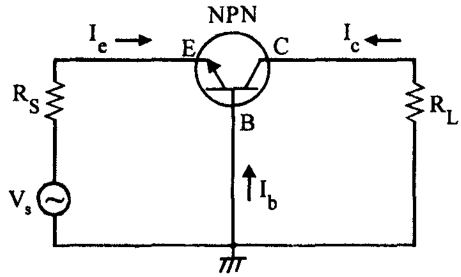


Fig. 1.10 CB Amplifier

$$h_{ib} = \left.\frac{V_{eb}}{I_e}\right|_{V_{cb}=0}$$

V_{eb} is small fraction of a volt. I_e is in mA. So, h_{ib} is small.

$$h_{fb} = \left.\frac{I_c}{I_e}\right|_{V_{cb}=0} = -0.99 \text{ (Typical Value)}$$

$$I_c < I_e \qquad \therefore \qquad h_{fb} < 1$$

$$h_{ob} = \left.\frac{I_c}{V_{cb}}\right|_{I_e=0} = 7.7 \times 10^{-8} \text{ mhos (Typical Value)}$$

I_c will be very small because $I_e = 0$. This current flows in between base and collector loop.

$$h_{rb} = \left.\frac{V_{eb}}{V_{cb}}\right|_{I_e=0} = 37 \times 10^{-6} \text{ (Typical Value)}$$

h_{rb} is small, because V_{eb} will be very small and V_{cb} is large.

1.4.1 Input Resistance (R_i)

$$R_i = h_{ib} - \frac{h_{fb}.h_{rb}}{h_{ob} + \frac{1}{R_L}}; \quad h_{fb} \text{ is } -\text{ve} \qquad .....(1.7)$$

when R_L is small < 100 KΩ, the second term can be neglected.

$$\therefore \qquad R_i = h_{ib} \simeq 30\Omega.$$

when R_L is very large, $\frac{1}{R_L}$ can be neglected.

$$R_i = h_{ib} - \frac{h_{fb}.h_{rb}}{h_{ob}}$$

So $\quad R_i \simeq 500\Omega$ (Typical value) $\quad$ [$\because h_{fb}$ is negative]

$$\therefore \qquad R_i = h_{ib} + \frac{h_{fb}h_{rb}}{h_{ob}}$$

The variation of R_i with R_L is shown in Fig. 1.11. R_i varies from 20Ω to 500Ω.

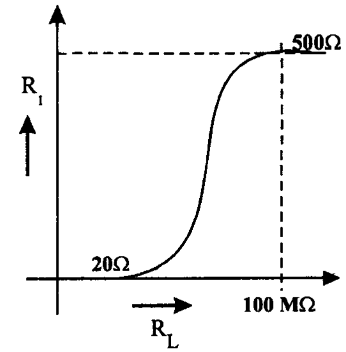


Fig. 1.11 Variation of R_i with R_L

1.4.2 Output Resistance (R_0)

$$R_o = \frac{1}{h_{ob} - \dfrac{h_{rb}h_{fb}}{h_{ib} + R_s}} \qquad \text{.....(1.8)}$$

If R_s is small, $\quad R_o = 1 \Big/ \left(h_{ob} - \dfrac{h_{rb}h_{fb}}{h_{ib}} \right)$

But h_{fb} is negative.

$$\therefore \qquad R_o = \frac{1}{h_{ob} + \dfrac{h_{rb}h_{fb}}{h_{ib}}}$$

This will be sufficiently large, of the order of 300 KΩ. Therefore, value of h_{ob} is small. As R_s increases, $R_0 = \dfrac{1}{h_{ob}}$ also increases. [This will be much larger because, in the previous case, in the denominator, some quantity is subtracted from h_{ob}.]

$$\therefore \qquad R_o = 12M\Omega$$

The variation of R_0 with R_s is shown in Fig. 1.12.

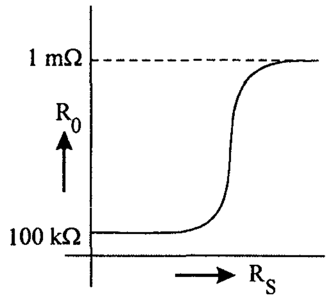


Fig. 1.12 Variation of R_0 with R_S

1.4.3 Current Gain (A_i)

$$A_i = \frac{-h_{fb}}{1+h_{ob}R_L} \qquad .....(1.9)$$

A_i is < 1. Because h_{fe} < 1. As R_L increases, A_i decreases. A_i is negative due to h_{fb}. The variation of A_i with R_L is shown in Fig. 1.13.

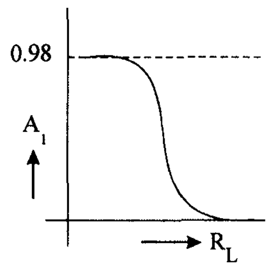


Fig. 1.13 Variation of A_i with R_L

1.4.4 Voltage Gain (A_V)

$$A_v = \frac{-h_{fb}R_L}{h_{ib}+R_L(h_{ib}h_{ob}-h_{fb}h_{rb})} \qquad ....(1.10)$$

As R_L increases, A_V also increases. If R_L tends to zero, A_V also tends to zero. ($A_V \rightarrow 0$, as $R_L \rightarrow 0$). The variation of Voltage Gain A_V with R_L is shown in Fig. 1.14.

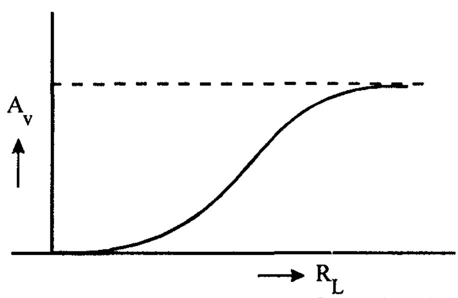


Fig. 1.14 Variation of A_v with R_L

1.4.5 Power Gain (A_P)

Power Gain $A_P = A_V \cdot A_I$

A_V increases as R_L increases. But A_I decreases as R_L increases. Therefore, Power Gain, which is product of both, varies with R_L as shown in Fig. 1.15.

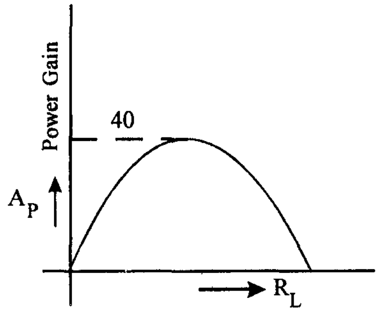


Fig 1.15 Variation of A_P with R_L

The characteristics of Common Base Amplifier with typical values are as given below.

1. *Low Input Resistance (few 100 Ω).*
2. *High Output Resistance (MΩ).*
3. *Current Amplification $A_I < 1$.*
4. *High Voltage Amplification and No Phase Inversion*
5. *Moderate Power Gain (30).* $\because$ $A_i < 1$.

1.5 Common Collector Amplifier

The simplified circuit diagram for AC of a transistor (BJT) in Common Collector Configuration is as shown in Fig. 1.16 (without biasing resistors).

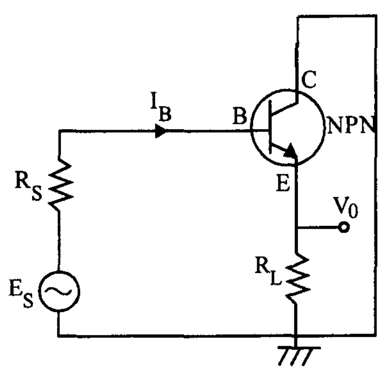


Fig. 1.16 CC Amplifier

The ***h-parameter*** equivalent circuit of transistor in Common Collector Configuration is shown in Fig. 1.17.

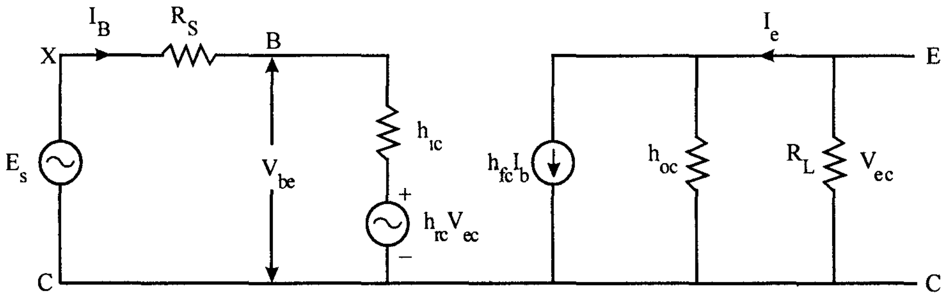


Fig. 1.17 h-parameter Equivalent Circuit

$$h_{ic} = \left.\frac{V_{bc}}{I_b}\right|_{V_{ec}=0} = 2{,}780\ \Omega \text{ (Typical Value)}$$

$$h_{oc} = \left.\frac{I_e}{V_{ec}}\right|_{I_b=0} = 7.7 \times 10^{-6} \text{ mhos (Typical Value)}$$

$$h_{fc} = -\left.\frac{I_e}{I_b}\right|_{V_{ce}=0} = 100 \text{ (Typical value)}$$

$\because\ I_e >> I_b$.

h_{fc} is negative because, I_E and I_B are in opposite direction.

$$h_{rc} = \left.\frac{V_{bc}}{V_{ec}}\right|_{I_b=0} ; \quad V_{bc} = V_{ec} \text{ (Typical Value)}$$

Because, $I_B = 0$, E - B junction is not forward baised.

$\therefore$ $V_{EB} = 0$.

For other circuit viz., Common Base and Common Emitter, h_r is much less than 1.

For Common Collector Configuration, $h_{rc} \simeq 1$.

The graphs (variation with R_C) are similar to Common Base Configuration.

Characteristics

1. *High Input Resistance* $\simeq 3\ K\Omega\ (R_i)$
2. *Low Output Resistance 30* Ω. (R_0)
3. *Good Current Amplification* $A_i >> 1$
4. $A_v \leq 1$
5. *Lowest Power Gain of all the configurations.*

Since, A_v is < 1, the output voltage (Emitter Voltage) follows the input signal variation. Hence it is also known as *Emitter Follower*. The graphs of variation with R_L and R_S are similar to Common Base amplifier.

Example : 1.1

For the circuit shown in Fig.1.18 estimate A_I, A_V, R_i and R_0 using reasonable approximations. The ***h-parameters*** for the transistor are given as

$h_{fe} = 100$ $h_{ie} = 2000\ \Omega$ h_{re} is negligible and $h_{oe} = 10^{-5}$ mhos(℧).

$I_b = 100\ \mu A$.

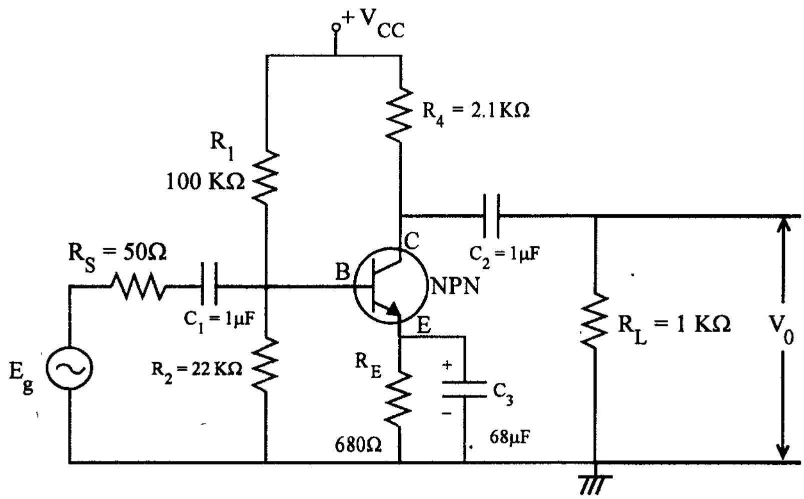


Fig. 1.18 CE Amplifier Circuit

Solution :

At the test frequency capacitive reactances can be neglected. V_{CC} point is at ground because the AC potential at $V_{CC} = 0$. So it is at ground. R_1 is connected between base and ground for AC. Therefore, $R_1 \parallel R_2$. R_4 is connected between collector and ground. So R_4 is in parallel with $1/h_{oe}$ in the output. The A.C. equivalent circuit in terms of ***h-parameters*** of the transistor is shown in Fig. 1.19.

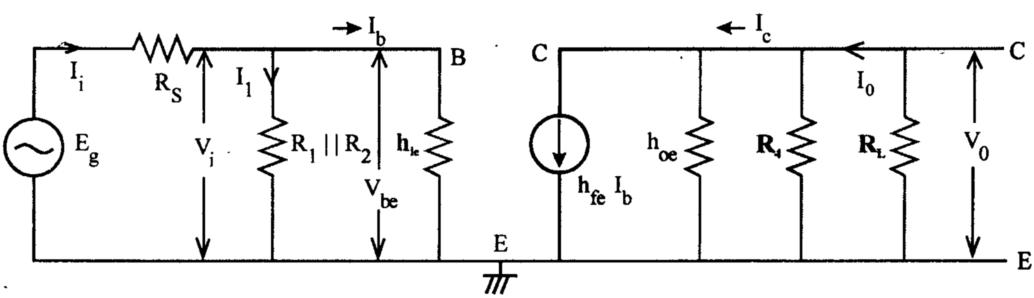


Fig. 1.19 Equivalent Circuit

The voltage source $h_{re}\ V_{ce}$ is not shown since, h_{re} is negligible. At the test frequency of the input signal ,the capacitors C_1 and C_2 can be regarded as short circuits. So they are not shown in the AC equivalent circuit. The emitter is at ground potential. Because X_{C_3} is also negligible, all the AC passes through C_3. Therefore, emitter is at ground potential and this circuit is in Common Emitter Configuration.

1.5.1 Input Resistance (R_i)

R_i input resistance looking into the base is h_{ie} only

$$\text{The expression for } R_i \text{ of the transistor alone} = h_{ie} - \left(\frac{h_{fe}\, h_{re}}{h_{oe} + \dfrac{1}{R_L}} \right).$$

R_L is very small and h_{re} is negligible. Therefore, the second term can be neglected. So R_i of the transistor alone is h_{ie}. Now R_i of the entire amplifier circuit, considering the bias resistors is,

$$R_i = h_{ie} \,||\, R_1 \,||\, R_2$$

$$\therefore \qquad \frac{R_1 R_2}{R_1 + R_2} = \frac{100 \times 22}{100 + 22} = 18\ \text{K}\Omega$$

$$\therefore \qquad R_i = \frac{18 \times 2}{18 + 2} = 1.8\ \text{K}\Omega$$

1.5.2 Output Resistance (R_0)

$$R_0 = \frac{1}{h_{oe} - \left[\dfrac{h_{re} h_{fe}}{h_{ie} + R_S} \right]} \qquad \text{.....(7.11)}$$

Because, h_{re} is negligible, R_0 of the transistor alone in terms of ***h-parameters*** of the transistor $= \dfrac{1}{h_{oe}}$. Now R_0 of the entire amplifier circuit is,

$$\left(\frac{1}{h_{oe}} \,||\, R_4 \,||\, R_L \right) = (2.1 \times 10^{+3}) \,||\, (100\ \text{K}\Omega) \,||\, (1\ \text{k}\Omega)$$

$$= 2\text{K}\Omega. \,||\, (1\ \text{k}\Omega) = 0.67\ \text{k}\Omega$$

1.5.3 Current Gain (A_i)

To determine A_i the direct formula for A_i in transistor in Common Emitter Configuration is, $\dfrac{-h_{fe}}{1 + h_{oe} R_L}$.

But this cannot be used because the input current I_i gets divided into I_1 and I_b. There is some current flowing through the parallel configuration of R_1 and R_2. So the above formula cannot be used.

$$V_{be} = I_b \cdot h_{ie}$$

$$V_{be} = 10^{-4} \times (2000) = 0.2\text{V}. \text{ (This is AC Voltage not DC)}$$

Voltage across R_1 R_2 parallel configuration is also V_{be}.

$$\therefore \qquad \text{Current} \quad I_1 = \frac{V_{be}}{50 \times 10^3} = \frac{0.2}{50\text{k}\Omega} = 4\ \mu\text{A}.$$

Therefore, total input current,

$$I_i = I_1 + I_b = 4 + 100 = 104\ \mu A.$$

I_0 is the current through the 1KΩ load.

$\frac{1}{h_{oe}}$ = 100 KΩ is very large compared with R_4 and R_L. Therefore, all the current on the output side, $h_{fe}\, I_b$ gets divided between R_4 and R_L only.

Therefore, current through R_L is I_0,

$$I_0 = h_{fe}\, I_b \cdot \left[\frac{R_4}{R_4 + R_L}\right]$$

$$I_o = 100 \times 10^{-4}\ \frac{2.1\times10^3}{(2.1\times10^3+10^3)}$$

$$= 6.78 \text{ mA.}$$

Therefore, current amplification,

$$A_i = \frac{I_0}{I_i}$$

$$= \frac{6.78\times10^{-3}}{104\times10^{-6}} = 65.$$

$$A_v = \frac{V_0}{V_i}; \quad V_i = V_{be}$$

$$V_o = -\, I_0 \cdot R_L$$

$$= (-\,6.78 \times 10^3) \times (10^3)$$

$$= -\,6.78\text{V}$$

Because, the direction of I_0 is taken as entering into the circuit. But actually I_0 flows down, because V_0 is measured with respect to ground.

$\therefore$ $$A_v = \frac{-6.78}{0.2}$$

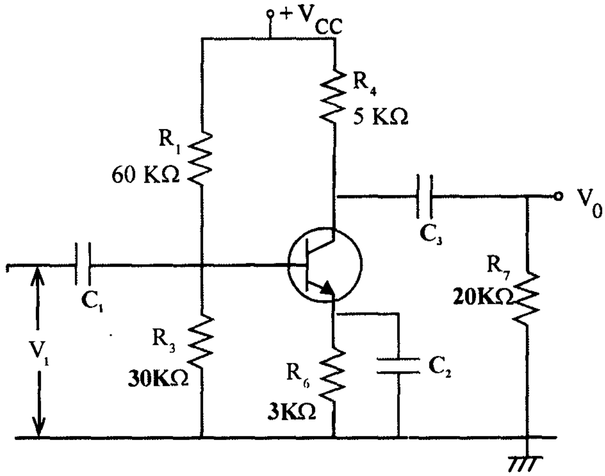
$$= -\,33.9$$

Negative sign indicates that there is phase shift of 180^0 between input and output voltages, i.e. as base voltage goes more positive, (it is NPN transistor), the collector voltage goes more negative.

Example : 1.2

For the circuit shown, in Fig. (1.20), estimate A_v and R_i. $\frac{1}{h_{oe}}$ is large compared with the load seen by the transistor. All capacitors have negligible reactance at the test frequency.

$h_{ie} = 1K\Omega, \quad h_{fe} = 99 \quad h_{re}$ is negligible.



Solution :

Fig. 1.20 AC Amplifier Circuit (Ex : 1.2)

The same circuit can be redrawn as,

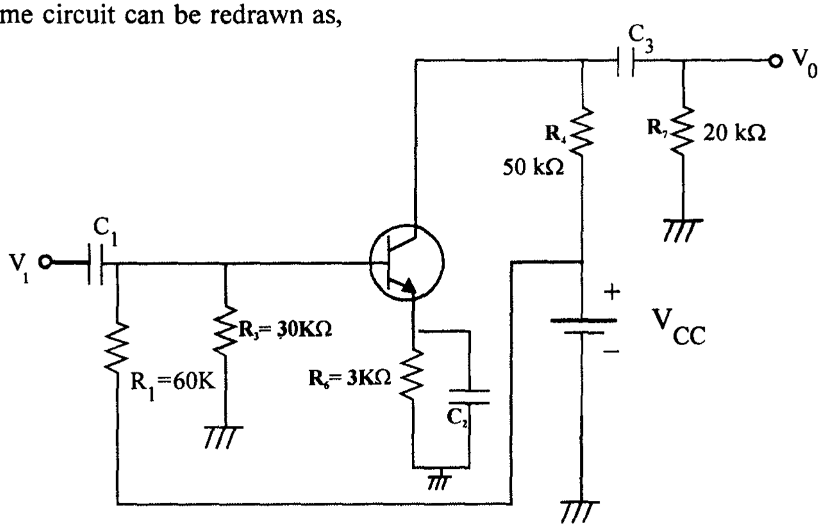


Fig. 1.21 Redrawn Circuit of AC Amplifier

In the second circuit also, R_4 is between collector and positive of V_{CC}. R_1 is between $+V_{CC}$ and base. Hence both the circuits are identical. Circuit in Fig. 1.20 is same as circuit in Fig. 1.21. In the AC equivalent circuit, the direct current source should be shorted to ground. Therefore, R_4 is between collector and ground and R_1 is between base and ground. Therefore, R_4 is in parallel with R_7 and R_1 is in parallel with R_3 (Fig. 1.21).

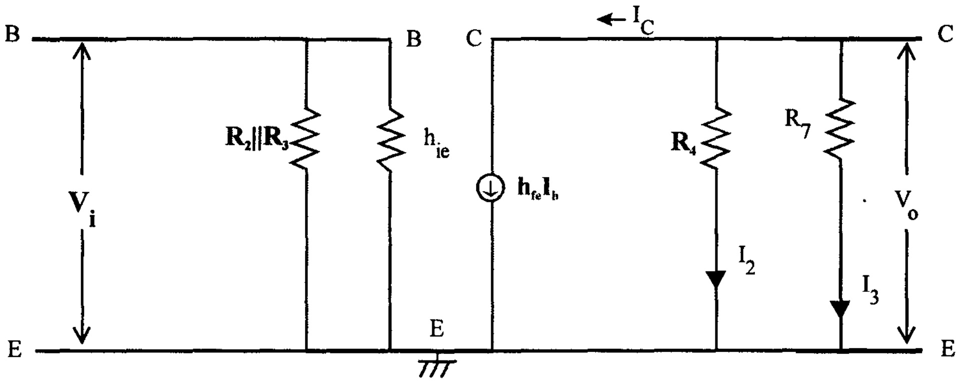


Fig. 1.22 h - Parameter equivalent circuit

$$R_2 \parallel R_3 = \frac{60 \times 30}{60+30} = \frac{1800}{90} = 20K\Omega.$$

$$R_4 \parallel R_7 = R_L = \frac{5 \times 20}{5+20} = 4K\Omega.$$

Therefore, the circuit reduces to, (as shown in Fig. 1.23).

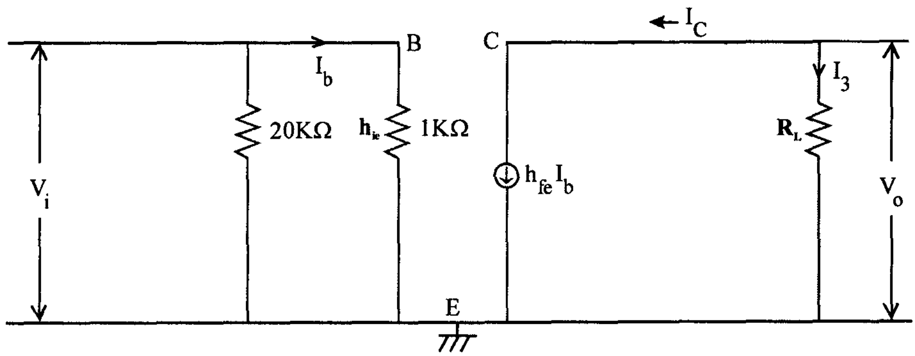


Fig. 1.23 Simplified circuit of Fig. 1.22

$$I_b = \frac{V_i}{h_{ie}} \qquad (\because h_{re} \text{ is negligible})$$

$$I_c = h_{fe}\, I_b = \frac{h_{fe}.V_i}{h_{ie}}$$

$$\therefore \qquad V_0 = -I_c \,.\, R_L = -\frac{h_{fe}V_i.R_L}{h_{ie}}$$

$$A_v = \frac{V_0}{V_i} = -\frac{h_{fe}R_L}{h_{ie}} = \frac{-99\ (14.28 \times 10^3)}{10^3}$$

$$A_v = -400$$

R_i is the parallel combination of 20KΩ and h_{ie}.

$$\frac{20 \times 1K\Omega}{20+1} = 950\Omega$$

Example : 1.3

Given a single stage transistor amplifier with *h - parameter* as h_{ic} = 1.1 KΩ, h_{rc} = 1, h_{fc} = –51, h_{oc} = 25 μA/v. Calculate A_I, A_V, A_{Vs}, R_i, and R_o for the Common Collector Configuration, with $R_s = R_L$ = 10K.

Solution :

$$A_I = \frac{-h_{fc}}{(1+h_{oc} R_L)} = \frac{51}{1+25\times10^{-6}\times10^4} = 40.8$$

$$R_i = h_{ic} + h_{rc} A_I R_L = 1.1 \times 10^3 + 1 \times 40.8 \times 10^4 = 409.1 \text{ K}\Omega$$

$$A_v = \frac{A_I . R_L}{R_i} = \frac{40.8\times10^4}{409.1\times10^3} = 0.998$$

$$A_{vs} = \frac{A_V . R_i}{R_i + R_s} = \frac{0.998\times409.1}{419.1} = 0.974$$

$$R_0 = \frac{1}{h_{oc} - \dfrac{h_{fc}.h_{rc}}{h_{ic}+R_s}} = \frac{1}{25\times10^{-6} + \dfrac{51\times1}{(1.1+10)10^3}} = \frac{1}{4.625\times10^{-3}}$$

$$R_0 = 217\Omega$$

Example : 1.4

For any transistor amplifier prove that

$$R_i = \frac{h_i}{1-h_r A_V}$$

Solution :

$$R_i = h_i - \frac{h_f . h_r}{h_o + \dfrac{1}{R_L}}$$

But $$A_I = \frac{-h_f}{1+h_o . R_L}$$

$\therefore$ $$R_i = h_i + h_r A_I R_L$$

$$\therefore \qquad A_v = \frac{A_I . R_L}{R_i}$$

$$R_L = \frac{A_V . R_i}{A_I}$$

Substituting this value of R_L in equation (1)

$$R_i = h_i + \frac{h_r . A_I . A_V . R_i}{A_I} = h_i + h_r . A_V . R_i$$

$$R_i [1 - h_r A_v] = h_i \qquad \therefore \boxed{R_i = \frac{h_i}{1 - h_r A_v}}$$

Example : 1.5

For a Common Emitter Configuration, what is the maximum value of R_L for which R_1 differs by not more than 10% of its value at $R_2 = 0$?

$h_{ie} = 1100\Omega$; $\qquad h_{fe} = 50$

$h_{re} = 2.50 \times 10^{-4}$; $\qquad h_{oe} = 25\mu$ A/v

Solution :

Expression for R_i is,

$$R_i = h_{ie} - \frac{h_{fe} . h_{re}}{h_{oe} + \frac{1}{R_L}} .$$

If $R_2 = 0$, $R_i = h_{ie}$. The value of R_L for which $R_i = 0.9\ h_{ie}$ is found from the expression,

$$0.9\ h_{ie} = h_{ie} - \frac{h_{fe} . h_{re}}{h_{oe} + \frac{1}{R_L}}$$

or $$\frac{h_{fe} . h_{re}}{h_{oe} + \frac{1}{R_L}} = h_{ie} - 0.9\ h_{ie} = 0.1\ h_{ie}$$

$$\frac{h_{fe} . h_{re}}{0.1 h_{ie}} = h_{oe} + \frac{1}{R_L}$$

$$\frac{1}{R_L} = \frac{h_{fe} . h_{re}}{0.1 h_{ie}} - h_{oe} = \frac{h_{fe}\ h_{re} - 0.1\ h_{oe}\ h_{re}}{0.1 h_{ie}}$$

or $$R_L = \frac{0.1 h_{ie}}{h_{fe} h_{re} - 0.1 h_{oe}\ h_{ie}} = \frac{0.1 \times 1100}{50 \times 2.5 \times 10^{-4} - 0.1 \times 1100 \times 25 \times 10^{-6}}$$

$$R_L = 11.3 K\Omega$$

1.6 JFET Amplifiers

1.6.1 Common Drain Amplifier

The circuit is shown in Fig.1.24.

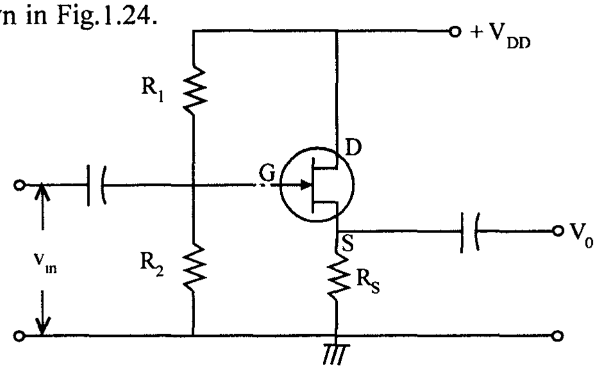


Fig. 1.24 Common drain amplifier circuit

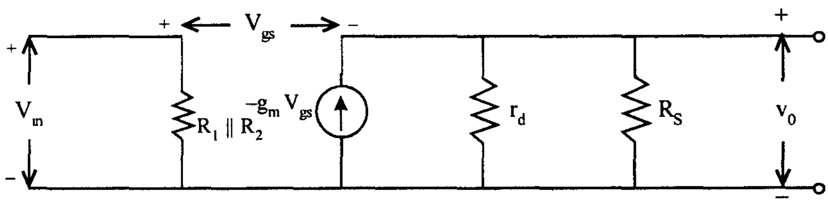


Fig. 1.25 Equivalent circuit

KVL

$$V_{in} - V_{gs} = V_0$$

$$V_0 = R_S' \cdot g_m [V_{in} - V_0]$$

where $R_S' = R_S \parallel r_d$

$$V_0 = R_S' g_m V_{in} - R_S' g_m V_0$$

$$V_0 \times [1 + R_S' g_m] = R_S' g_m V_{in}$$

$$\therefore \quad \boxed{\frac{V_0}{V_{in}} = \frac{R_S' g_m}{1 + R_S' g_m}}$$

1.6.2 Common Gate Amplifier

Small signal equivalent of Fig. 1.26.

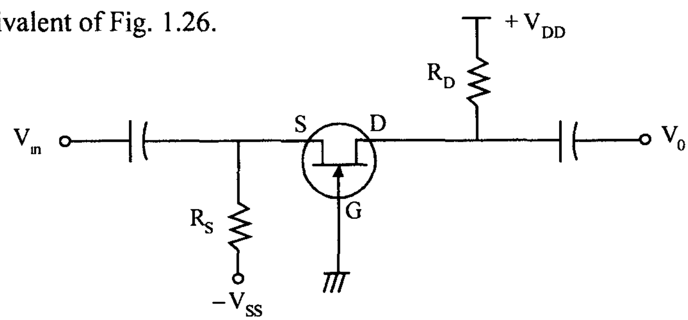


Fig. 1.26 Common Gate Amplifier

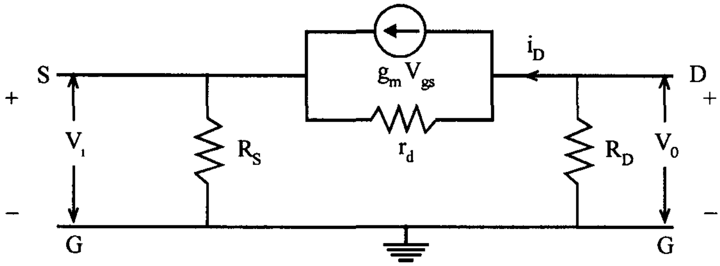


Fig. 1.27 (a) Equivalent circuit

$$V_0 = -i_D R_D$$

$$i_D = g_m V_{gs} + \frac{V_{ds}}{r_d}$$

$$V_0 = -R_D \left[g_m V_{gs} + \frac{V_{ds}}{r_d} \right]$$

$$V_0 = V_{in} + V_{ds}$$
$$V_{ds} = V_0 - V_{in}$$

$$V_0 = -R_D \left[g_m (-V_{in}) + \frac{V_0 - V_{in}}{r_d} \right]$$

$$V_0 = g_m R_D V_{in} - \frac{V_0 R_D}{r_d} + \frac{V_{in}}{r_d} R_D$$

$$V_0 \left[1 + \frac{R_D}{r_d} \right] = \left[g_m R_D + \frac{R_D}{r_d} \right] V_{in}$$

$$\frac{V_0}{V_{in}} = \frac{g_m R_D + \dfrac{R_D}{r_d}}{1 + \dfrac{R_D}{r_d}} = \frac{(g_m r_d + 1) R_D}{r_d + R_D}$$

$$\boxed{A_V = \frac{(\mu + 1) R_D}{r_d + R_D}}$$

JFET amplifier has very *small gate leakage current.* G – S junction is a reverse biased P – N junction. In the ideal case, $I_G = 0$. This is equivalent to saying, $I_D = I_S$ ($\because$ $I_G = 0$).

JFET amplifier has high input impedance, therefore the input side i.e, G – S junction is reverse biased. [For a bipolar transistor amplifier circuit, the input side i.e., E – B junction is forward. So it has less resistance].

The price paid for high input resistance is less control over output current. That is, a JFET takes larger changes in input voltage to produce changes in output current, therefore a *JFET amplifier has much less voltage gain than a bipolar amplifier.*

Equation

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

This is a square law. This is another name for parabolic shape. So JFET is often called as a *square law device.*

Example : 1.6

What is the DC input resistance of a JFET which has I_{GSS} (gate leakage current) = 5 picoamperes (pA) at 20 V ?

Solution :

$$R_{GS} = \text{Input resistance,}$$

$$= \frac{20\text{V}}{5 \times 10^{-12}} = 4 \times 10^{12}\,\Omega$$

1.6.3 Common Source (CS) Amplifier

When a small AC signal is coupled into the gate, it produces variations in gate – source voltage. This produces a sinusoidal drain current. Since AC flows through the drain resistor, we get an amplified AC voltage at the output.

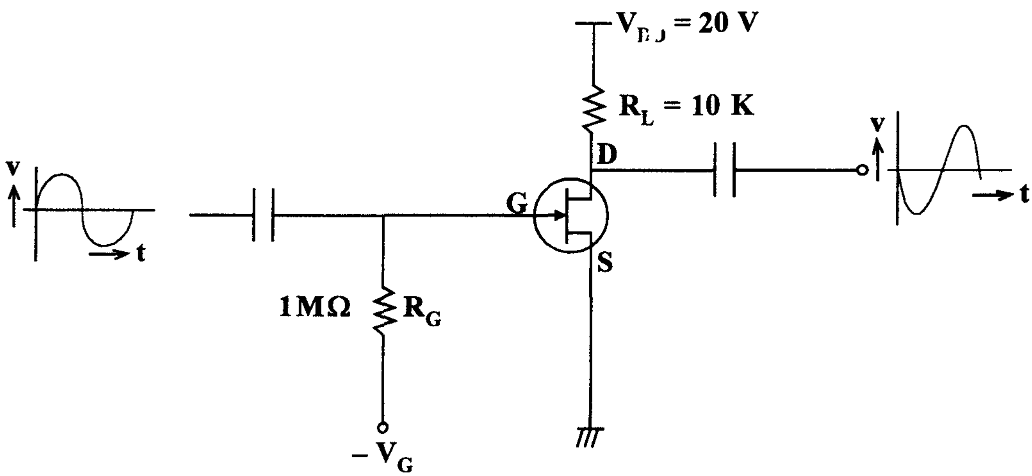
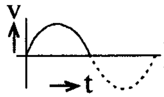


Fig. 1.27 (b) Common Source Amplifier

This is FET equivalent of common emitter transistor amplifier in BJT. As common emitter configuration is widely used, C.S. configuration is also widely used in the case of FETs. As in the case of common emitter configuration, C.S configuration also introduces a phase-shift of 180^0.

$$V_{DS} = V_{DD} - I_D \cdot R_L \text{ (DC values)}$$

Suppose AC input of positive voltage (positive half cycle 

) is applied. Gate is p - type. So reverse bias of G – S junction is reduced. So I_D increases, because V_{DS} decreases. Therefore, with respect to AC, initially AC is zero, now the AC signal (output) is negative, therefore, V_D decrease. So for positive input AC, the AC output i s negative. Hence it introduces a phase-shift.

Low frequency equivalent circuit (C)

Capacitance and DC voltages are shorted. FET is replaced by its small signal model so the equivalent circuit is as shown in Fig. 1.27 (c).

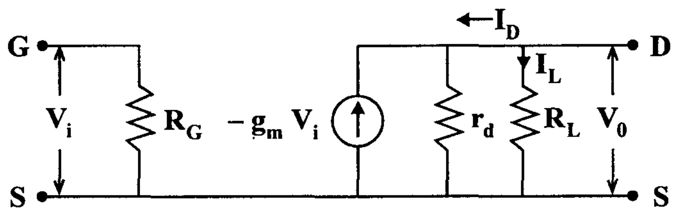


Fig. 1.27 (c) C.S amplifier

I_L = AC drain current

r_d = drain resistance

$$V_0 = I_d R_L$$

$$I_d = -g_m V_i \frac{r_d}{r_d + R_L}$$

$$V_0 = -g_m \cdot V_i \left\{ \frac{r_d \times R_L}{r_d + R_L} \right\}$$

$\therefore$ $$\text{Voltage gain} = Av = \frac{V_0}{V_i}$$

$$= \frac{-g_m . r_d . R_L}{r_d + R_L}$$

But $\qquad r_d >> R_L$

$\therefore \qquad r_d + R_L \simeq r_d$

$$\therefore \qquad \boxed{Av \simeq \frac{-g_m . r_d . R_L}{r_d}}$$

$$\boxed{Av \simeq - g_m . R_L}$$

1.6.4 Phase Inversion

An increase in gate - source voltage produces more drain current, which means that drain voltage is decreasing because drop across R_D increases.

$$V_{DD} - I_D R_D = V_{DS} \text{ decreases.}$$

So increasing input voltage produces decreasing output voltage. Therefore there is phase inversion.

1.6.5 Voltage Gain

$$V_0 = - g_m V_{gs} R_D \quad \text{(phase inversion for negative sign)}$$

$$V_{in} = V_{gs}$$

$$\therefore \qquad A_V = \frac{V_0}{V_i}$$

$$= - g_m R_D.$$

1.6.6 Distortion

The transconductance curve of a JFET is non-linear. It follows square law. Because of this, *JFET distorts large signals*. This is known as *square law distortion*.

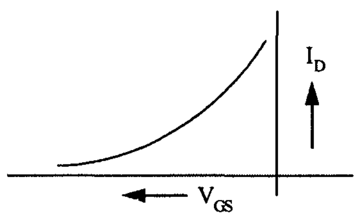


Fig. 1.28 Transfer Characteristic of JFET

1.6.7 Swamping Resistor

The resistor that is connected in series with the source resistance R_S is called *Swamping resistor*. The source resistance R_S is bypassed by C_S, the source bypass capacitor. (Similarly to R_E in BJT circuit)

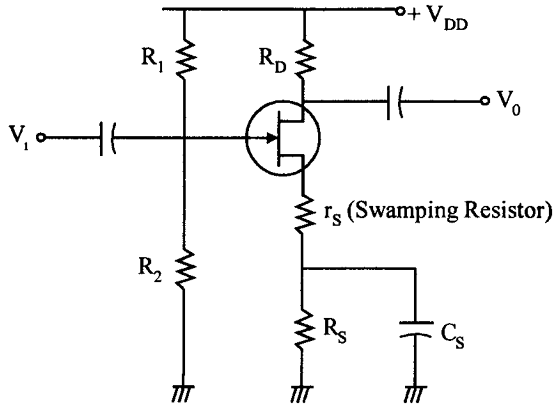


Fig. 1.29 Circuit with Swamping resistor

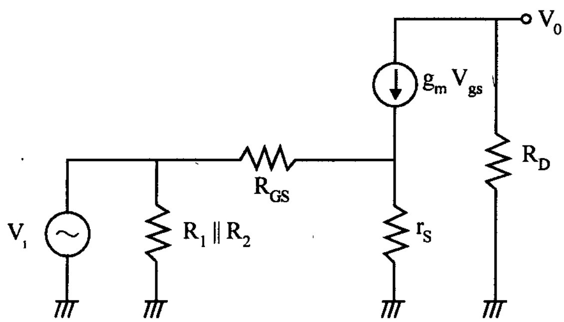


Fig. 1.30 Equivalent circuit

If r_s is not there, source is at ground potential. But when r_s is connected, AC current is passing, through this, because source is not at ground potential. Thus local feedback will help in reaching the non-linearity of the square law transconductance curve of JFET. So distortion will be reduced.

The voltage gain will be $(-R_D / r_s)$. So the effect of swamping resistor is,

1. It reduces distortion.
2. It reduces voltage gain.

$$V_{gs} + g_m V_{gs} r_s - V_{in} = 0$$

$$V_{in} = (1 + g_m r_s) V_{gs}$$

$$V_0 = -g_m V_{gs} R_D$$

$$\therefore \quad \frac{V_0}{V_{in}} = ?$$

$$A_V = \frac{-R_D}{r_S + \left(1/g_m\right)}$$

If g_m is large, $\boxed{A_V = \frac{-R_D}{r_S}}$

1.7 Common Drain (CD) Amplifier

It is similar to CC amplifier or emitter follower. So it is also called *source follower*.

1. $A_V < 1$.
2. No phase change.
3. Less distortion than a common source amplifier, because the source resistor is not bypassed.

$$V_0 = g_m V_{gs} R_s$$

$$V_{gs} + g_m V_{gs} R_s - V_{in} = 0$$

$$V_{in} = (1 + g_m R_s) V_{gs}$$

$$\therefore \quad \frac{V_0}{V_{in}} = \frac{g_m R_S}{1 + g_m R_S}$$

$$A_V = \frac{R_S}{R_S + \frac{1}{g_m}}$$

1.8 Common Gate Amplifier (CG)

The input |Z| of CG amplifier is low. Therefore, its application is very less.

$$Z_{in} = \frac{1}{g_m} = 500\ \Omega$$

$$V_0 = g_m V_{gs} R_D$$

$$V_{in} = V_{gs}$$

$$\frac{V_0}{V_{in}} = A_V = g_m R_D$$

$$i_{in} = i_d = g_m V_{gs}$$

$$\therefore \quad \frac{V_{gS}}{i_{in}} = \frac{1}{g_m} = Z_{in}$$

Example : 1.7

For the JFET amplifier circuit shown in Fig. 1.31, if $g_m = 2500\ \mu\mho$, and $V_{in} = 5$ mV, what is the value of V_0?

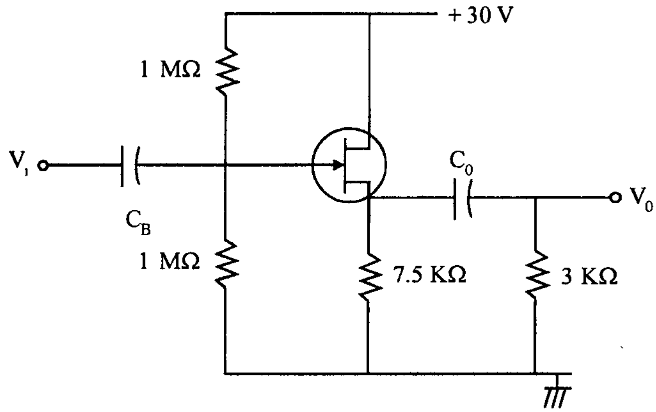


Fig. 1.31 Circuit diagram of Ex : 1.7

Solution :

$$\frac{1}{g_m} = \frac{1}{2500\ \mu} = 400\ \Omega$$

Open circuit output voltage, that is without considering R_L, = (0.949) (5mV) = 4.75 mV.

Output impedance is, $Z_0 = R_S \parallel \dfrac{1}{g_m}$

$$= 7500\ \Omega \parallel 400\ \Omega$$

$$= 380\ \Omega$$

This is the AC equivalent circuit. An AC source of 4.75 mV is in series drawn circuit with an output impedance of 380 Ω.

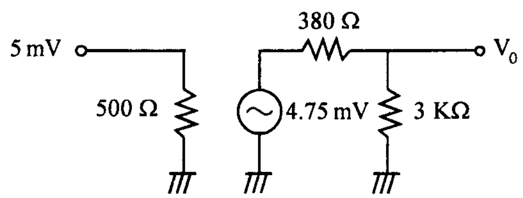


Fig. 1.32 AC Equivalent circuit

Therefore, AC voltage across the load resistor is,

$$V_0 = \frac{3000}{3380} \times 4.75 \text{ mV}$$

$$= \mathbf{4.22\ mV}$$

1.9 Gain - Bandwidth (B.W) Product

This is a measure to denote the performance of an amplifier circuit. Gain – B.W product is also referred as Figure of Merit of an amplifier. Any amplifier circuit must have large gain and large bandwidth. For certain amplifier circuits, the midband gain A_m may be large, but not Band width or Vice - Versa. Different amplifier circuits can be compared with thus parameter. The expression for Gain – B.W product of BJT.

$$A \times f_2 \simeq f_T = \frac{h_{fe}}{h_{ie}} \times \frac{1}{2\pi C_s}$$

where C_s is shunt capacitor. At $f = f_T$, $A_I = 1$. So value of gain - B.W product is f_T itself.

for high frequency amplifiers, the approximate expression for 'f_T' is,

$$f_T = \frac{g_m}{2\pi\, C_e}$$

Objective Type Questions

1. The units of h-parameters are ....
2. h-parameters are named as hybrid parameters because ....
3. The general equations governing h-parameters are

$$V_1 = \text{..............................}$$

$$I_2 = \text{..............................}$$

4. The parameter h_{re} is defined as h_{re} = ...
5. h-parameters are valid in the .... frequency range.
6. Typical values of h-parameters in Common Emitter Configuration are ....
7. The units of the parameter h_{rc} are ....
8. Conversion Efficiency of an amplifier circuit is ....
9. Expression for current gain A_I in terms of h_{fe} and h_{re} are A_I = ...
10. In Common Collector Configuration, the values of $h_{rc} \simeq$ ....
11. In the case of transistor in Common Emitter Configuration, as R_L increases, R_i ....
12. Current Gain A_I of BJT in Common Emitter Configuration is high when R_L is ....
13. Power Gain of Common Emitter Transistor amplifier is ....
14. Current Gain A_I in Common Base Configuration is ....
15. Among the three transistor amplifier configurations, large output resistance is in .... configuration.
16. Highest current gain, under identical conditions is obtained in .... transistor amplifier configuraiton.
17. C.C Configuration is also known as .... circuit.

Essay Type Questions

1. Write the general equations in terms of h-parameters for a BJT in Common Base Amplifiers configuration and define the h-parameters.
2. Convert the h-parameters in Common Base Configuration to Common Emitter Configuration, deriving the necessary equations.
3. Compare the transistor (BJT) amplifiers circuits in the three configurations with the help of h-parameters values.
4. Draw the h-parameter equivalent circuits for Transistor amplifiers in the three configurations.
5. With the help of necessary equations, discuss the variations of A_V, A_I, R_i R_O, A_P with R_S and R_L in Common Emitter Configuration.
6. Discuss the Transistor Amplifier characteristics in Common Base Configuration and their variation with R_S and R_L with the help of equations.
7. Compare the characteristics of Transistor Amplifiers in the three configurations.

Answers to Objective Questions

1. Ω, mhos and constants
2. the units of different parameters are not the same
3. $h_{11}I_1 + h_{12}V_2$
   $h_{21}I_1 + h_{22}V_2$
4. $\left.\dfrac{\partial V_B}{\partial V_C}\right|_{I_B=K}$
5. Audio
6. $h_{ie} = 1K\Omega$, $h_{re} = 1.5 \times 10^{-4}$,
   $h_{oe} = 6\mu mhos$, $h_{fe} = 200$
7. No units (constant)
8. $\dfrac{\text{AC Signal Power Delivered to the Load}}{\text{DC Input Power}} \times 100$
9. $\dfrac{h_{fe}}{1 + h_{oe}R_L}$
10. 1
11. Decreases
12. Low
13. Large
14. < 1
15. Common Base configuration
16. Common Collector
    Configuration
17. Voltatge follower/buffer

UNIT - 2

Multistage Amplifiers

In this Unit,

- Cascading of single stage amplifiers is discussed.
- Expressions for overall voltage gain are derived.
- Lower cut-off frequency, upper cut-off frequency, when n-stages are cascaded are given.
- Phase response of an amplifier, decibel voltage gain, stiff coupling terms are explained.
- Other types of transistor circuits, Darlington pair circuits, Boot strapped sweep circuit, Cascode amplifiers are also discussed.
- Numerical examples are also given.

2.1 Multistage Amplifiers Methods of Inter Stage Coupling

If the amplification obtained from a single stage amplifiers is not sufficient, two or more such amplifiers are connected in Cascade or Series i.e., the output of the first stage will be the input to the second stage. This voltage is further amplified by the second stage and so we get large amplification or large output voltage compared to the input. In the multistage amplifiers, the output of the first stage should be coupled to the input of the second stage and so on : Depending upon the type of coupling, the multistage amplifiers are classified as :

1. Resistance and Capacitance Coupled Amplifiers (RC Coupled)
2. Transformer Coupled Amplifiers
3. Direct Coupled DC Amplifiers
4. Tuned Circuit Amplifiers.

2.1.1 Resistance and Capacitance Coupled Amplifiers (RC Coupled)

This type of amplifier is very widely used. It is least expensive and has good frequency response. In the multistage resistive capacitor coupled amplifiers, the output of the first stage is coupled to the next through coupling capacitor and R_L. In two stage Resistor Capacitor coupled amplifiers, there is no separate R_L between collector and ground, but R_C, the resistance between collector and V_{CC} (R_C) itself acts as R_L in the AC equivalent circuit.

2.1.2 Transformer Coupled Amplifiers

Here the output of the amplifier is coupled to the next stage or to the load through a transformer. With this overall circuit gain will be increased $\left(\because \dfrac{N_2}{N_1} = \dfrac{V_2}{V_1}\right)$ and also impedance matching can be achieved.

But such transformer coupled amplifiers *will not have broad frequency response* i.e., $(f_2 - f_1)$ is small since inductance of the transformer windings will be large. So Transformer coupling is done for power amplifier circuits, where impedance matching is critical criterion for maximum power to be delivered to the load.

2.1.3 Direct Coupled (DC) Amplifiers

Here DC stands for direct coupled and not (direct current). In this type, there is no reactive element. L or C used to couple the output of one stage to the other. The AC output from the collector of one stage is directly given to the base of the second stage transistor directly. So type of amplifiers are used for large amplification of DC and using low frequency signals. Resistor Capacitor coupled amplifiers can not be used for amplifications of DC or low frequency signals since X_C the capacitive reactance of the coupling capacitor will be very large or open circuit for DC ($X_C = 1/2\,\pi f_C$. If $f = 0$ or low, then $X_C \to \infty$.)

2.1.4 Tuned Circuit Amplifiers

In this type there will be one RC or LC tuned circuit between collector and V_{CC}, in the place of R_C. These amplifiers will amplify signals of only fixed frequency f_0 which is equal to the resonance frequency of the tuned circuit LC. These are also used to amplify signals of a narrow band of frequencies centerd around the tuned frequency f_0.

2.1.5 Bandwidth of Amplifiers

The gain provided by an amplifier circuit is not the same for all frequencies because the reactance of the elements connected in the circuit and the device reactance value depend upon the frequency. *Bandwidth of an amplifier is the frequency range over which the amplifier stage gain is reasonably constant within $\pm$ 3 db, or 0.707 of A_V Max Value.*

Based upon the B.W. of the amplifiers, they can be classified as :

1. ***Narrow band amplifiers :*** Amplification is restricted to a narrow band of frequencies around a centre frequency.

   There are essentially tuned amplifiers.

2. ***Untuned amplifiers :*** These will have large bandwidth. Amplification is desired over a considerable range of frequency spectrum.

Untuned amplifiers are further classified w.r.t bandwidth.

1. DC amplifiers (Direct Coupled)	:	DC to few KHz
2. Audio frequency amplifiers (AF)	:	20 Hz to 20 KHz
3. Broad band amplifier	:	DC to few MHz
4. Video amplifier	:	100 Hz to few MHz

2.1.5.1 Distortion in Amplifiers

If the input signal is a sine wave the output should also be a true sine wave. But in all the cases it may not be so, which we characterize as distortion. Distortion can be due to the nonlinear characteristic of the device, due to operating point not being chosen properly, due to large signal swing of the input from the operating point or due to the reactive elements L and C in the circuit. Distortion is classified as :

(a) ***Amplitude distortion :*** This is also called non linear distortion or harmonic distortion. This type of distortion occurs in large signal amplifiers or power amplifiers. It is due to the nonlinearity of the characteristic of the device. This is due to the presence of new frequency signals which are not present in the input. If the input signal is of 10 KHz the output signal should also be 10 KHz signal. But some harmonic terms will also be present. Hence the amplitude of the signal (rms value) will be different $V_0 = A_V V_i$. But it will be V_0'.

(b) ***Frequency distortion :*** The amplification will not be the same for all frequencies. This is due to reactive component in the circuit.

(c) ***Phase - shift delay distortion :*** There will be phase shift between the input and the output and this phase shift will not be the same for all frequency signals. It also varies with the frequency of the input signal.

In the output signal, all these distortions may be present or any one may be present because of which the amplifier response will not be good.

Example : 2.1

The transistor parameters are given as,

$h_{ie} = 2$ K	$h_{fe} = 50$	$h_{re} = 6 \times 10^{-4}$	$h_{oe} = 25\ \mu A/V$
$h_{ic} = 2$ K	$h_{fc} = -51$	$h_{rc} = 1$	$h_{oc} = 25\ \mu A/V$

Find the individual as well as overall voltage gains and current gains.

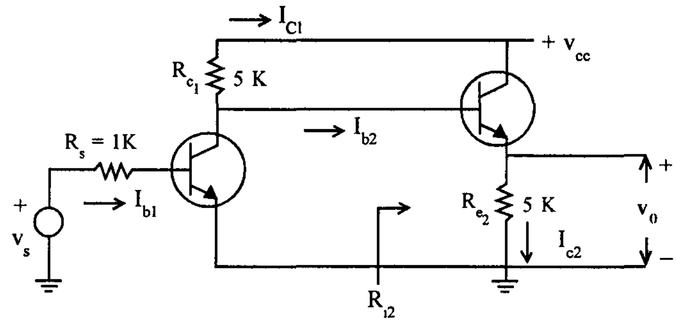


Fig. 2.1 (a) Circuit for Ex : 2.1

Solution :

It is advantageous to start the analysis with the last stage. Compute the current gain first, then the input impedance and voltage gain.

II stage : For the second stage $R_L = R_{e_2}$

$$A_{I_2} = \frac{-I_{e2}}{I_{b_2}} = \frac{-h_{fc}}{1 + h_{oc}R_{e_2}}$$

(negative (–) sign is there because for NPN transistor, I_e is negative (–) since it is leaving the transistor)

$$= \frac{51}{1 + 25 \times 10^{-6} \times 5 \times 10^3}$$

$$= \mathbf{45.3}$$

Input impedance $R_{i_2} = h_{ic} + h_{rc}\ A_{I2}\ R_{e2}$

$= 2 + 45.3 \times 5K = 228.5$ K.

$\therefore$ Input Z of the C.C. stage is very high.

Voltage gain of the second stage

$$A_{V_2} = \frac{V_0}{V_2} = A_{I_2}\frac{R_{e2}}{R_{i_2}}$$

$\because$ $V_0 = I_{e_2}\ R_{e_2}$;

V_2 = Input voltage for the second stage = $R_{i_2} \,.\, I_i$

$\therefore$
$$\frac{V_0}{V_2} = \frac{I_0 . R_{e_2}}{I_1 . R_{i_2}}$$

$$= A_{I_2}\frac{R_{e2}}{R_{i_2}}$$

$$= \frac{45.3 \times 5}{228.5} = \mathbf{0.99}$$

I stage : For the first stage, the net load resistance in the parallel combination of R_{C_1} and R_{i_2} or

$$R_{i2} = \frac{R_{c1}.R_{i2}}{R_{c1}+R_{i2}} = \frac{5\times 228.5}{233.5} = 4.9\ K\Omega$$

Hence
$$A_{I_1} = \frac{-I_{C_1}}{I_{b_1}} = \frac{-h_{fe}}{1+h_{oe}R_{L_1}} = \frac{-50}{1+25\times 10^{-6}\times 4.9\times 10^3} = -44.5$$

The input impedance of the first stage will also be the input Z of the two stages since input Z of the second stage is also considered in determining the value of R_{L_1}. R_{i_1} depends on R_{L_1}.

$\therefore$ $R_{i_1} = h_{i_e} + h_{r_e} A_{I_1} R_{L_1}$ (from the standard formula)

$$= 2 - 6 \times 10^{-4} \times 44.5 \times 4.9$$

$$R_{i_1} = 1.87\ K\Omega.$$

Voltage gain of the first stage is,

$$A_{V_1} = \frac{V_2}{V_1} = \frac{A_{I_1}.R_{L_1}}{R_{i_1}}$$

$$= \frac{-44.5\times 4.9}{1.87} = -116.6$$

$$A_I = \frac{-I_{e2}}{I_{b_1}} = \frac{-I_{e2}}{I_{b2}}.\frac{+I_{b2}}{I_{c1}}.\frac{+I_{c1}}{I_{b1}}$$

$$= -A_{I2}.\frac{I_{b2}}{I_{c1}}.A_{I_1}$$

In the actual circuit, the current gets branched into I_{c1} and I_{b2} which depend upon the values of R_{C_1} and R_{i_2}

$\because$ $(-I_{b2} + I_{c1})\, R_{c1} = I_{b2} \cdot R_{i2}$

$\therefore$ $+ I_{b2}\,(R_{i2} + R_{c1}) = I_{c1} \cdot R_{c1}$

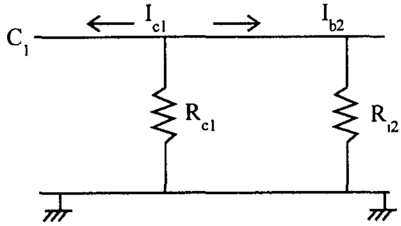


Fig. 2.1 (b) Current branching

$$\frac{I_{b2}}{I_{c1}} = \frac{R_{c1}}{R_{c1}+R_{i2}}$$

$$\therefore \qquad A_I = A_{I2}\,A_{I1}\cdot\frac{R_{c1}}{R_{i2}+R_{c_1}}$$

$$= \frac{45.3\times(-44.5)\times 5}{228.5+5}$$

$$A_I = -43.2$$

$$A_V = \frac{V_0}{V_1} = \frac{V_0}{V_2}\cdot\frac{V_2}{V_1} = A_{V2}\cdot A_{V1}$$

$$A_V = 0.99 \times (-116.6) = -115.$$

2.1.6 R - C Coupled Amplifier Circuit (Single Stage)

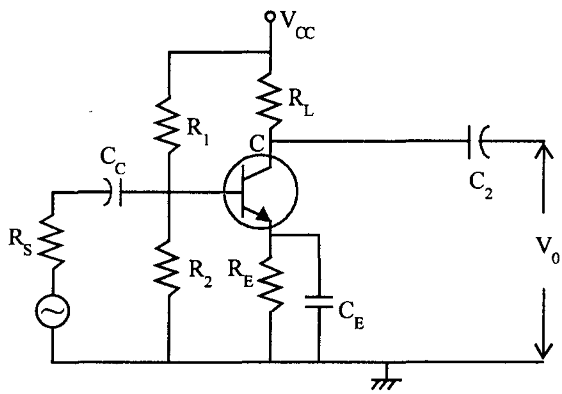


Fig. 2.2 RC Coupled amplifier circuit

R_L is the load resistor that develops the output voltage from the transistor. C_2 is used to couple the AC component of the output to R_L.

In the self bias circuit, R_E the emitter resistors is connected between emitter and ground. But through R_E, a negative feedback path is there. So to prevent A.C. negative feedback, if a capacitor is connected in parallel with R_E, and it is chosen such that X_E provides least resistance path compared to R_E, AC signal passes through C_E and not through R_E. Therefore, there will not be any negative feedback for AC signals.

$$X_E \text{ is chosen such that } X_E \leq \frac{R_E}{10}$$

and X_E is chosen at the frequency f_1. For frequencies higher than f_1, X_E any way will be less.

The equivalent circuit for the above transistor configuration is,

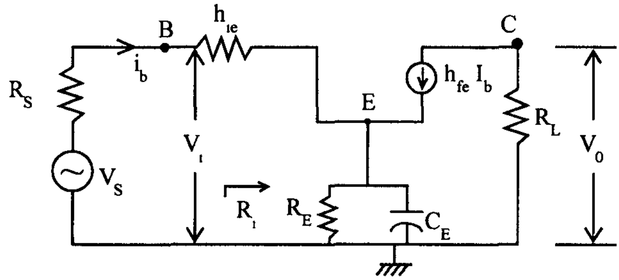


Fig. 2.3 Equivalent circuit

Suppose the value of C_C is very large. Then at the low and medium frequencies, the impedance is negligible. So the *equivalent* circuit is as shown. We shall consider the effect of C_E later.

From the *equivalent* circuit,

$$V_0 = -h_{fe}.\ i_b.\ R_L$$

negative sign is used since it is NPN transistor. The collector current is flowing into the transistor.

Input current, $\quad I_b = V_s / R_s + R_i$

For a transistor amplifier circuit in common emitter configuration,

$$R_i = h_{ie} + (1 + h_{fe})\ Z_E.$$

Where $\quad Z_E = R_E$ in parallel with $C_E = \dfrac{R_E}{1 + j\omega C_E R_E}$

$$\therefore \quad V_0 = -h_{fe}.\ R_L \times \frac{V_S}{R_S + h_{ie} + \dfrac{(1+h_{fe})R_E}{1 + j\omega C_E R_E}}$$

$$\therefore \quad A_V = \frac{V_0}{V_S}$$

A_V at low frequencies, (LF)

$$A_V\,(LF) = \frac{V_0}{V_S}$$

$$\boxed{A_V\,(LF) = \frac{-h_{fe}.\ R_L}{R_S + h_{ie} + \dfrac{(1+h_{fe})R_E}{1 + j\omega\, C_E R_E}}}$$

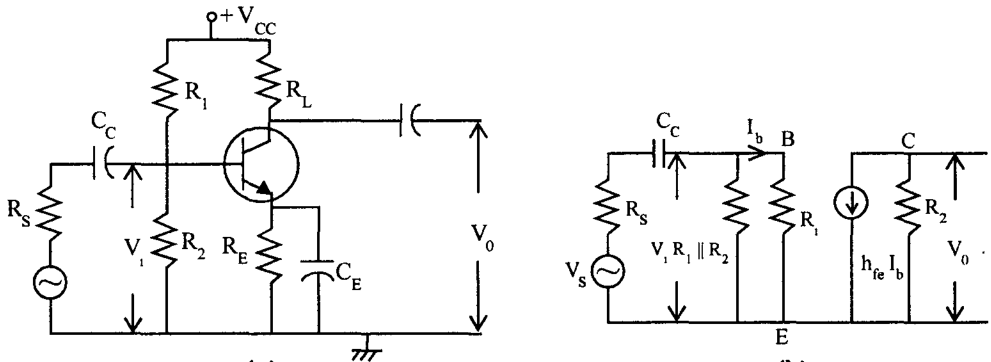
When ω is large, $\dfrac{(1+h_{fe})R_E}{1 + j\omega\, C_E R_E}$ can be neglected. So in the Mid Frequency range, (M.F.),

$$\therefore \quad \boxed{A_V\,(M.F) = \frac{-h_{fe} R_L}{R_S + h_{ie}}}$$

In this expression, there is no f or ω term. Hence in the mid frequency range, A_V is independent of f or the gain remains constant, irrespective of change in frequency.

2.1.7 Effect of Coupling Capacitor on Low Frequency Response

Suppose that the value of C_E is such that its effect on the frequency response can be neglected and



(a) (b)

Fig. 2.4 Effect of coupling capacitors

the value of X_C at low frequencies is such that it is not a simple short circuit for A.C. signals, so that its effect has to be considered.

The effect of C_E is, voltage drop across C_C will reduce V_i with a corresponding drop in V_0.

The frequency at which the gain drops by a factor of $\frac{1}{\sqrt{2}}$, is the lower 3 db frequency.

$$f_1 = \frac{1}{2\pi(R_S + R_1')C_C}$$

where $R_i' = R_1 \parallel R_2 \parallel R_i$

and $R_i = h_{ie}$, for an ideal capacitor C_E.

These expressions are valid when emitter is bypassed. In AC *equivalent circuit, emitter is assumed to be at GND potential. Therefore C_E has no effect.*

Large values of capacitors are required (10μF, 5μF etc.) in transistor amplifiers for coupling and bypass purposes for good low frequency response. Since these values are large, only electrolytic capacitors are used. Capacitors of such large values are not available in other types of capacitors. These capacitors are bulky. So audio amplifier circuits, Integrated Circuits (I.C) often have large capacitors connected externally to the (I.C) itself to provide the required low frequency response.

Example : 2.2

In the Resistance Capacitance (RC) coupled amplifier, $A_{v_m} = 50$, $f_1 = 50$ Hz and $f_2 = 100$ K Hz. Find the values of frequencies at which the gain reduces to 40 on either side of midband region.

Solution :

$$A_{VH} = \frac{A_{V\,MF}}{1 + j\left(\frac{f}{f_2}\right)}$$

Phase shift angle $\quad \phi = 180^\circ - \tan^{-1}\left(\frac{f}{f_2}\right)$

$$A_{V\,LF} = \frac{A_{V\,MF}}{\sqrt{1 + \left(\frac{f_1}{f}\right)^2}}$$

$$A_{VL} = \frac{A_{V\,M}}{1 + j\left(\frac{f_1}{f}\right)}$$

$$\phi = 180^\circ + \tan^{-1}\left(\frac{f_1}{f}\right)$$

At the frequency f, the gain is $A_{V\,L.F} = 40$.

$A_{VL.F} = 40, \quad A_{VM..F} = 50, \quad f_1 = 50$ Hzs, $f = ?$

$$\frac{40}{50} = \frac{1}{\sqrt{1 + \left(\frac{50}{f}\right)^2}} \qquad \therefore\ f = 66.66 \text{ Hz.}$$

$$A_{V\,H.F} = \frac{A_{V\,M.F}}{\sqrt{1 + \left(\frac{f}{f_2}\right)^2}}$$

At frequency f, $\quad A_{V\,H.F} = 40. \quad \therefore \quad f = ? \qquad f_2 = 100$ KHz.

$$\frac{40}{50} = \frac{1}{\sqrt{1 + \left(\frac{f}{100 \times 10^3}\right)^2}}; \qquad f = 75 \text{ KHz.}$$

Example : 2.3

An amplifier of 40db gain has both its input and output load resistances equal to 600Ω. If the amplifier input power is – 30db, what is the output power and voltage ? Assume that reference power level used is 1mW in a 600 Ω resistance.

Solution :

Since it is logarithmic scale, for dbs,

$$P_0\ (db) = (P_i)_{db} + (gain\ _{db});$$

$$P_0 = P_i \times A_P \quad \text{Output power } (P_0) = \text{Input Power } (P_i) \times \text{Power Gain } (A_P)$$

$$P_0 = ?\ P_i = -30db,\ gain = 40db$$

$$\therefore \quad P_0 = -30 + 40 = \mathbf{10db.}$$

Reference power level = 1mW.

$$\therefore \quad 10 \log = \left(\frac{P_0}{1mW}\right) = 10db$$

$$10 \log \frac{P_0}{0.001} = 10$$

$$\log \frac{P_0}{0.001} = 1$$

$$\frac{P_0}{0.001} = 10$$

$$\because \quad \log 10 = 1$$

$$\therefore \quad P_0 = 10 \times 0.001$$

$$= \mathbf{10mW}$$

(With respect to, 1mW, the input and output powers are compared and expressed in db)

$$\therefore \quad 10 \log \frac{P_0}{1mW} = 10db)$$

RMS output voltage is,

$$P_0 = \frac{V_0^2}{R}$$

or

$$V_0 = \sqrt{P_0.R} = \sqrt{10 \times 10^{-3} \times 600}$$

$$= \sqrt{6} = \mathbf{2.45\ V}$$

Example : 2.4

An amplifier has $R_i = 0.5K\Omega$ and $R_0 = 0.05K\Omega$. The amplifier gives an output voltage of 1V peak for an input voltage of 1mV peak. Find A_V, A_i, A_P in db.

Solution :

$$V_0 \text{ (peak)} = 1V.$$

$$V_{0\,(rms)} = \frac{V_0(\text{peak})}{\sqrt{2}}; \qquad V_{0\,(rms)} = \frac{1V}{\sqrt{2}}$$

$$A_V = 20 \log \left(\frac{V_0}{V_i}\right)$$

$$= 20 \log \left(\frac{1}{1mV}\right) = 60 \text{ db}$$

$$I_{i\,(peak)} = V_{i\,(Peak)} / R_i$$
$$= 1mV/500$$
$$= 2 \times 10^{-6} A.$$

$$I_{0\,(peak)} = V_{0\,(Peak)} / R_0$$
$$= 1/50$$
$$I_{0\,(Peak)} = 0.02 \ A.$$

$$\therefore \text{ Current Gain } (A_i) = 20 \log \left(\frac{0.02}{2\times10^{-6}}\right) = \mathbf{80\ db}$$

$$P_i = \frac{V_i^2}{R_i} = 10^{-9} W;$$

$$P_0 = \frac{V_0^2}{R_0} = 10^{-2} W.$$

$$\text{Power gain,} \quad A_P = 10 \log \left(\frac{P_0}{P_i}\right) = \mathbf{70\ db}$$

2.2 n - Stage Cascaded Amplifier

2.2.1 Overall Voltage Gain

The resultant voltage gain is given by the product of the individual voltage gains of each stage.

$$A_{V_1} = \frac{V_2}{V_1} = A_1 \angle \theta_1$$

$A_1 =$ Magnitude of the voltage gain of the first stage and θ_1 is the phase angle between output and input voltage of this stage

$$\frac{V_0}{V_1} = \frac{V_2}{V_1} \cdot \frac{V_3}{V_2} \cdot \frac{V_4}{V_3} \cdots \frac{V_n}{V_{n-1}} \cdot \frac{V_o}{V_n}$$

$$A_V = A_{V1} A_{V2} \ldots A_{Vn}$$

$$= A_{V1} \angle\theta_1 \cdot A_{V2} \angle\theta_2 \cdot A_{V3} \angle\theta_3 \ldots\ldots A_{Vn} \angle\theta_n$$

$$= A_{V1} A_{V2} \ldots\ldots A_{Vn} \angle\theta_1 + \angle\theta_2 + \angle\theta_3 \ldots\ldots \angle\theta_n$$

$$= A_V \angle\theta. \quad [\text{Since } A_V = A_{V1} A_{V2} A_{V3} \ldots A_{Vn} \text{ and } \theta = \theta_1 + \theta_2 + \ldots + \theta_n]$$

2.2.2 Current Gain

$$A_I = \frac{I_O}{I_{b1}}$$

It is the ratio of the output current I_0 of the last stage to the input current or base current I_{b_1} of the first stage.

$$A_I = \frac{I_O}{I_{b1}} = \frac{-I_{cn}}{I_{b1}}$$

Where I_{cn} is equal to the collector current of the n^{th} stage transistor.

$$\frac{I_n}{I_{b1}} = \frac{I_1}{I_{b1}} \cdot \frac{I_2}{I_1} \ldots\ldots \frac{I_n}{I_{n-1}}$$

$$= A'_{I_1} \; A'_{I_2} \ldots\ldots A'_{I_n}$$

A_{I_1} = The base to collector current gain of the first stage

A'_{I_n} = Base collector current gain of the n^{th} stage

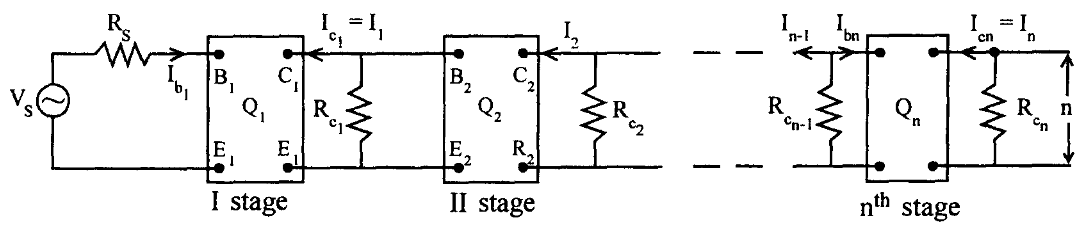


Fig. 2.5 Multistage amplifiers

2.2.3 Power Gain

$$A_P = \frac{\text{Output power}}{\text{Input power}} = \frac{-V_0 I_n}{V_1 I_{b1}} = A_V \cdot A_I$$

But $$A_V = \frac{I_n \cdot R_{cn}(R_0)}{I_{b1} \cdot R_{i1}}$$

$$A_V = \frac{\text{Output Voltage}}{\text{Input Voltage}}$$

But $I_n/I_{b1} = A_I$

$$\therefore \quad A_V = A_I = \frac{R_{cn}(R_0)}{R_{i1}}$$

R_{cn} = Collector Ressistance of n^{th} stage transistor
R_{i1} = Input resistance of I stage amplifier

$$\therefore \quad A_P = (A_I)^2 \cdot \frac{R_{cn}}{R_{i1}}$$

2.2.4 Choice of Transistor in a Cascaded Amplifier Configuration

By connecting transistor in cascade, voltage gain gets multiplied. But what type of configuration should be used ? Common Collector (CC) or Common Base (CB) or Common Emitter (CE)? To get voltage amplification and current amplification, only Common Emitter (CE) configuration is used. Because for Common Collector, the voltage gain is less than 1 for each stage. So the overall amplification is less than 1.

Common Base Configuration is also not used since A_I is less than 1.

$$\therefore \quad A_V = A_I \times \frac{R_L}{R_i}$$

Effective load resistance R_L is parallel combination of R_C and R_i of the following stage, (next stage) (since in multi stage connection, the output of one stage is the input to the other stage). This parallel combination is less than R_i. Therefore, $\frac{R_L}{R_i} < 1$.

The current gain A_I in common base configuration is $h_{fb} < 1$ or $\cong 1$.

Therefore overall voltage gain $\cong$ 1. Therefore Common Base configuration is not used for cascading.

So only Common Emitter configuration is used. ($h_{fe} >> 1$)

Therefore overall voltage gain and current gains are >1 in Common Emitter configuration. For a single stage Resistor Capacitor coupled amplifier, bandwidth is $(f_2 - f_1) \cong f_2$. f_1 is very small compared to f_2. f_2 is usually of the order of KHz or MHz. f_1 is of the order of few HZ.

$$A_H = \frac{A_M}{\sqrt{1+\left(\frac{f}{f_2}\right)^2}}$$

$$\left(\frac{A_H}{A_M}\right)^n = \left\{\frac{1}{\sqrt{1+\left(\frac{f}{f_2}\right)^2}}\right\}^n$$

$$\therefore \qquad \frac{1}{\sqrt{2}} = \left\{\frac{1}{\sqrt{1+\left(\frac{f_{2n}}{f_2}\right)^2}}\right\}^n$$

If f_{2n} is the upper 3 db frequency

$$\left(\frac{A_H}{A_M}\right)^n = \left(\frac{1}{\sqrt{2}}\right) \quad \text{for } f = f_{2n}$$

f_2 is the frequency at which

$$A_H = \frac{A_M}{\sqrt{2}},$$

When n stages of RC coupled amplifiers are connected in cascade, the upper 3db frequency $(f_2)^n$ for which the overall voltage gain falls to $\frac{1}{\sqrt{2}}$ of its midband value is,

$$\left\{\frac{1}{\sqrt{1+\left(\frac{f_{2n}}{f_2}\right)^2}}\right\}^n = \frac{1}{\sqrt{2}}$$

or $$\left\{\sqrt{1+\left(\frac{f_{2n}}{f_2}\right)^2}\right\}^n = \sqrt{2}$$

$$\left\{1+\left(\frac{f_{2n}}{f_2}\right)^2\right\}^n = 2$$

$$1+\left(\frac{f_{2n}}{f_2}\right)^2 = (2)^{\frac{1}{n}}$$

$$\left(\frac{f_{2n}}{f_2}\right)^2 = \left[(2)^{\frac{1}{n}} - 1\right]$$

$\therefore$ $$\frac{f_{2n}}{f_2} = \sqrt{2^{1/n} - 1}$$

$$A_L = \frac{A_M}{\sqrt{1+\left(\frac{f_1}{f}\right)^2}}.$$

$$\left(\frac{A_L}{A_M}\right)^n = \left\{\frac{1}{\sqrt{1+\left(\frac{f_1}{f}\right)^2}}\right\}$$

If $f = f_{1n}$,

then $$\left(\frac{A_L}{A_M}\right)^n = \frac{1}{\sqrt{2}}$$

$$\therefore \qquad \frac{1}{\sqrt{2}} = \left\{\frac{1}{\sqrt{1+\left(\frac{f_1}{f_{1n}}\right)^2}}\right\}$$

When n stages are connected in cascade, the lower cut off frequency for nth stage is, $\left(\frac{A_L}{A_M}\right)^n = \frac{1}{\sqrt{2}}$.

$$\left\{\frac{1}{\sqrt{1+\left(\frac{f_1}{f_{1n}}\right)^2}}\right\}^n = \frac{1}{\sqrt{2}}$$

or $$\left[1+\left(\frac{f_1}{f_{1_n}}\right)^2\right]^{n/2} = \sqrt{2}$$

or $$1+\left(\frac{f_1}{f_{1_n}}\right)^2 = 2^{1/n}$$

$$\frac{f_1}{f_{1_n}} = \sqrt{2^{1/n}-1}$$

or $$f_{1_n} = f_1 \Big/ \sqrt{2^{1/n}-1}$$

2.2.5 Midband frequency f_0

It is the geometric mean of the lower cut off frequency f_1 and upper cut off frequency f_2. It lies in the middle of the mid frequency range and has maximum gain. $f_0 = \sqrt{f_1 f_2}$.

f_β and f_T are the frequency constants of a Transistor in Common Emitter configuration.

For a Transistor in Common Emitter configuration, the plot of A_i V_S R_L is as shown Fig. 2.6. Short circuit current gain of Common Emitter Transistor varies with frequency. Short circuit current gain of transistor varies with frequency.

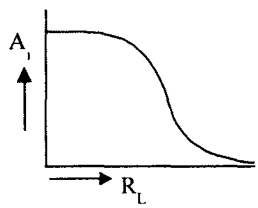


Fig. 2.6 Variation of A_i with R_L

The frequency f_β ; It is the frequency at which short circuit current gain of the Transistor falls to $\frac{1}{\sqrt{2}}$ of its maximum value. This is called as the Bandwidth of the transistor.

$$\boxed{h_{fe} \cdot f_\beta = f_T}$$

2.2.6 Cascading Transistor Amplifiers

When the amplification of a single transistor is not sufficient for a particular purpose (say to deliver output to the speaker or to drive a transducer etc) or when the input or output impedance is not of the correct magnitude for the desired application, two or more stages may be connected in cascade. Cascade means in series i.e. The output of first stage is connected to the input of the next stage.

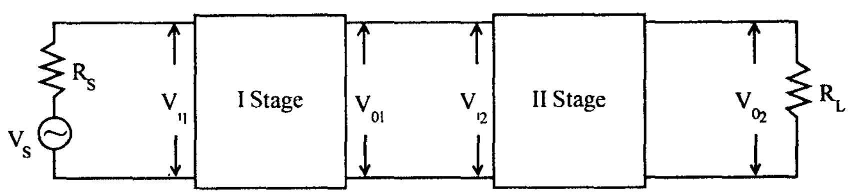


Fig. 2.7 Cascaded amplifier stages

Let us consider two stage cascaded amplifier. Let the first stage is in common emitter configuration. Current gain is high and let the II stage is in common collector configuration to provide high input impedance and low output impedance. So what are the expressions for the total current gain A_I of the entire circuit (i.e. the two stages), Zi, A_V and Y_0 ? To get these expressions, we must take the h-parameters of these transistors in that particular configuration. Generally manufactures specify the h-parameters for a given transistor in common emitter configuration. It is widely used circuit and also A_I is high. To get the transistor h-parameters in other configurations, conversion formulae are used.

2.2.7 The Two Stage Cascaded Amplifier Circuit

The Transistor Q_1 is in Common Emitter configuration (Fig. 2.8). The second Transistor Q_2 is in Common Collector (CC) configuration. Output is taken across 5K, the emitter resistance. Collector is at ground potential in the A.C. equivalent circuit.

Biasing resistors are not shown since their purpose in only to provide the proper operating point and they do not affect the response of the amplifier. In the low frequency equivalent circuit, since the capacitors have large value, and so is X_C low, and can be neglected. So the capacitive reactance is not considered, and capacitive reactance $X_c = \dfrac{1}{2\pi f C}$ is low when C is large and taken as short circuit.

The small signal Common Emitter configuration circuit reduces as shown in Fig 2.8.

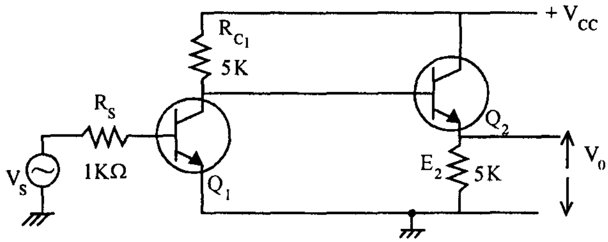


Fig. 2.8 Two stage cascaded amplifier circuit

In this circuit Q_2 collector is at ground potential, in AC equivalent circuit. It is in Common Collector configuration and the output is taken between emitter point E_2 and ground. So the circuit is redrawn as shown in Fig. 2.9 (a) indicating voltages at different stages and input and output resistances.

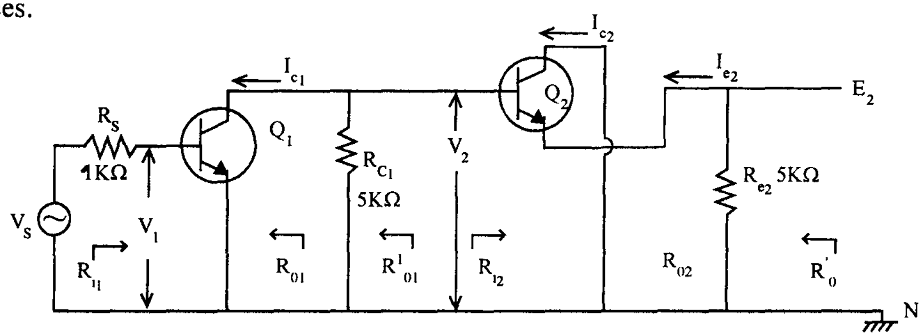


Fig. 2.9 (a) Redrawn circuit

2.2.8 Phase Response

Since the transistor is in Common Emitter configuration, there will be a phase shift of 180° between input and output.

But in the L.F. range, $\theta = +\tan^{-1}\left(\frac{f_1}{f}\right)$

When $f = f_1$, $\theta = +\tan^{-1}(1) = 45^0$. As f, increases, θ decreases.

$\therefore$ Total phase difference in the L.F. range is, +180°. Phase shift due to Common Emitter configuration $\theta = +\tan^{-1}\left(\frac{f_1}{f}\right)$

This phase lead decreases as frequency increases.

In the high frequency range $\theta = \tan^{-1}\left(\frac{f}{f_2}\right)$. When $f = f_2$, $\theta = \tan^{-1} 1 = 45°$

As f increases, θ decreases. Therefore Phase lag decreases

In the low frequency range, the signal is leading. Since θ is positive and +180°

$$\text{Total Phase angle} = +180° + \theta;\ \phi = 180° + \tan^{-1}\left(\frac{f_1}{f}\right)$$

In the high frequency range the signal is lagging. Therefore $+180° - \theta$;

$$\phi = 180° - \tan^{-1}\left(\frac{f}{f_2}\right)$$

Phase Response : 180°, because, Common Emitter configuration introduces 180° phase shift.

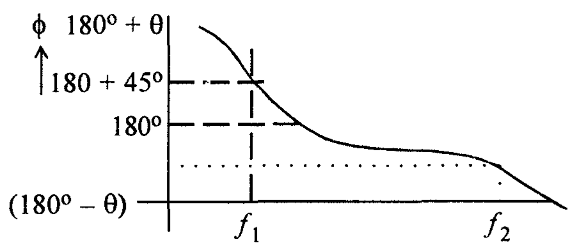


Fig. 2.9 (b) Variation of phase angle with frequency

In the low frequency range, Phase shift $\phi = (180^o + \theta)$
In the high frequency range, Phase shift $\phi = (180^o - \theta)$

2.2.9 Gain - Bandwidth Product

$$A_{MF} = \frac{-h_{fe}}{h_{ie}}\left(\frac{R_C R_L}{R_C + R_L}\right)$$

$$\text{Bandwidth} = f_2 - f_1 \simeq f_2 \quad \because \quad f_1 << f_2$$

$$f_2 = \frac{1}{2\pi C_S \cdot \left(\frac{R_C . R_L}{R_C + R_L}\right)}$$

$\therefore$ The product of these two, (A_{MF} and BW) is,

$$A \times f_2 = f_T = \frac{-h_{fe}}{h_{ie}} \times \frac{1}{2\pi C_S} = f_T$$

For a given value of C_S, this product is constant.

We can increase the voltage gain by increasing R_C, R_L parallel combination. But $f_2 \propto \frac{1}{R_C \parallel R_L}$. Therefore f_2 will reduce if A_{MF} is increased. *Therefore if voltage gain increases, Bandwidth decreases and vice versa.*

f_2 can be increased without affecting voltage gain by reducing the value of C_S - But there is a limit to which C_S can be reduced. If higher gain is required then Bandwidth has to be scarificed. It (B.W) will reduce.

The product of midband gain and Bandwidth is also known as the figure of Merit of the circuit.

Example : 2.5

If β = 150, what are the cutoff frequencies of the input and output lead networks of the given circuit ?

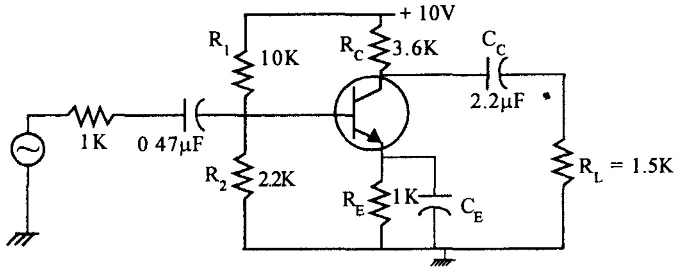


Fig. 2.10 Circuit for Ex : 2.5

Solution

When β value is given, and not h_{ie} of the transistor, the input impedance of the transistor can be determined.

$$Z_{in} = \frac{V_{in}}{i_b}$$

$$V_{in} = i_e r_e' \qquad i_e \simeq i_C \simeq \beta\, i_b$$

$$\therefore \quad V_{in} \simeq \beta\, i_b . r_e'$$

$$\therefore \quad Z_{in} = \frac{\beta i_b . r_e'}{i_b} = \beta r_e'$$

$$R_{in} = R_1 \parallel R_2 \parallel \beta_{re}'$$

$$\beta_{re}' = 150 \times 22.7 = 3.14\ K\Omega$$

$$R_{in} = 10K \parallel 2.2K \parallel 3.14\ K = 1.18K\Omega$$

$$f_{in} = \frac{1}{2\pi(R_S + R_{in})C_{in}}$$

Cutoff frequencies of input network (HPF)

$$f_0 = \frac{1}{2\pi(R_0 + R_L)C_0}$$

$$f_{in} = \frac{1}{2\pi(1K\Omega + 1.18K\Omega)(0.47\mu F)}$$
$$= 155Hzs.$$

$$f_0 = \frac{1}{2\pi(3.6K + 1.5K\Omega)(2.2\mu F)}$$
$$= 14.2\ Hzs$$

LPF Cutoff frequency of output network.

2.2.10 Emitter Bypass Capacitor

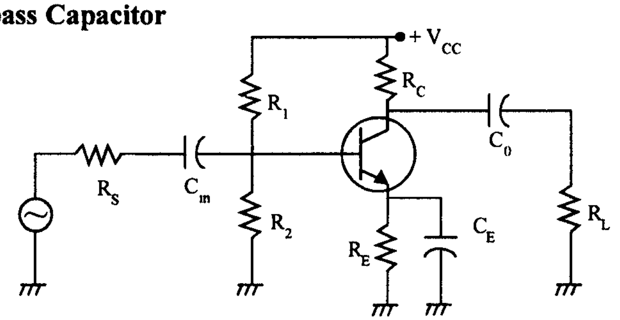


Fig. 2.11 CE Amplifier circuit

C_E is the emitter bypass capacitor. This causes the frequency response of an amplifier to break at a cutoff frequency, designated f_E. To understand the effects of emitter bypass capacitor, suppose, C_{in} and C_0 (coupling capacitor) are shorted, then the frequency response will be, as shown in Fig. 2.12(a).

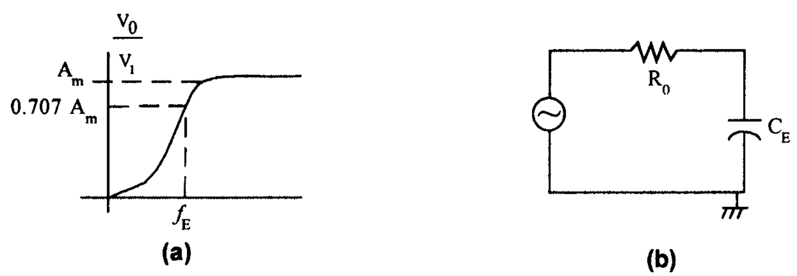


Fig. 2.12 Effect of emitter by pass capacitor

This means that frequency response breaks at f_E. Thevenin's equivalent resistance driving Common Emitter, R_{out} is the Thevenin's resistance facing the capacitor.

$$\therefore \qquad R_{out} \simeq r_e' + \frac{R_S \| R_1 \| R_2}{\beta}$$

$$[i_e r_e' + i_e R_E - V_{in} + i_b (R_S \| R_1 \| R_2)] = 0$$

$$\because i_b = i_c/\beta, \ \cong i_e/\beta,$$

Solving for i_e, $$i_e \simeq \frac{V_{in}}{R_E + r_e' + (R_s \| R_1 \| R_2)/\beta}$$

The emitter resistor R_E is driven by an AC source with an AC output resistance of

$$Z_O\,(\text{emitter}) = r_e' + \frac{R_s \| R_1 \| R_2}{\beta}$$

2.3 Equivalent Circuits

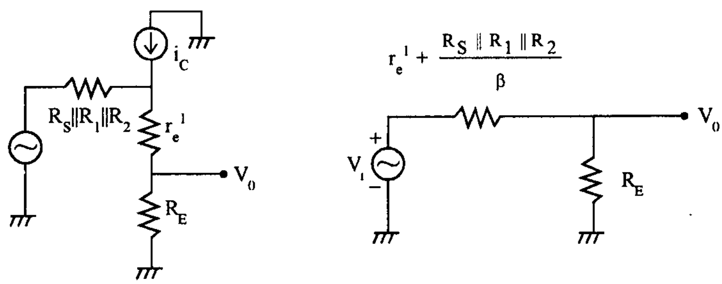


Fig. 2.13 Equivalent circuits

$$\therefore \qquad f_E = \frac{1}{2\pi R_{out} C_E}$$

f_E = Cutoff frequency of emitter network.
R_{out} = Output resistance facing bypass capacitor.
C_E = Emitter bypass capacitance.

2.3.1 Decibel

n many cases it is convenient to compare two powers on a logarithemic scale rather than on a linear scale. The unit of this logarithemic scale is called the decibel abbreviated as db.

Suppose P_2 is the output power and P_1 is the input power, then the power gain in decibels is

$$N = 10 \log_{10} \frac{P_2}{P_1}$$

Where N is in dbs

If N is negative, it means P_2 is less than P_1.

Noise power is also expressed in decibels (dbs). It should be negative for a given device or amplifier i.e the output noise is less than what is present in the input.

If for a given amplifier circuit, the input and output resistances are same (as R), then

$$P_1 = \frac{V_1^2}{R}, \quad P_2 = \frac{V_2^2}{R} \text{ where } V_1 \text{ and } V_2 \text{ are input and output voltages.}$$

$$\therefore \qquad N = 20 \log \frac{V_2}{V_1} = 20 \log A_V$$

But even though, the input and output impedances are not equal, this convention is followed for convenience i.e, $N = 20 \log A_V$. If $A_V = 10$, $N = 20 \log 10$ is 20 the decibel voltage gain of the amplifier. 20 is not the power gain because, the input resistances are not equal. Therefore 20 is the decibel voltage gain. If the output resistances are equal decibel voltage gain is equal, to power gain. Overall db V of a multistage amplifier is equal to sum of db V of individual stages.

2.4 Miller's Theorem

Fig. 2.14(a) shows an amplifier with a capacitor between input and output terminals. It is called as feedback capacitor. When the gain K is large, the feedback will change the input Z and output Z of the circuit.

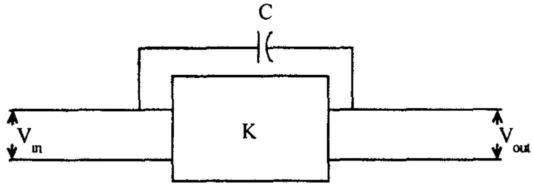


Fig. 2.14 (a) Feedback capacitor

A circuit as shown above is difficult to analyze, because of capacitor. So according to the Miller's theorem, the feedback capacitor can be split into two values, one as connected in the input side and the other on the output side, as shown in Fig. 2.14 (b).

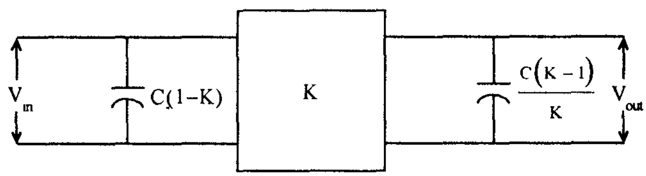


Fig. 2.14 (b) Splitting of feedback capacitor using Miller's Theorem.

2.4.1 Mathematical Proof of Miller's Theorem

The AC current passing through capacitor (C) in Fig. 2.14 (a) is

$$I_C = \frac{V_{in} - V_{out}}{\left(\frac{1}{j\omega c}\right)} = \frac{(V_{in} - V_{out})}{-J\, X_C}$$

$$V_{out} = K\, V_{in}$$

$$\therefore \qquad I_C = \frac{(V_{in} - KV_{in})}{-jX_C} = \frac{V_{in}(1-K)}{-jX_C}$$

$$\frac{V_{in}}{I_C} = Z_{in} = \frac{V_{in}}{\frac{V_{in}(1-K)}{-jX_C}} = \frac{-jX_C}{(1-K)}$$

$$= \frac{-j}{2\pi f C(1-K)}$$

Since $\quad X_C = \dfrac{1}{2\pi f C}$

$\dfrac{V_{in}}{I_C}$ is the input Z as seen from the input terminals.

$$\therefore \qquad Z_{in} = \frac{-j}{2\pi f[C(1-K)]}$$

$$\therefore \qquad C_{in} = C\,(1-K)$$

Similarly output capacitance can be derived as follows :

Current in the capacitor,

$$I_C = \frac{V_{out} - V_{in}}{-jX_C} = \frac{V_{out}\left(1 - \frac{V_{in}}{V_{out}}\right)}{-jX_C}$$

$$I_C = \frac{V_{out}\left(1 - \frac{1}{K}\right)}{-jX_C}$$

$$= \frac{V_{out}}{I_C} = Z_{out}$$

$$= \frac{V_{out}}{\frac{V_{out}\left(1 - \frac{1}{K}\right)}{-jX_C}}$$

$$Z_{out} = \frac{-jX_C}{\left(\frac{A-1}{A}\right)} = \frac{-j}{2\pi f C\left(\frac{K-1}{K}\right)}$$

$$\therefore \qquad C_{out}\,(\text{Miller}) = C\left(\frac{K-1}{K}\right)$$

2.5 Frequency Effects

2.5.1 Lead Network

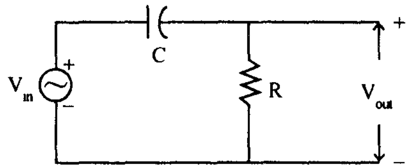


Fig. 2.15 Lead Network

$$I = \frac{V_{in}}{R + \frac{1}{j\omega C}}$$

$$V_0 = I.\, R = \frac{V_{in}.R}{\left(R + \frac{1}{j\omega C}\right)}$$

V_0 leads with respect to V_{in}. So it is called as *lead network* for the above circuit, at low frequencies, $X_C = \infty$.

$\therefore$ V_0 is low since (I is low). As f increases X_c decreases. Hence I flows, and V_o increases.

$\therefore$ Gain increases. Hence the frequency response is as shown.

2.5.2 Cut-off Frequency

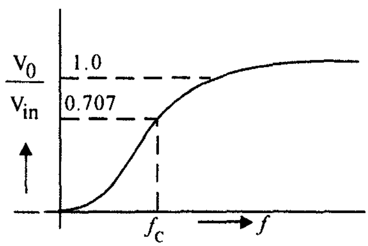


Fig. 2.16 Frequency response

$$V_{out} = \frac{R}{\sqrt{R^2 + X_C{}^2}}.V_{in}$$

$$\frac{V_{out}}{V_{in}} = \frac{R}{\sqrt{R^2 + X_C^2}}$$

Cut-off frequency is the frequency at which $\frac{V_{out}}{V_{in}} = \frac{1}{\sqrt{2}}$.

This happens when, $X_c = R$

$$\frac{1}{2\pi f_c C} = R \quad \text{or} \quad \boxed{f_C = \frac{1}{2\pi RC}}$$

Lower cut-off frequency.

2.5.3 Half Power Point

At $\quad f = f_C, \quad P = \dfrac{V_{out}^2}{2R}$

Power is half of maximum power when V_{out} is maximum. Therefore it is also called as half power point.

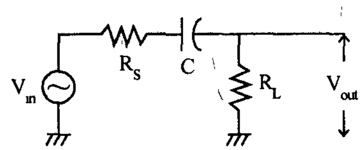


Fig. 2.17 Equivalent circuit

Considering Source Resistance :

$$\frac{V_{out}}{V_{in}} = \frac{R}{\sqrt{(R_S + R_L) + X_c^2}}$$

$$\text{At } f_C, \quad R_S + R_L = X_C$$

$$\therefore \quad f_C = \frac{1}{2\pi(R_S + R_L).C}$$

In the midband frequency region $X_C \cong 0$.

$$\therefore \quad \frac{V_{out}}{V_{in}} = \frac{R_L}{R_S + R_L}$$

$$A_{mid} \text{ (midband voltage gain)} = \frac{R_L}{R_S + R_L}$$

2.5.4 Stiff Coupling

If $X_c = 0.1\ (R_S + R_L)$ it is called *Stiff Coupling.*

The coupling capacitor must have (or bypass capacitor).

$$X_c = \frac{1}{10} R_E$$

This is known as *Stiff Coupling.*

2.6 Amplifier Analysis

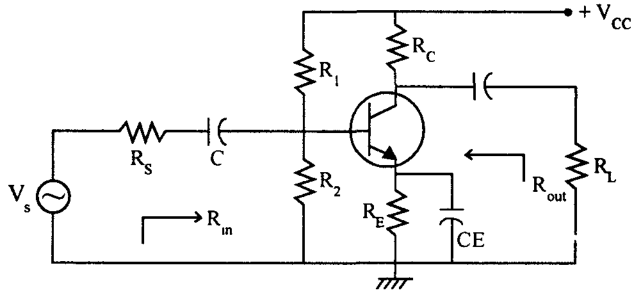


Fig. 2.18 Amplifier circuit

The equivalent circuit from input side, not considering R_S.
The equivalent circuit from output side, not considering R_L.

$$R_{in} = R_1 \parallel R_2 \parallel \beta r_e' \quad \text{(Not cosidering } R_S\text{)}$$
$$R_{out} \cong R_C \text{ (Not cosidering } R_L\text{)}$$

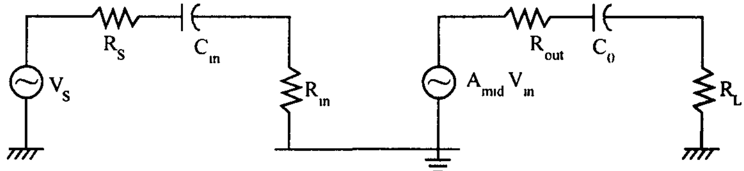


Fig. 2.19 Equivalent circuit

Considering the input side as a load network,

$$f_{in} = \frac{1}{2\pi(R_S + R_{in})C_{in}}$$

Similarly output lead network has cut-off frequency

$$f_{out} = \frac{1}{2\pi(R_{out} + R_L)C_{out}}$$

2.6.1 Lag Networks

$$V_0 = I.\ X_c$$
$$= \frac{V_i\ .\ X_C}{\left(R + \frac{1}{j\omega C}\right)}$$
$$V_0 = \frac{\frac{1}{j\omega C}.V_{in}}{\sqrt{R^2 + X_C{}^2}}$$
$$V_0 = \frac{-j(V_i / \omega C)}{\sqrt{R^2 + X_C^2}} \text{ therefore it is lag network}$$

V_0 lags with respect to V_i.

$$\frac{V_{out}}{V_{in}} = \frac{X_c}{\sqrt{R^2 + X_c^2}}$$

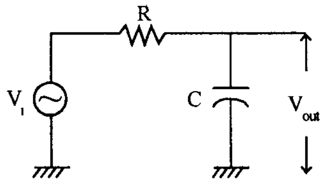


Fig. 2.20 Lag Network

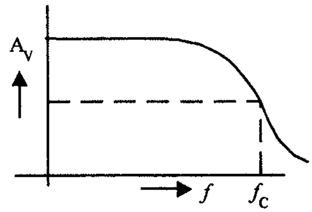


Fig. 2.21

at f_C, $\quad R = X_C$

$\therefore \quad \boxed{f_C = \frac{1}{2\pi RC}}$

Midband gain $\quad A_{mid} = \frac{R_L}{R_S + R_L}$

2.6.2 Decibel

Power gain $= G = \frac{P_2}{P_1}$

P_2 = Output power.
P_1 = Input power.

Decibel power gain $= G' = 10 \log_{10} G$.

If $G = 100$, $G' = 10 \log 100 =$ **20 db**.

If $G = 2$, $G' = 10 \log 2 = 3.01$db.

Usually, it is rounded off to 3.

2.6.3 Negative Decibel

If a < 1, a' will be negative.

If $\quad G = \frac{1}{2}$,

$G' = 10 \log \frac{1}{2} =$ **– 3.01 db**

	G	G'
If	1	0 db
	10	10 db
	100	20 db
	1000	30 db
	10, 000	40 db

Ordinary Gains Multiply :

If two stages are there,

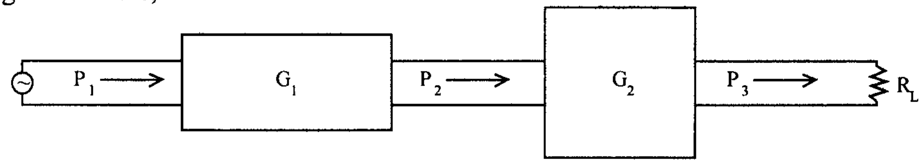


Fig. 2.22 Cascaded amplifier stages

$$G_1 = \frac{P_2}{P_1};\ G_2 = \frac{P_3}{P_2}$$

Overall gain $\quad G = \frac{P_3}{P_1}$

$$= \frac{P_2}{P_1} \cdot \frac{P_3}{P_2}$$

$$\mathbf{G = G_1\,G_2}$$

Decibel gains add up.

2.6.4 Decibel Voltage Gain

If $A =$ Normal Voltage Gain $\frac{V_2}{V}$, decibel voltage gain $A' = 20 \log A$. $A = \frac{V_2}{V_1}$

If R_1 is output resistance,

Input power $\quad P_1 = \frac{V_1^2}{R_1}$

If R_2 is output resistance, $P_2 = \frac{V_2^{\,2}}{R_2}$

$\therefore$ Power gain $\quad G = \frac{P_2}{P_1} = \frac{V_2^{\,2}}{V_1^{\,2}} \cdot \frac{R_1}{R_2}$

If the impedances are matched, i.e. input resistance

$R_1 =$ output resistance R_2

Power gain $\quad G = \frac{V_2^{\,2}}{V_1^{\,2}} = A^2$

In decibels, $10 \log G = G' = 10 \log A^2$.

In decibels, $10 \log G = G' = 20 \log A$.

2.6.5 Cascaded Stages

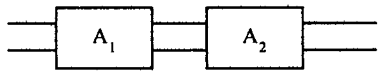


Fig. 2.23 Cascaded stages

$$A = A_1 \times A_2$$
$$A_1 = A_1' + A_2' \text{ (in decibels)}$$

2.6.7 Stiff Coupling

When the capacitor is chosen such that, $X_c = \dfrac{-R_E}{10}$, it is called as stiff coupling. Because, for the circuit shown.

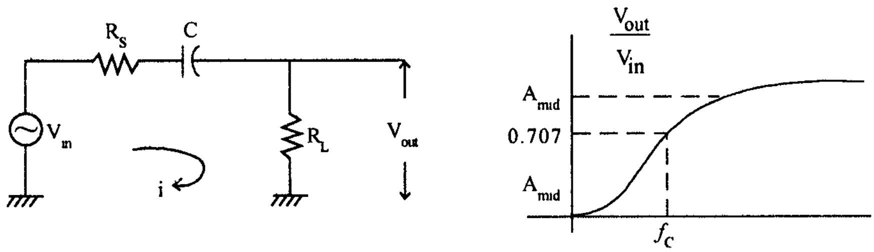


Fig. 2.24 Stiff coupling network

For the circuit, shown above, in the mid frequency range, X_c is negligible.

$\therefore$ $$i = \frac{V_{in}}{(R_S + R_L)}$$

$$V_{out} = i.\, R_L = \left(\frac{V_{in}}{R_S + R_L}\right) R_L.$$

$\therefore$ $A_{(mid)}$ = Voltage gain in the mid frequency range is,

$$A_{mid} = \frac{V_{out}}{V_{in}} = \frac{R_L}{R_S + R_L}$$

For the complete circuit, $\dfrac{V_{out}}{V_{in}} = \dfrac{R_L}{\sqrt{(R_S + R_L)^2 + {X_c}^2}}$

When $(R_S + R_L) = X_c, = \dfrac{1}{2\pi f_C C}$

$$\frac{V_{out}}{V_{in}} = \frac{R_L}{\sqrt{2}(R_S + R_L)}$$
$$= 0.707\, A_{mid}$$

$\therefore \qquad f_C = \dfrac{1}{2\pi(R_S + R_L).C}$

When $\qquad X_c = 0.1\ (R_S + R_L)$,

$$\frac{V_{out}}{V_{in}} = \frac{R_L}{\sqrt{(R_S+R_L)^2+[0.1\,(R_S+R_L)]^2}}$$

$$\frac{V_{out}}{V_{in}} = 0.995\ A_{mid}.$$

X_c is made = 0.1 (R_S + R_L), at the lowest frequency. (f_C lower)

$\therefore$ At the frequency, A = 0.995 A_{mid}. So it is called as *Stiff Coupling*.

$$A = \frac{V_{out}}{V_{in}} = \frac{X_c}{\sqrt{R^2 + X_c^{\ 2}}} = \frac{1}{\sqrt{1+\left(\dfrac{R}{X_c}\right)^2}}$$

$\because \qquad \dfrac{R}{X_c} = \dfrac{R}{\dfrac{1}{2\pi\ f_C}} = 2\pi fRC = \dfrac{f}{f_C}$

$\because \qquad f_c = \dfrac{1}{2\pi RC}$

$\therefore \qquad A = \dfrac{1}{\sqrt{1+\left(\dfrac{f}{f_C}\right)^2}}$

Decibel voltage gain $A' = 20 \log \dfrac{1}{\sqrt{1+\left(\dfrac{f}{f_c}\right)^2}}$

f_C = cutoff frequency.

When $\qquad \dfrac{f}{f_C} = 0.1,$

$$A_1 = 20 \log \frac{1}{\sqrt{1+(0.1)^2}} \cong 0\text{db}$$

When $\dfrac{f}{f_C} = 1,$

$$A^1 = 20 \log \frac{1}{\sqrt{1+1^2}} = -3.01 \text{ db} \cong 3 \text{ db}$$

When $\dfrac{f}{f_C} = 10,$

$$A^1 = 20 \log \frac{1}{\sqrt{1+10^2}} = -20 \text{ db}$$

When $\dfrac{f}{f_C} = 100,$

$$A^1 = 20 \log \frac{1}{\sqrt{1+100^2}} = -40 \text{ db}$$

When $\dfrac{f}{f_C} = 1000,$

$$A^1 = 20 \log \frac{1}{\sqrt{1+1000^2}} = 60 \text{ db}$$

$\therefore$ when $f = \dfrac{f_C}{10}$, $A' = 0$

$f = f_C$, $A_1 = -3$ db

$f = 10 f_C$, $A_1 = -20$ db

and so on.

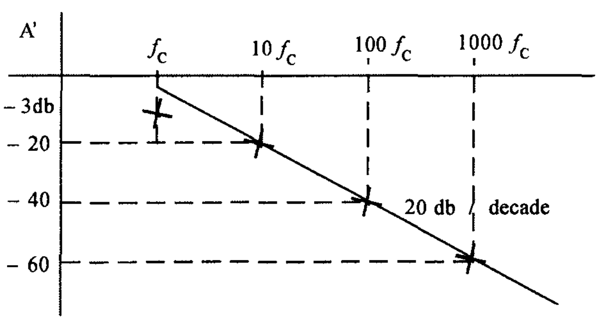


Fig. 2.25 Frequency Roll - off

$\therefore$ A change of **20db** per decade *change* in frequency.

An Octave is a factor of 2 in frequency change

When *f changes from 100 to 200 Hzs, it has changed by one octave.*

When, f changes from 100 to 400 Hzs, it is two octaves for lead network, Bode Plot is

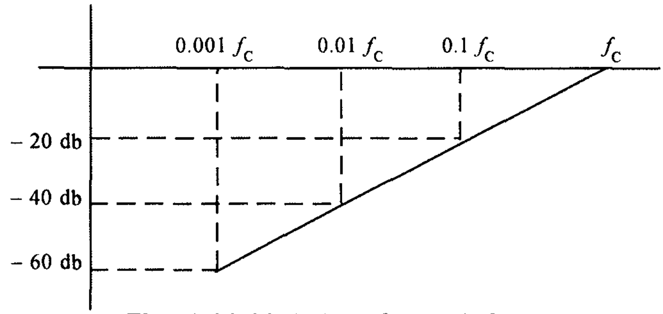


Fig. 2.26 Variation of A_V with f

2.7 High Input Resistance Transistor Circuits

In some applications the amplifier circuit will have to have very high input impedance. Common Collector Amplifier circuit has high input impedance and low output impedance. But its $A_V < 1$. If the input impedance of the amplifier circuit is to be only 500 KΩ or less the Common Collector Configuration can be used. But if still higher input impedance is required a circuit shown in Fig. 2.29 is used. This circuit is known as the ***Darlington Connection*** (named after Darlington) or ***Darlington Pair Circuit.***

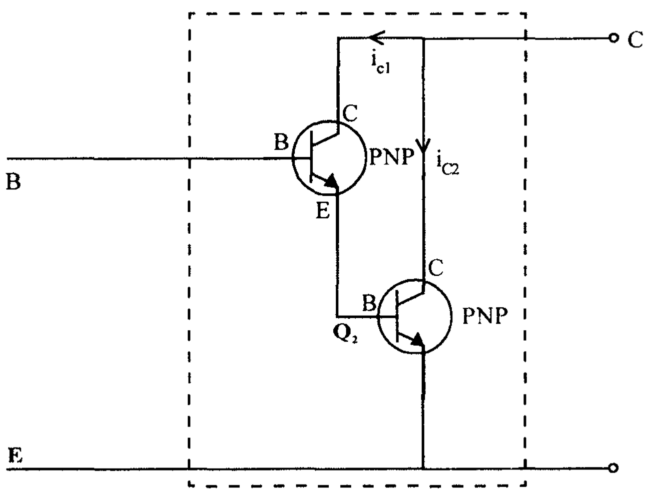


Fig. 2.27 Darlington Pair Circuit

In this circuit, the two transistors are in Common Collector Configuration. The output of the first transistor Q_1 (taken from the emitter of the Q_1) is the input to the second transistor Q_2 at the base. The input resistance of the second transistor constitutes the emitter load of the first transistor. So, Darlington Circuit is nothing but two transistors in Common Collector Configuration connected in series. The same circuit can be redrawn as AC equivalent circuit. So, DC is taken as ground shown in Fig.2.29. Hence, 'C' at ground potential. Collectors of transistors Q_1 and Q_2 are at ground potential.

The AC equivalent Circuit is shown in Fig. 2.29.

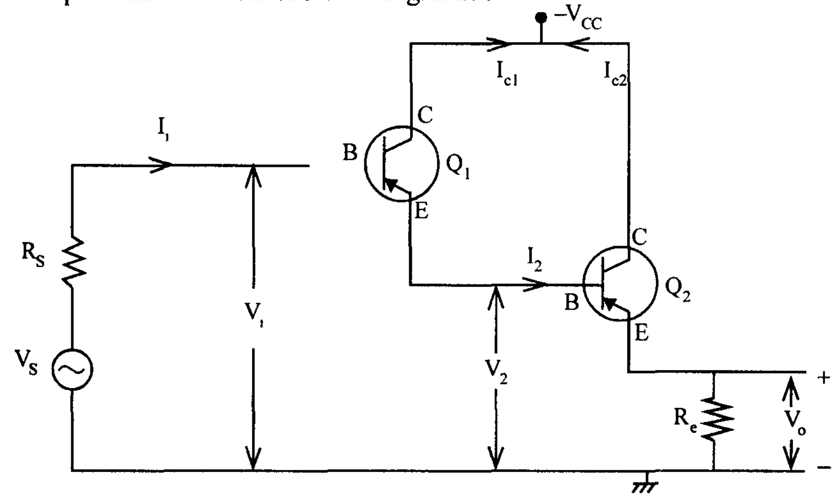


Fig. 2.28 AC equivalent circuit of Darlington Pair

There is no resistor connected between the emitter of Q_1 and ground i.e., Collector Point. So, we can assume that infinite resistance is connected between emitter and collector. For the analysis of the circuit, consider the equivalent circuit shown in Fig. 2.29 and we use Common Emitter ***h-parameters***, h_{ie}, h_{re}, h_{oe} and h_{fe}.

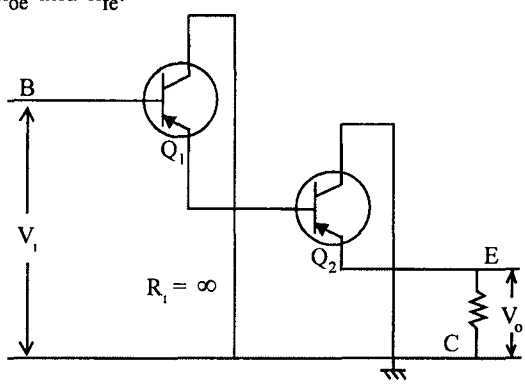


Fig. 2.29 Simplified circuit

For PNP transistor, I_c leaves the transistor, I_e enters the transistor and I_b leaves the transistor.

2.7.1 Current Amplification for Darlington Pair

$I_c = I_{c1} + I_{c2}$.

$I_{c1} = I_{b1}\, h_{fe}$;

$I_{c_2} = I_{b_2}\, h_{fe}$. (Assuming identical transistor and h_{fe} is same)

But $\quad I_{b_2} = I_{e_1}$ (The emitter of Q_1 is connected to the base of Q_2)

$\therefore \quad I_c = I_{b1}\, h_{fe} + I_{e1}\, h_{fe}$ .....(1)

$I_{e_1} = I_{b_1} + I_{c_1} = I_{b_1}\,(1 + h_{fe})$ .....(2)

$\therefore \quad I_{c_1} = h_{fe}\, I_{b_1}$

Substituting equation (2) in (1),

$$I_c = I_{b_1} h_{fe} + I_{b_1}(1 + h_{fe})h_{fe} = I_{b_1}(2h_{fe} + h_{fe}^2)$$

But $h^2_{fe} >> 2h_{fe}$

Since, h_{fe} is of the order of 100.

$$\therefore \quad I_c = I_{b_1} h_{fe}^2$$

It means that we get very large current amplification $\left(A_I = \frac{I_c}{I_{b_1}}\right)$ in the case of Darlington Pair Circuit, it is of the order h_{fe}^2 i.e. $100^2 = 10{,}000$.

$$\therefore \quad \boxed{A_I = \frac{I_c}{I_{b_1}} \cong (h_{fe})^2}$$

2.7.2 Input Resistance (R_i)

Input resistance R_{i_2} of the transistor Q_2 (which is in Common Collector Configuration) in terms of ***h- parameters*** in Common Emitter Configuration is,

$$R_{i_2} = h_{ie} + (1+h_{fe})\, R_L$$

But $\quad h_{ie} << h_{fe}R_L$, and $h_{fe}\, R_E >> h_{ie}$, $A_{I_2} = \frac{I_0}{I_2} = (1 + h_{fe})$

Here R_L is R_e, since, output is taken across emitter resistance.

$$\therefore \quad R_{i2} \cong (1+ h_{fe})\, R_e$$

The input resistance Ri_1 of the transistor Q_1 is, since it is in Common Collector Configuration

$$R_i = h_{ic} + h_{re}\, A_I.R_L.$$

Expressing this in term of Common Emitte' ***h-parameters***,

$$hi_C \cong h_{ie};\; h_{rc} \cong 1.$$

(For Common Collector Reverse Voltage Gain is equal to 1) and R_L for transistor Q_1 is the input resistance of transistor Q_2.

$\therefore \quad R_{i_1} = h_{ie} + A_{I_1} R_{i2}$. R_{i_2}, is large,

Therefore, $\quad h_{oe}.R_{i_2} \leq 0.1$. and $A_I \cong 1+ h_{fe}$

$$R_{i_1} \cong A_{I_1} R_{i_2}$$

$$R_{i_2} = (1 + h_{fe})\, R_e$$

But the expression for Common Collector Configuration in terms of Common Emitter ***h-parameters*** is

$$A_I = \frac{1+h_{fe}}{1+h_{oe}.R_L}$$

Here, $\quad R_L = R_{i2}$ and $R_{i2} = (1 + h_{fe})\, R_e$.

$$\therefore \qquad A_{I1} = \frac{1+h_{fe}}{1+h_{oe}(1+h_{fe})R_e}$$

$h_{oe}\,R_e$ will be is less than 0.1 and can be neglected.

$\therefore$ h_{o_e} value is of the order of μ mhos (micro mhos)

$$\therefore \qquad A_{I1} = \frac{1+h_{fe}}{1+h_{oe}h_{fe}R_e}$$

$$\therefore \qquad R_{i1} \simeq A_{I1}.\,R_{i2}$$

$$\boxed{R_i \simeq \frac{(1+h_{fe})^2 R_e}{1+h_{oe}h_{fe}R_e}}$$

This is a very high value. If we take typical values, of R_e = 4KW, using ***h-parameters,***

R_{i_2} = 205 KΩ.
R_i = 1.73 MΩ.
A_I = 427.

Therefore, Darlington Circuit has ***very high input impedance*** and very ***large current gain*** compared to Common Collector Configuration Circuit .

2.7.3 Voltage Gain

General expression for A_v for Common Collector in term of ***h-parameters*** is

$$A_v = 1 - \frac{h_{ie}}{R_i};\ h_{ie} \cong h_{ic} \quad \text{or } A_{V_1} = \frac{V_2}{V_i} = \left[1-\frac{h_{ie}}{R_{i_1}}\right]$$

But $\qquad R_i \cong A_{I1}.\,R_2.$

$$\therefore \qquad A_{V_1} = \left(-\frac{h_{ie}}{A_{I_1}\,R_{i_2}}\right)$$

$$\therefore \qquad A_{V2} = \frac{V_O}{V_2} = \left(1-\frac{h_{ie}}{R_{i2}}\right)$$

Therefore, over all Voltage Gain $A_v = A_{v_1} \times A_{v_2}$

$$= \left(1-\frac{h_{ie}}{A_{I_1}.R_{i_2}}\right)\left(1-\frac{h_{ie}}{R_{i_2}}\right)$$

$$A_v \cong \left(1-\frac{h_{ie}}{Ri_2}\right) \qquad \because\ R_{i_2} >> h_{ie}\ \text{ and } A_{i_1} \text{ is } >> 1$$

Therefore, A_v is always less than 1.

2.7.4 Output Resistance

The general expression for R_o of a transistor in Common Collector Configuration in terms of Common Emitter ***h-parameters*** is,

$$R_o = \frac{R_s + h_{ie}}{1 + h_{fe}}$$

$$\therefore \qquad R_{o1} = \frac{R_s + h_{ie}}{1 + h_{fe}}$$

Now for the transistor Q_2, R_s is R_{o1}.

$$\therefore \qquad R_{o2} = \frac{\dfrac{R_s + h_{ie}}{1 + h_{fe}} + h_{ie}}{1 + h_{fe}}$$

Therefore, R_{o2} is the output resistance of the Darlington Circuit.

$$\therefore \qquad R_{o2} = \frac{R_s + h_{ie}}{(1 + h_{fe})^2} + \frac{h_{ie}}{1 + h_{fe}}$$

This is a small value, since, $1 + h_{fe}$ is $>> 1$.

Therefore, the characteristic of Darlington Circuit are

1. *Very High Input Resistance (of the order of $M\Omega$).*
2. *Very Large Current Gain (of the order of 10,000).*
3. *Very Low Output Resistance (of the order of few Ω).*
4. *Voltage Gain, $A_v < 1$.*

Darlington Pairs are available in a single package with just three leads, like one transistor in integrated form.

2.7.5 Disadvantages

We have assumed that the ***h-parameters*** of both the transistors are identical. But in practice it is difficult to make ***h-parameters*** depend upon the operating point of Q_1 and Q_2. Since the emitter current of transistor Q_1 is the base current for transistor Q_2, the value of $I_{c2} >> I_{c1}$

1. *The quiescent or operating conditions of both the transistors will be different. h_{fe} value will be small for the transistor Q_1.* $\because$ *$h_{fe} = (I_c/I_b).I_{b2}$ is less*

   CDIL make CIL997 is a transistor of Darlington Pair Configuration with $h_{fe} = 1000$.
2. *The second drawback is leakage current of the first transistor Q_1 which is amplified by the second transistor Q_2 ($\because$ $I_{e1} = I_{b2}$).*

Hence overall leakage current is more. Leakage Current is the current that flows in the circuit with no external bias voltages applied

(a) *The **h-parameters** for both the transistors will not be the same.*

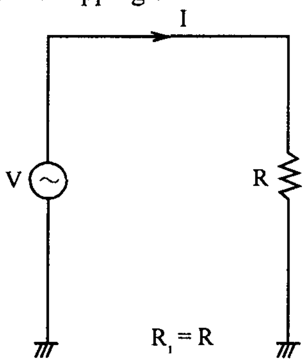
(b) *Leakage Current is more.*

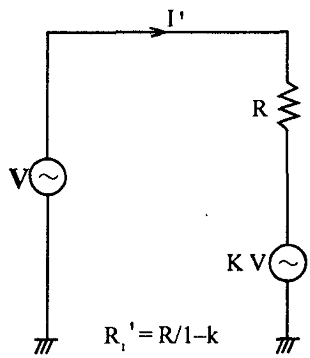
Darlington transistor pairs are in single package available with h_{fe} as high as 30,000

2.7.6 Boot Strapped Darlington Circuit

The maximum input resistance of a practical Darlington Circuit is only 2 MΩ. Higher input resistance cannot be achieved because of the biasing resistors R_1, R_2 etc. They come in parallel with R_i of the transistors and thus reduce the value of R_i. The maximum value of R_i is only $\frac{1}{h_{ob}}$ since, h_{ob} is the resistance between base and collector. The input resistance can be increased greatly by boot strapping, the Darlington Circuit through the addition of C_0 between the first collector C_1 and emitter B_2.

What is Boot Strapping ?





Boot strapping

Fig. 2.30 **Fig 2.31**

In Fig. 2.31, V is an AC signal generator, supplying current I to R. Therefore, the input resistance of the circuit as seen by the generator is $R_i = \frac{V}{I}$ = R itself. Now suppose, the bottom end of R is not at ground potential but at higher potential i.e. another voltage source of KV (K< 1) is connected between the bottom end of R and ground. Now the input resistance of the circuit is (Fig.2.31).

$$R_i' = \frac{V}{I'} \qquad I' = \frac{(V - KV)}{R}$$

or $$R_i' = \frac{VR}{V(1-K)} = \frac{R}{1-K}$$

I' can be increased by increasing V. When V increases KV also increases. K is constant. Therefore the potential at the two ends of R will increase by the same amount, K is less than 1, therefore $R_i > R$. Now if K = 1, there is no current flowing through R (So V = KV there is no

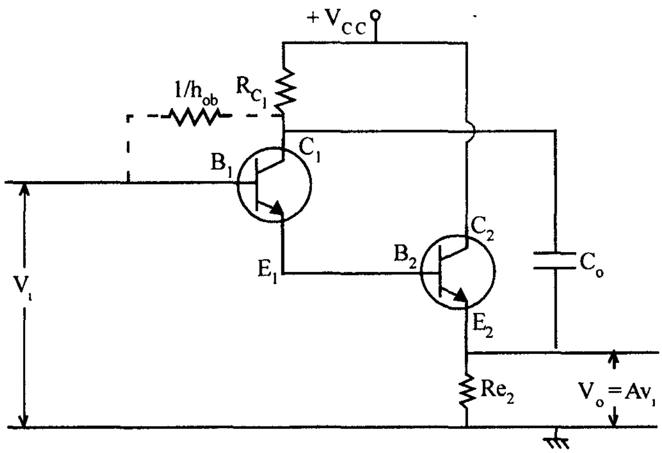


Fig. 2.32 Boot Strap Circuit

potential difference). So the input resistance $R_i = \infty$. Both the top and bottom of the resistor terminals are at the same potential. This is called as the Boots Strapping method which increases the input resistance of a circuit. If the potential at one end of the resistance changes, the other end of R also moves through the same potential difference. It is as if R is pulling itself up by its boot straps. For CC amplifiers $A_v < 1 \cong 0.095$. So R_i can be made very large by this technique. $K = A_V \cong 1$. If we pull the boot with both the edges of the strap (wire) the boot lifts up. Here also, if the potential at one end of R is changed, the voltage at the other end also changes or the potential level of R_3 rises, as if it is being pulled up from both the ends.

For Common Collector Amplifier,

$$R_i = \frac{h_{ie}}{1-A_{V.}}; \quad A_V \cong 1.$$

Therefore, R_i can be made large, since it is of the same form as

$$R_i = \frac{R}{1-K}$$

In the circuit shown in Fig. 2.32, capacitor C_0 is connected between C_1 and E_2. If the input signal changes by V_i, then E_2 changes by $A_v.V_i$ (assuming the resistance of C_0 is negligible).

Therefore, $\frac{1}{h_{ob}}$ is now effectively increased to $\frac{1}{h_{ob}(1-Av)} \cong 400M\Omega$

2.7.7 AC Equivalent Circuit

The input resistance

$$R_i = \frac{V_i}{I_{b1}} \cong h_{fe_1} h_{fe_2} R_e$$

If we take h_{fe} as 50, $R_e = 4K\Omega$, we get R_i as $10M\Omega$. If a transistor with $h_{fe} = 100$ is taken, R_i will be much larger. The value of X_{C_0} is chosen such that at the lower frequencies, under consideration X_{C_0} is a virtual short circuit. If the collector C_1 changes by certain potential, E_2 also changes by the same amount. So C_1 and E_2 are boot strapped. There is $\frac{1}{h_{ob}}$ between B_1 and C_1.

$$\therefore \qquad R_{eff} = \frac{1}{h_{ob}(1 - A_v)}$$

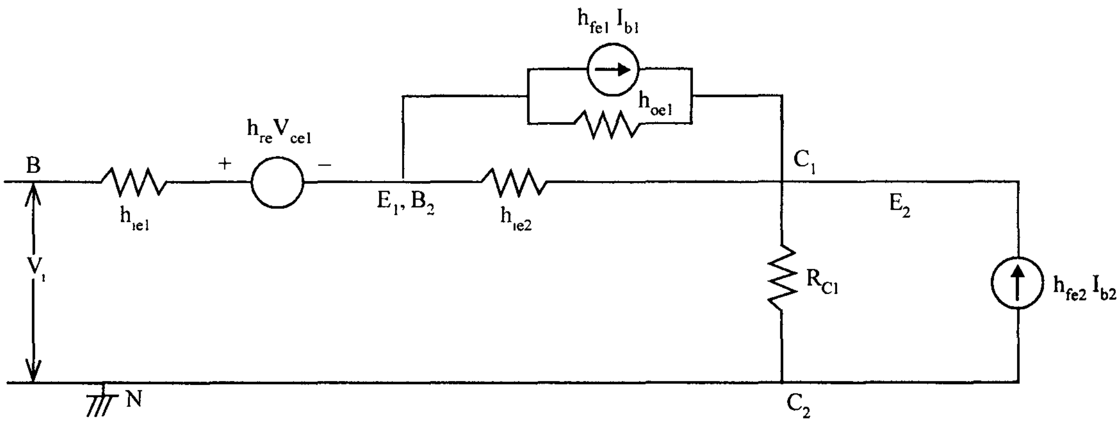


Fig. 2.33 AC equivalent circuit

Direct short circuit is not done between C_1 and E_2. Since, DC condition will change, X_{c_0} is a short only for AC signals and not for DC.

2.8 The CASCODE Transistor Configuration

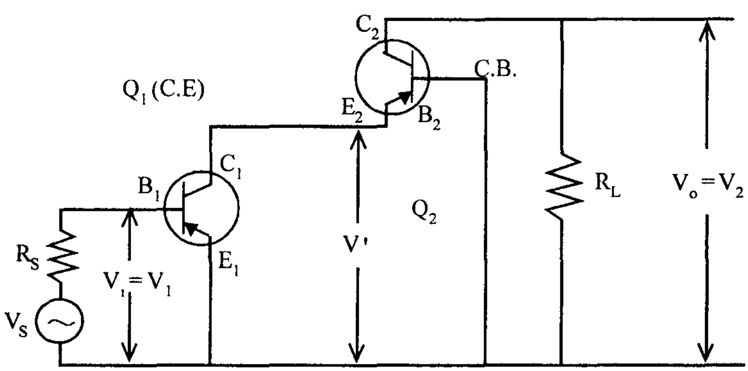


Fig. 2.34 CASCODE Amplifier (C.E, C.B configuration)

The circuit is shown in Fig. 2.34. This transistor configuration consists of a ***Common Emitter Stage*** in cascade with a ***Common Base Stage***. The collector current of transistor Q_1 equals the emitter current of Q_2.

The transistor Q_1 is in Common Emitter Configuration and transistor Q_2 is in Common Base Configuration. Let us consider the input impedance (h_{11}) etc., output admittance (h_{22}) i.e. the ***h - parameters*** of the entire circuit in terms of the ***h - parameters*** of the two transistors.

2.8.1 Input |Z| (h_{11})

$$h_{11} = \text{Input } Z = \left.\frac{V_1}{I_1}\right|_{V_2 = 0}$$

If V_2 is made equal to 0, the net impedance for the transistor Q_1 is only h_{ib_2}. But h_{ib}, for a transistor in common emitter configuration is very small $\cong$ 20. We can conclude that the collector of Q_1 is effectively short circuited.

$$\therefore \qquad h_{11} \cong h_{ie}$$

When $V_2 = 0$, C_2 is shorted. Therefore, $h_{12} = h_{ib_2}$. But h_{ib_2} is very small. Therefore C_1 is virtually shorted to the ground.

$$\therefore \qquad \boxed{h_i = h_{ie}}$$

2.8.2 Short Circuit Current Gain (h_{21})

$$h_{21} = \left.\frac{I_2}{I_1}\right|_{V_2 = 0}$$

$$h_{21} = \left.\frac{I_2}{I_1} = \frac{I}{I_1} \times \frac{I_2}{I_0}\right|_{V_2=0}$$

$$\frac{I'}{I_1} = h_{fe} \qquad \text{since, } I = I_{C_1}.\ I_1 = I_{B_1}$$

$$\frac{I_2}{I'} = -h_{fb} \quad \text{since, } I = I_{E_2}.\ I_2 = I_{C_2}.$$

$$\therefore \qquad h_{21} = -h_{fe}.\ h_{fb}.$$

$$h_{fe} >> 1\ .\ -h_{fb} \simeq 1, \qquad \text{since } h_{fb} = \frac{I_C}{I_E}$$

$$\therefore \qquad \boxed{h_{21} \cong h_{fe}}$$

2.8.3 Output Conductance (h_{22})

Output Conductance with input open circuited, for the entire circuit is,

$$h_{22} = \left.\frac{I_2}{V_2}\right|_{I_1 = 0}$$

when $I_1 = 0$, the output resistance of the transistor Q_1 is $\frac{1}{h_{oe}} \cong 40\ K\Omega$. (Since Q_1 is in Common Emitter configuration and h_{oe} is defined with $I_1 = 0$).

$$\therefore \qquad \frac{1}{h_{oe}} \cong 40K\Omega$$

is the source resistance for Q_2. Q_2 is in Common Base Configuration. What is the value of R_o of the transistor Q_2 with $R_s \cong 40k$

It is $\cong 1/h_{ob}$ itself.

Since, h_{oe_1} is very large, we can say that $I_1' = 0$ or between E_2 and ground there is infinite impedance. Therefore, output conductance of the entire circuit is $h_{22} \cong h_{ob}$.

2.8.4 Reverse Voltage Gain

$$h_{12} = \left.\frac{V_1}{V_2}\right|_{I_1 = 0}$$

$$= \left.\frac{V_1}{V'} \times \frac{V^1}{V_2}\right|_{I_1 = 0}$$

$$\left.\frac{V_1}{V_0'}\right|_{I_i = 0} = h_{re} \cdot \left.\frac{V'}{V_2}\right| = h_{rb}$$

(Since, Q_2 is in Common Base configuration)

$$\therefore \qquad h_{12} \cong h_{re}\, h_{rb}.$$

$h_{re} \cong 10^{-4}$ $\quad h_{rb} = 10^{-4}$. $\because$ h_{12} is very small

$\because$ $\quad h_i = h_{11} \cong h_{ie}$. $\quad$ Typical value = 1.1KΩ

$h_f = h_{21} \cong h_{fe}$. $\quad$ Typical value = 50

$h_o = h_{22} \cong h_{ob}$. $\quad$ Typical value = 0.49 μ A/V

$h_r = h_{12} \cong h_{re}\, h_{rb}$. $\quad$ Typical value = 7×10^{-8}.

Therefore, for a CASCODE Transistor Configuration, its input Z is equal to that of a single Common Emitter Transistor (h_{ie}). Its Current Gain is equal to that of a single Common Base Transistor (h_{fe}). Its output resistance is equal to that of a single Common Base Transistor (h_{ob}). The reverse voltage gain is very very small, i.e., there is no link between V_1 (input voltage) and V_2 (output voltage). In otherwords, there is negligible internal feedback in the case of, a CASCODE Transistor Circuit, acts like a single stage C.E. Transistor (Since h_{ie} and h_{fe} are same) with negligible internal feedback ($\therefore$ h_{re} is very small) and very small output conductance, ($\cong$ h_{ob}) or large output resistance ($\cong$ 2MΩ equal to that of a Common Base Stage). The above values are correct, if we make the assumption that $h_{ob} R_L < 0.1$ or R_L is < 200K. When the value of R_L is < 200 K. This will not affect the values of h_i, h_r, h_o, h_f of the CASCODE Transistor, since, the value of h_r is very very small.

CASCODE Amplifier will have

1. *Very Large Voltage Gain.*
2. *Large Current Gain (h_{fe}).*
3. *Very High Output Resistance.*

Example : 2.6

Find the voltage gains A_{vs}, A_{v1} and A_{v2} of the amplifier shown in Fig.2.35.

Assume

h_{ie} = 1KΩ, $h_{re} = 10^{-4}$, $h_{fe} = 50$

and $h_{oe} = 10^{-8}$ A / V.

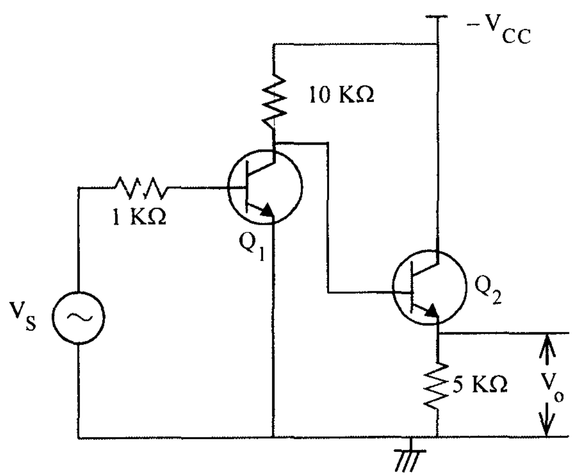


Fig. 2.35 Amplifier circuit Ex : 2.6

Solution :

The second transistor Q_2 is in Common Collector Configuration Q_1 is in Common Emitter Configuration. It is convenient if we start with the II stage.

II Stage :

$$h_{oe}.\ R_{L_2} = 10^{-8} \times 5 \times 10^3 = 5 \times 10^{-5} < 0.1.$$

Therefore, $h_{oe}\ R_{L_2}$ is < 0.1, approximate analysis can be made, rigorous expression of C.C. and C.B Configuration need not be used.

$$\therefore \quad R_{i_2} = h_{ie} + (1+h_{fe})R_{L_2}$$
$$= 1K\Omega + (1+50)\ 5K\Omega = 256\ K\Omega.$$

Av_2 is the expression for Voltage Gain of the transistor in Common Collector Configuration in terms of Common Emitter ***h-parameters*** is

$$A_{V_2} = 1 - \frac{h_{ie}}{R_{i_2}}$$

$$= 1 - \frac{1K\Omega}{256K\Omega} = 1 - 0.0039 = 0.996$$

I Stage :

$$R_{L_1} = 10\ K \parallel R_{i_2} = 10\ K \parallel 256\ K\Omega = 9.36\ K\Omega.$$

$h_{oe}\ .\ R_{L_1} < 0.1. \quad \because$ approximate equation can be used

$$A_{I_1} = -50$$

$$R_{i_1} = h_{ce}. = 1K\Omega.$$

$$A_{v_1} = -h_{fe}\frac{R_{L_1}}{h_{ie}} = \frac{-50 \times 9.63k}{1K\Omega} = -48.$$

$$= \left(A_I.\frac{R_{L1}}{R_i}\right)$$

Overall Voltage Gain $= A_{v_1} . A_{v_2} = -482 \times 0.996 = -480.$

$$\therefore \quad A_{vs} = A_v \times \frac{R_S}{R_S + h_{ie}} = A_V \times \frac{1K\Omega}{2K} = -240.$$

2.9 CE – CC Amplifiers

This is another type of two-stage BJT amplifier. The first stage in Common Emitter (CE) configuration provides voltage and current gains. The second stage in Common-Collector (CC) configuration provides impedance matching. This circuit is used in audio frequency amplifiers. The circuit is shown in Fig. 2.36.

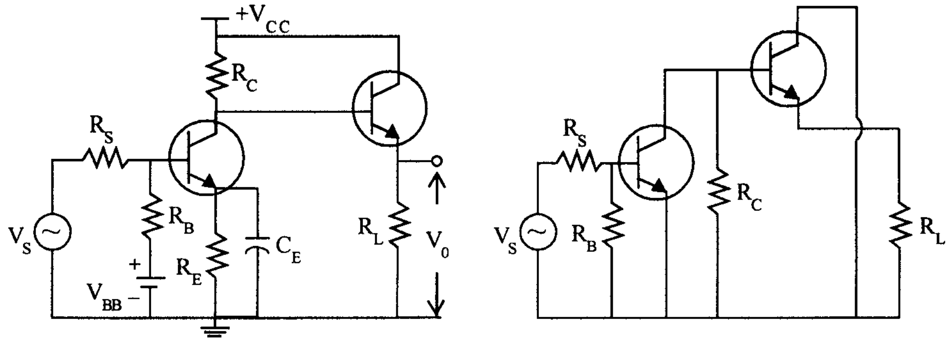


Fig. 2.36 CE, CC Amplifiers

Analysis

Here biasing resistors are neglected for simplification of analysis.

II Stage in CC amplifier :

$$R_{L_2} \simeq R_L$$

$$h_{oc}\ R_{L_1} \leq 0.1$$

$$A_{I2} = A_{I'2} = (1 + h_{fe})$$

$$R_{i_2} = (1 + h_{fe})\ R_{L_2}$$

$$A_{V2} = A_{V2'} = \frac{A_{I_2} . R_{L_2}}{R_{i_2}}$$

$$= \frac{\left(1 + h_{fe}\ R_{L_2}\right)}{h_{ie} + \left(1 + h_{fe}\right) R_{L_2}}$$

$$= 1 - \frac{h_{ie}}{R_{i_2}};$$

$\therefore$ $$A_{V_2} < 1$$

for CE stage

$$A_{I_1} = A_{I_1}' = -h_{fe}$$

$$R_{i_1} = R_{i_1}' = h_{ie}$$

$$A_{V_1} = A_{V_1}' = (A_{I_1} . R_{L_1} / R_i)$$

Overall Characteristics

$$A_V = A_{V_1} \cdot A'_{V_2}$$
$$R_i = R_{i_1}$$
$$R_o = R_{o_1}$$
$$A_I = \frac{A_V . R_{i_1}}{R_{L_2}}$$

2.10 Two Stage RC Coupled JFET amplifier (in Common Source (CS) configuration)

The circuit for two stages of RC coupled amplifier in CS configuration is as shown in Fig. 2.37.

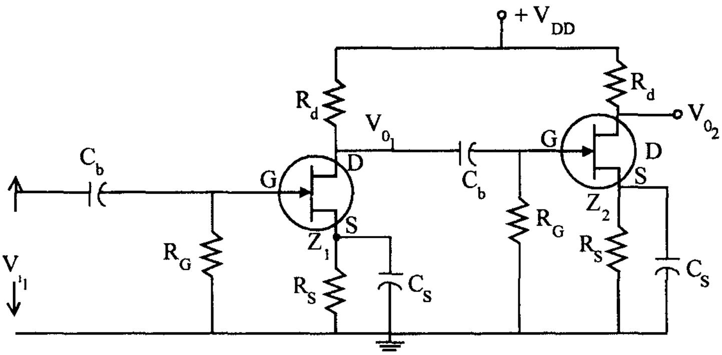


Fig. 2.37 Two stage RC coupled JFET amplifier

The output V_{0_1} of I Stage is coupled to the input V_{i_2} of II Stage through a blocking capacitor C_b. It blocks the DC components present in the output of I Stage from reaching the input of the II stage which will alter the biasing already fixed for the active device. Resistor R_g is connected between gate and ground resistor R_D is connected between drain and V_{DD} supply. C_S is the bypass capacitor used to prevent loss of gain due to negative feedback. The active device is assumed to operate in the linear region. So the small signal model of the device is valid.

Frequency Roll-off is the term used for the decrease in gain with frequency in the upper cut-off region. It is expressed as db/octave on db/decade. In the logarithmic scale of frequency,

octave is $\frac{f_2'}{f_2} = 2$ decade is $\frac{f_2'}{f_2} = 10$.

The purpose of multistage amplifiers is to get large gain. So with BJTs, Common Emitter Configuration is used. If JFETs are employed, common source configuration is used.

2.11 Difference Amplifier

This is also known as *differential amplifier*. The function of this is to amplify the difference between the signals. The advantage with this amplifier is, we can eliminate the noise in the input signals which is common to both the inputs. Thus S/N ratio can be improved. The difference amplifier can be represented as a blackbox with two inputs V_1 and V_2 and output V_0 where $V_0 = A_d (V_1 - V_2)$.

where A_d is the gain of the differential amplifier. But the above equation will not correctly describe the characteristic of a differential amplifier. The output V_0 depends not only on the difference of the two signals $(V_1 - V_2) = V_d$ but also on the average level called *common mode signal* $V_C = V_1 + V_2 \mid 2$.

If one signal is (V_1) 100 μV and the other signal (V_2) is −100 μV.

$\therefore$ V_0 should be A_d (200) μV.

Now in the second case, if V_1 = 800 μV, and V_2 = 600 μV. V_d = 800 − 600 = 200 μV and V_0 should be A_d (200) μV. So in both cases. for the same circuit. V_0 should be the same. But in practice it will not be so because the average of these two signals V_1 & V_2 is not the same in both the cases.

$$V_d = V_1 - V_2$$

$$V_c = \frac{1}{2}(V_1 + V_2)$$

from the equations above, we can write that,

$$V_1 = V_c + \frac{1}{2} V_d$$

[∵ If we substitute the values of V_c and V_d we get the same.

$$V_2 = V_c - \frac{1}{2} V_d \qquad V_1 = V_c + \frac{1}{2} V_d = \frac{V_1}{2} + \frac{V_1}{2} = V_1]$$

V_0 can be represented in the most general case as

$$V_0 = A V \ + A_2 V_2$$

Substituting the values of V_1 and V_2

$$V_0 = A_1 [V_c + \frac{1}{2} v_d] + A_2 [V_c - \frac{1}{2} V_d]$$

$$= A_1 V_c + \frac{A_1}{2} V_d + A_2 V_c - \frac{A_2}{2} V_d$$

$$V_0 = V_c (A_1 + A_2) + V_d \left[\frac{A_1 - A_2}{2}\right]$$

$$\therefore \quad V_0 = V_c A_c + V_d A_d$$

where $A_d = \dfrac{A_1 - A_2}{2}$ and $A_c = A_1 + A_2$.

for operational amplifiers, always input is given to the inverting node to get $\dfrac{A_1 - (-A_2)}{2}$ so that A_d is very large and A_c is very small.

A_1 and A_2 are the voltage gains of the two amplifier circuits separately.

The voltage gain from the difference signal is A_d.

The voltage gain from the common mode signal is A_c.

$$V_0 = A_d V_d + A_c V_c.$$

To measure A_d, directly set $V_1 = -V_2 = 0.5V$ so that

$$V_d = 0.5 - (-0.5) = 1V.$$

$$V_c = \frac{(0.5-0.5)}{2} = 0$$

$\therefore$ $$V_0 = A_d \,.\, 1 = A_d \text{ it self}$$

$\therefore$ If $V_1 = -V_2$ and output voltage is measured,

Output voltage directly gives the value of A_d.

Similarly if we set $V_1 = V_2 = 1V$. then

$$V_a = 0, \quad V_c = \frac{V_1 + V_2}{2} = \frac{2}{2} = 1V.$$

$\therefore$ $$V_0 = 0 + A_c \,.\, 1 = A_c.$$

$\therefore$ The measured output voltage directly gives Ac. We want A_d to be large and A_c to be very small because only the difference of the two signals should be amplified and the average of the signals should not be amplified. $\therefore$ The ratio of the these two gains $\rho = \left|\frac{A_d}{A_c}\right|$ is called the common mode rejection ratio. This should be large for a good difference amplifier.

$$V_0 = A_d V_d + A_c V_c$$

$$\rho = \frac{A_d}{A_c} \qquad \therefore\ A_c = \frac{A_d}{\rho}$$

$\therefore$ $$V_0 = A_d V_d + \frac{A_d}{\rho} \,.\, V_c$$

$$V_0 = A_d V_d \left(1 + \frac{1}{\rho} \cdot \frac{V_c}{V_d}\right)$$

2.12 Circuit for Differential Amplifier

In the previous D.C amplifier viz., C.B, C.C and C.E, the output is measured with respect to ground. But in difference amplifier, the output is α to the difference of the inputs. So V_0 is not measured w.r.t ground but w.r.t to the output of one transistor Q_1 or output of the other transistor Q_2.

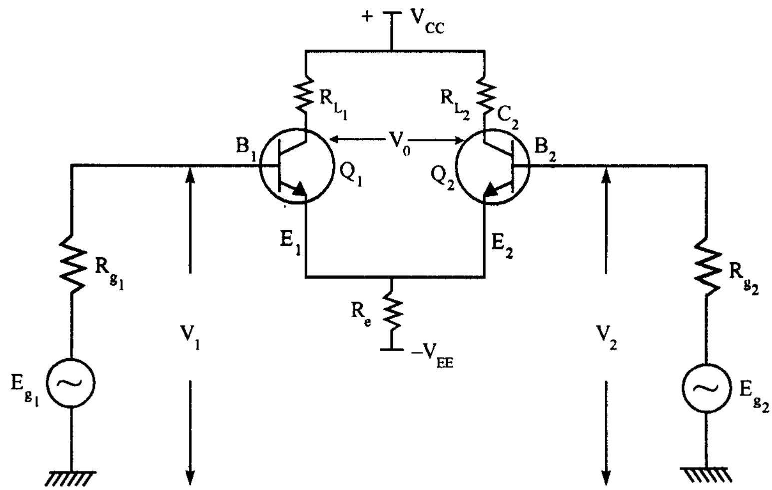
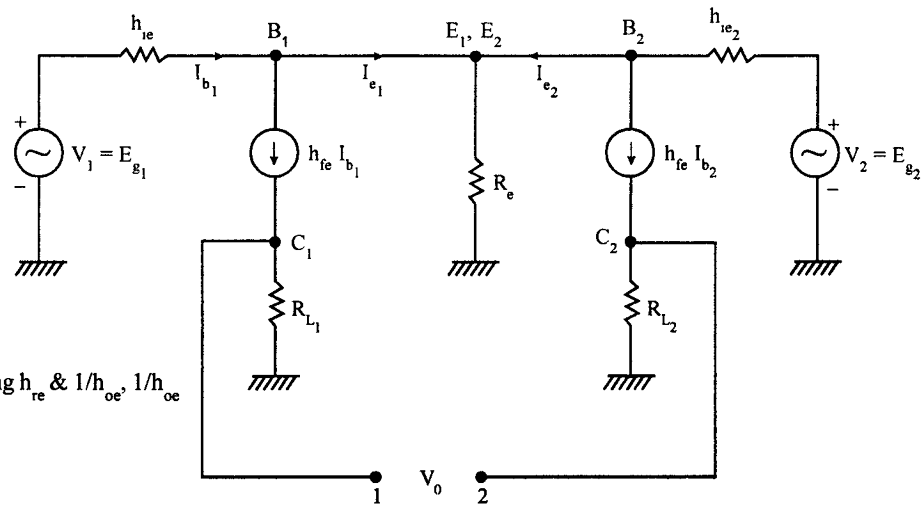


Fig. 2.38 Differential amplifier

Equivalent Circuit



Neglecting h_{re} & $1/h_{oe}$, $1/h_{oe}$

Fig. 2.39 Equivalent circuit

The advantage with this type of amplifiers is the drift problem is eliminated. Drift means, even when there is no input, V_i there can be some output V_0 which is due to the internal thermal noise of the circuit getting amplified and coming at the output. Drift is reduced in this type of circuit, because, the two points should be exactly identical. Hence, I_{c_s}, h_{FE}, V_{BE} will be the same for the two transistors. Now if I_{c_1} rises across R_L ($I_{c_1} R_{L_1}$) increases with increase in I_{c_1}. So the voltage at collector of Q_1 decreases. If Q_2 is also identical to Q_1 its collector voltage also drops by the same amount. Hence V_0 which is the difference of these voltages remains the same thus the drift of these transistors gets cancelled.

The input to a differential amplifer are of two types. 1. Differential mode 2. Common mode.

If V_1 and V_2 are the inputs, the differential mode input = $V_2 - V_1$.

Here two different a.c. signal are being applied V_1 & V_2. So these will be interference of these signals and so both the signals will be present simultaneously at both input points i.e., if V_1 is applied at point 1, it also prices up the signal V_2 and so the net input is $(V_1 + V_2)$. This is due to interference.

Common node input $= \dfrac{V_1 + V_2}{2}$

An ideal differential amplifier must provide large gain to the differential mode inputs and zero gain to command input.

$$\therefore \qquad V_0 = A_2 V_2 - A_1 V_1 \qquad .....(1)$$

A_2 = voltage gain of the transistor Q_2

A_1 = voltage gain of the transistor Q_1

we can also express the output in term of the common mode gain A_c and differentil gain A_d.

$$\therefore \qquad V_0 = A_d (V_2 - V_1) + A_c \left(\frac{V_1 + V_2}{2}\right) \qquad .....(2)$$

$$= A_d V_2 - A_d \cdot V_1 + A_c \cdot \frac{V_1}{2} + A_c \cdot \frac{V_2}{2} \qquad .....(3)$$

$$V_0 = V_2 \left(A_d + \frac{A_c}{2}\right) - V_1 \left(A_d - \frac{A_c}{2}\right) \qquad .....(4)$$

Comparing eqns. 4 and 1,

$$A_2 = A_d + \frac{A_c}{2}$$

$$A_1 = A_d + \frac{A_c}{2}$$

Solving these two eqns. $A_d = \dfrac{A_1 + A_2}{2}$

$$A_c = A_2 - A_1/2$$

µA 730 is an I.C differential amplifier.

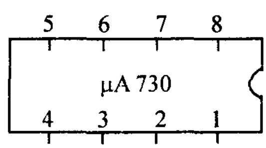


Fig. 2.40 IC µA 730 Pin configuration

8 pins. Input is given to pins 2 and 3. V^{+}_{cc} to pin 7, 4 is ground. Output is taken at pin no 6. In the difference amplifier, the difference of the input voltages V_1 and V_2 is amplified. The collectors of the transistor Q_1 & Q_2 are floating. They are not at ground potential. So the output voltage is not at ground potential. Hence the output voltage is the difference of the collector voltages (a.c) of transistors Q_1 & Q_2. Difference amplifiers are used in measuring instants and instrumentations systems. The difference of V_{i_1} & V_{i_2} may be 1 μV which is difficult to measure. So if this is amplified to 1mV or 1V the measurement will be accurate. So difference amplifiers are used to measure very small increased voltages.

While computing A_1 & A_2 of individual transistors, the other input should be made zero. One while computing A_1, $V_2 = 0$. Because there should be no common mode signal, while computing A_1, A_1 is the actual gain. Not differential gain. ∴ the other input is made zero.

In the case of operational amplifiers for single ended operation, always the positive end is grounded (non inverting input) & input is applied to the inverting input (–). It is because, at this part the feedback current & input current get added algebraically. So this is known as the swimming junction. When sufficient negative feedback is used, the closed looop performance becomes virtually independent of the characters of the operational amplifiers & depends on the external passive elements, which is desired.

Objective Type Questions

1. Based on the type of Coupling, the Amplifiers are classified as ____________
2. Based on Bandwidth, the amplifiers are classified as ____________
3. Different types of Distortion in amplifiers are ____________.
4. When n stages with gains A_1, A_2 .... A_n are cascaded, overall voltage gain A_{Vn} = ____________.
5. Expression for voltage gain A_v in the Mid Frequency range, interms of h_{fe}, R_L, R_S and h_{ie} is, A_V(M.F) = ____________
6. Expression for A_v (H.F) in terms of f, f_2 and A_v (M.F) is, A_v (H.F) = ____________
7. Phase shift ϕ interms of f_1 and f is, ____________.
8. Expression for A_v (L.F) in terms of f, f_1 and A_v (M.F) is ____________.
9. When n stages are cascaded, the relation between f_{2n}, and f_2 is ____________.
10. When h stages are cascaded, the relation between f_{1n} and f_1 is, ____________.
11. The relation between h_{fe}, f_β and f_T is ____________.
12. Figure of Merit of an amplifier circuit is ____________.
13. CMRR (ρ) = ____________.
14. Expression for V_0 interms of A_d, V_d, V_c and ρ is, ____________.
15. Expression for A_d and A_c interms of A_1 and A_2 are ____________.
16. Stiff coupling is ____________.
17. When frequency change is octave $\frac{f_2}{f_1}$ = ____________.
18. In cascade form, ordinary gains ____________ decibal gains ____________.
19. Phase response is a plot between ____________.
20. According to Miller's theorem the feedback capacitance when referred to input side, with gain A is ____________.
21. Interms of h_{fe}, current gain in Darlington Pair circuit is approximately ____________.
22. The disadvantage of Darlington pair circuit is ____________.

23. Compared to Common Emitter Configuration R_i of Darlington pair circuit is ___________________.
24. In CASCODE amplifier, the transistors are in ___________________ configuration.
25. The salient featuers of CASCODE Amplifier are ___________________
26. What is distortion ?
27. What are the types of distortion ? Define them.
28. How does the amplifier behave for low frequencies and high frequencies ?
29. Which configuration is the best in cascade for an output stage and for an intermediate stage ?
30. What is the darlington pair ? What is its significance ?
31. How is the bandwidth of a cascade affected compared to the bandwidth of a single stage ?
32. Why is the emitter bypass capacitor used in an RC coupled amplifier ?
33. What is the affect of emitter bypass capacitor on low frequency response ?
34. What are types of cascade ?
35. How would you differentiate an interacting stage from a non-interacting stage ?
36. What is the expression for the upper 3dB frequency for a n-stage non interacting cascade ?
37. What is the expression for lower 3dB cutoff frequency in n-stage interacting cascade ?
38. What is the expression for upper 3dB cutoff frequency in a n-stage interacting cascade ?
39. What is the slope of the amplitude response for an n-stage amplifier ?
40. Why do we go for multistage amplifier ?

Essay Type Questions

1. Explain about the classification of Amplifiers based on type of coupling and bandwidth.
2. What are the different types of distortions possible in amplifiers outputs ?
3. Obtain the expression for the voltage gain A_v in the L.F, M.F and H.F ranges, in the case of single stage BJT amplifier.
4. When h-identical stages of amplifiers are cascaded, derive the expressions for overall gain A_{vn}, lower cutoff frequency f_{1n} and upper cutoff frequency f_{2n}.
5. With the help of necessary waveforms, explain about the step response of amplifiers.
6. What is the significance of square wave testing in amplifiers ?
7. Draw the circuit for differential amplifier and derive the expression for CMRR.
8. Explain about the characteristics of operational amplifiers.
9. Draw the circuit for Darlington pair and device the expressions for A_I, A_V, R_i and R_O.
10. Draw the circuit for CASCODE Amplifier. Explain its working, obtaining overall values of the circuit for h_i, h_f, h_o and h_r.

Answers of Objective Type Questions

1. (a) R-C coupled (b) Transformer coupled
   (c) Direct coupled (d) Tuned circuit
2. (a) Narrow band (b) Untuned amplifiers
3. (a) Frequency distortion (b) Phase distortion (c) Amplitude distortion
4. $A_{vn} = A_1, A_2, A_3 \ldots.. A_n$
5. $A_v\,(M.F) = \dfrac{-h_{fe}.R_L}{R_S + h_{ie}}$
6. $A_v\,(H.F) = A_V\,(M.F) \Big/ 1 + j\left(\dfrac{f}{f_2}\right)$
7. $\phi = 180^0 - \tan^{-1}\left(\dfrac{f_1}{f}\right)$
8. $A_v\,(L.F) = \dfrac{A_V(M.F)}{1 - j\left(\dfrac{f_1}{f}\right)}$
9. $\dfrac{f_{2n}}{f_2} = \sqrt{\left(2^{1/n} - 1\right)}$
10. $f_{l_n} = f_l \Big/ \sqrt{2^{1/n} - 1}$
11. $h_{fe}, f_\beta = f_T$
12. Figure of merit = Gain × Bandwidth
13. CMRR = (A_d / A_c)
14. $V_0 = A_d\,V_d\left(1 + \dfrac{1}{\rho}.\dfrac{V_C}{V_d}\right)$
15. $A_d = \dfrac{(A_1 + A_2)}{2}$; $A_c = (A_2 - A_1)/2$
16. When capacitor is chosen such that $X_C = \dfrac{R_E}{10}$
17. 2
18. Multiply, Add up

19. Phase angle and frequency
20. $C_{in} = C\,(1 - A)$
21. $(h_{fe})^2$
22. Leakage current is more
23. Very high
24. CE – CB
25. Large voltage and current gains
26. If the output waveform is not the replica of the input waveform, it is called distortion.
27. (i) Non linear distortion : If harmonic frequencies are generated at the o/p, it is called non linear or amplitude distortion.

    (ii) Freqeuncy distortion : If different frequency components are amplified differently, it is called frequency distortion.

    (iii) Phase distortion : If the output is shifted by different phased each time, it is called phase distortion.
28. Low frequencies - high pass filter.

    High frequencies - low pass filter.
29. Output stage - CC

    Intermediate stage - CE
30. CC-CC cascade is called Darlington pair.

    Significance : (i) It has very high input impedance. (ii) It behaves life a constant current source.
31. It decreases.
32. To decrease the loss in gain due to negative feedback
33. The tilt is more
34. Interacting and non interacting.
35. If the input impedance of next stage loads the previous stage, it is called interacting stages. If the input impedance of next stage does not load the previous stage, it is called non interacting stage.
36. $f_L = \dfrac{f}{\sqrt{2^{1/n} - 1}}$
37. $f_H = f \cdot \sqrt{2^{1/n} - 1}$
38. $f_H = 0.94\,f_D$.
39. 6n dB/octave or 20n dB/decade.
40. For high gain.

UNIT - 3

High Frequency Transistor Circuits

In this Unit,

- Single stage amplifiers in the three configurations of C.E, C.B, C.C, with design aspects are given.
- Using the design formulae for A_V, A_I, R_i, R_o etc, the design of single stage amplifier circuits is to be studied.
- Single stage JFET amplifiers in C.D, C.S and C.G configurations are also given.
- The Hybrid - π equivalent circuit of BJT, expressions for Transistor conductances and capacitances are derived.
- Miller's theorem, definitions for f_β and f_T are also given.
- Numerical examples, with design emphasis are given.

3.1 Transistors at High Frequencies

At low frequencies it is assumed that *Transistor* responds instantaneously to changes in the input voltage or current i.e., if you give AC signal between the base and emitter of a *Transistor* amplifier in Common Emitter configuration and if the input signal frequency is low, the output at the collector will exactly follow the changes in the input (amplitude etc.,). If '*f*' of the input is high (MHz) and the amplitude of the input signal is changing the *Transistor* amplifier will not be able to respond.

What is the reason for this ? It is because, the carriers from the emitter side will have to be injected into the *collector* side. These take definite amount of time to travel from Emitter to Base, however small it may be. But if the input signal is varying at a much higher speed than the actual time taken for the carries to respond, then the *Transistor* amplifier will not respond instantaneously. Thus, the junction capacitances of the transistor, puts a limit to the highest frequency signal which the transistor can handle. Thus depending upon doping area of the junction etc, we have transistors which can respond in AF range and also RF range.

To study and analyze the behavior of the transistor to high frequency signals an equivalent model based upon transmission line equations will be accurate. But this model will be very complicated to analyze. So some approximations are made and the equivalent circuit is simplified. If the circuit is simplified to a great extent, it will be easy to analyze, but the results will not be accurate. If no *approximations* are made, the results will be accurate, but it will be difficult to analyze. The desirable features of an equivalent circuit for analysis are simplicity and accuracy. Such a circuit *which is fairly simple and reasonably accurate* is the *Hybrid-pi* or *Hybrid-π model, so called because the circuit is in the form of π. The parameter have units of Ω, ℧ etc. So it is a hybrid circuit. Hence it is called as hybrid-π model.* Using this model a detailed analysis of single stage Common Emitter Transconductance amplifier is made.

3.2 Hybrid - π Common Emitter Transconductance Model

For *Transconductance* amplifier *circuits Common Emitter configuration is preferred. Why* ? Because for Common Collector ($h_{rc} < 1$). For Common Collector Configuration, voltage gain $A_V < 1$. So even by cascading you can't increase voltage gain. For Common Base, current gain $h_{fb} < 1$. So overall voltage gain is < 1. But for Common Emitter, $h_{fe} >> 1$. Therefore Voltage gain can be increased by cascading Common Emitter stage. So Common Emitter configuration is widely used.

The *Hybrid-π* or *Giacoletto Model* for the Common Emitter amplifier circuit (single stage) is as shown :

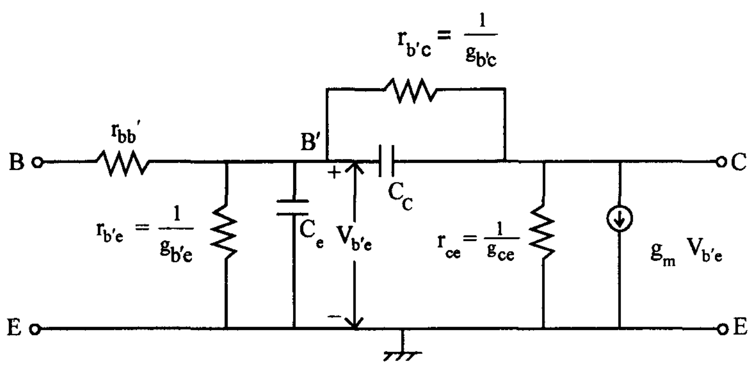


Fig. 3.1 Hybrid - π C.E BJT Model

Analysis of this circuit gives satisfactory results at *all* frequencies not only at *high frequencies* but also at *low frequencies*. All the parameters are assumed to be independent of frequency.

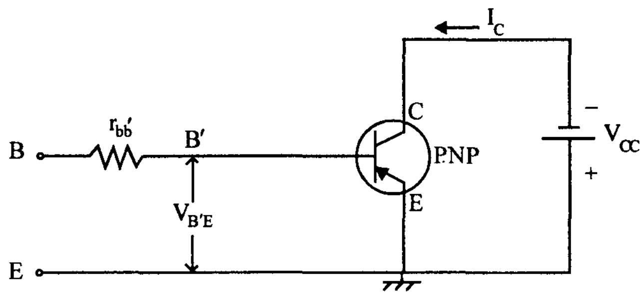


Fig. 3.2 PNP transistor amplifier

3.2.1 Circuit Components

B' is the internal node of the base of the Transconductance amplifier. It is not physically accessible. The base spreading resistance $r_{b'b}$ is represented as a *lumped* parameter between base B and internal node B'. (g_m $V_{b'e}$) is a current generator. $V_{b'e}$ is the input voltage across the emitter junction. If $V_{b'e}$ increases, more carriers are injected into the base of the transistor. So the increase in the number of carriers is α $V_{b'e}$. This results in small signal current (since we are taking into account changes in $V_{b'e}$). This effect is represented by the current generator g_m $V_{b'e}$. This represents the current that results because of changes in $V_{b'e}$, when C is shorted to E.

When the number of carriers injected into the base increase, base recombination also increases. So this effect is taken care of by $g_{b'e}$. As recombination increases, base current increases. *Minority carrier storage* in the *base is represented* by C_e, *the diffusion capacitance*.

According to *Early Effect*, the change in voltage between Collector and Emitter changes the base width. So base width will be modulated according to the voltage between Collector and Emitter. When base width changes, the minority carrier concentration in base changes. Hence the current which is proportional to carrier concentration also changes. So I_E changes and hence I_C changes. This feedback effect [I_E on input side, I_C on output side] is taken into account by connecting $g_{b'c}$ between B', and C. The conductance between Collector and Base is g_{ce}.

C_C represents the collector junction barrier capacitance.

3.2.2 Hybrid - π Parameter Values

Typical values of the hybrid-π parameter at $I_C = 1.3$ mA are as follows :

$g_m = 50$ mA/V	$r_{bb'} = 100\ \Omega$	$r_{b'e} = 1\ k\Omega$
$r_{ce} = 80\ k\Omega$	$C_c = 3$ pf	$C_e = 100$ pf
$r_{b'c} = 4\ M\Omega$		

These values depend upon :

1. Temperature
2. Value of I_C

3.3 Determination of Hybrid-π Conductances

3.3.1 Transconductance or Mutual Conductance (g_m)

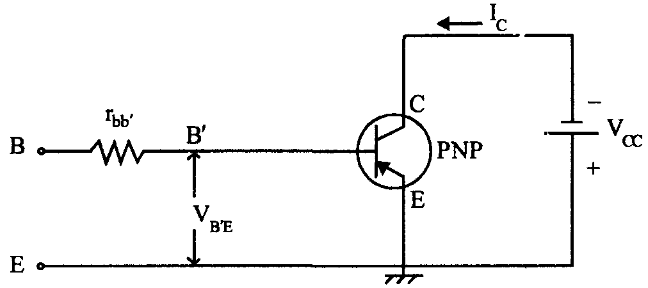


Fig. 3.3 PNP transistor amplifier

The above figure shows PNP transistor amplifier in Common Emitter configuration for AC purpose, Collector is shorted to Emitter.

$$I_C = I_{C0} - \alpha_0 \cdot I_E \qquad .....(1)$$

I_{C0} opposes I_E. I_E is negative. Hence $I_C = I_{C0} - \alpha_0 I_E$ α_0 is the normal value of α at room temperature.

In the hybrid - π equivalent circuit, the short circuit current = $g_m V_{b'e}$

Here only transistor is considered, and other circuit elements like resistors, capacitors etc, are not considered.

$$g_m = \left.\frac{\partial I_C}{\partial V_{b'e}}\right|_{V_{CE} = K}$$

Differentiate (1) with respect to $V_{b'e}$ partially. I_{C0} is constant.

$$\therefore \qquad g_m = 0 - \alpha_0 \frac{\partial I_E}{\partial V_{b'e}} \text{ for a PNP transistor, } V_{b'e} = -V_E$$

Since, for PNP transistor, base is n-type. So negative voltage is given.

$$\therefore \qquad g_m = \alpha_0 \frac{\partial I_E}{\partial V_E}$$

If the emitter diode resistance is r_e, then $r_e = \dfrac{\partial V_E}{\partial I_E}$

$$\therefore \qquad g_m = \frac{\alpha_0}{r_e}$$

But for a diode, $\quad r = \dfrac{\eta . V_T}{I} \qquad \because I = I_0 (e^{V/\eta\, VT} - 1) \quad I \simeq I_0 \cdot e^{V/\eta\, VT}$

$$\left[g = \frac{dI}{dV} = \frac{J_0 . e^{V/\eta V_T}}{\eta . V_T} \cong \frac{I}{\eta V_T} \right]$$

$\therefore \quad r = \dfrac{\eta . V_T}{I} \quad \eta = 1, \qquad I = I_E \qquad r = \dfrac{V_T}{I_E}$

$\therefore \quad g_m = \dfrac{\alpha_0 . I_E}{V_T} \qquad \alpha_0 \simeq 1, \qquad I_E \simeq I_C$

$I_E = I_{C0} - I_C$

$\therefore \quad g_m = \dfrac{I_{C0} - I_C}{V_T}$

Neglecting I_{C0},

$g_m = \dfrac{|I_C|}{V_T} \qquad g_m$ = (Transconductance or Mutual Conductance)

g_m is directly proportional to I_C. g_m is also $\alpha \dfrac{1}{T}$. For PNP transistor, I_C is negative.

$$\therefore \quad \boxed{g_m = \frac{-I_C}{V_T}}$$

will become positive. Since I_C is negative. So g_m is always positive.

V_T is volt equivalent of temperature $V_T = T/11{,}600$

At room temperature, $T \simeq 300$ K,

$g_m = \dfrac{|I_C|}{26}$, I_C is in mA.

If $\quad I_C = 1.3$ mA, $g_m = 0.05$ A/V

If $\quad I_C = 10$ mA, $g_m = 400$ mA/V

3.3.2 Input Conductance ($g_{b'e}$)

At low frequencies, *capacitive reactance* will be *very large* and can be considered as *Open circuit.* So in the hybrid-π equivalent circuit which is valid at low frequencies, all the capacitances can be neglected. The equivalent circuit is as shown in Fig. 3.4.

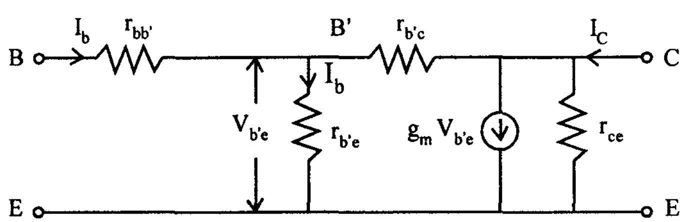


Fig. 3.4 Equivalent circuit at low frequencies

The value of $r_{b'c} >> r_{b'e}$ (Since Collector Base junction is Reverse Biased)

So I_b flows into $r_{b'e}$ only. [This is I_b. $(I_E - I_b)$ will go to collector junction]

$\therefore \quad V_{b'e} \simeq I_b \cdot r_{b'e}$

The short circuit collector current,

$$I_C = g_m \cdot V_{b'e}; \qquad V_{b'e} = I_b \cdot r_{b'e}$$

$$I_C = g_m \cdot I_b \cdot r_{b'e}$$

$$h_{fe} = \left.\frac{I_C}{I_B}\right|_{V_{CE}} = g_m \cdot r_{b'e}$$

or $$\boxed{r_{b'e} = \frac{h_{fe}}{g_m}}$$

But $$g_m = \frac{|I_C|}{V_T}$$

$\therefore$ $$r_{b'e} = \frac{h_{fe} \cdot V_T}{|I_C|}$$

$\therefore$ $$g_{b'e} = \boxed{\frac{|I_C|}{h_{fe} V_T}} \text{ or } \boxed{\frac{g_m}{h_{fe}}}$$

3.3.3 Feedback Conductance ($g_{b'c}$)

h_{re} = reverse voltage gain, with input open or $I_b = 0$

$$= \frac{V_{b'e}}{V_{ce}} = \frac{\text{Input voltage}}{\text{Output voltage}}$$

$$h_{re} = \frac{r_{b'e}}{r_{b'e} + r_{b'c}}$$

[With input open, i.e., $I_b - 0$, V_{ce} is output. So it will get divided between $r_{b'e}$ and $r_{b'c}$ only]

or $$h_{re}(r_{b'e} + r_{b'c}) = r_{b'e}$$

$$r_{b'e}[1 - h_{re}] = h_{re} r_{b'c}$$

But $$h_{re} << 1$$

$\therefore$ $$r_{b'e} = h_{re} \; r_{b'c}; \quad r_{b'c} = \frac{r_{b'e}}{h_{re}}$$

or $$\boxed{g_{b'c} = h_{re} \; g_{b'e}} \quad \frac{1}{r_{b'c}} = g_{b'c} = \frac{h_{re}}{r_{b'e}}$$

$$h_{re} = 10^{-4}$$

$\therefore$ $$r_{b'c} >> r_{b'e}$$

3.3.4 Base Spreading Resistance ($r_{bb'}$)

The input resistance with the output shorted is h_{ie}. If output is shorted, i.e., Collector and Emitter are joined, $r_{b'e}$ is in parallel with $r_{b'c}$.

But we have seen that $r_{b'e} = h_{re} \cdot r_{b'c}$

h_{oe} in very small and $r_{b'c} >> r_{b'e}$

$\therefore$ $r_{b'e}$ is parallel with $r_{b'c}$ is only $r_{b'e}$ (lower value)

$$h_{ie} = r_{bb'} + r_{b'e}$$

or $$\boxed{r_{bb'} = h_{ie} - r_{b'e}}$$

$$h_{ie} = r_{bb'} + r_{b'e}$$

But we know that

$$r_{b'e} = \frac{h_{fe} . V_T}{|I_C|}$$

$$h_{ie} = r_{bb'} + \frac{h_{fe} . V_T}{|I_C|}$$

$r_{bb'}$ is small, few Ωs, to few hundred Ωs

$\therefore$ $$h_{ie} \cong \frac{h_{fe} . V_T}{|I_C|}$$

3.3.5 Output Conductance (g_{ce})

This is the conductance with input open circuited. In h-parameters it is represented as h_{oe}. For $I_b = 0$, we have,

$\therefore$ $$I_C = \frac{V_{ce}}{r_{ce}} + \frac{V_{ce}}{r_{b'c} + r_{b'e}} + g_m \; V_{b'e}$$

But $$h_{re} = \frac{V_{b'e}}{V_{ce}} \qquad \therefore \qquad V_{b'e} = h_{re} . V_{ce}$$

$\therefore$ $$I_C = \frac{V_{ce}}{r_{ce}} + \frac{V_{ce}}{r_{b'c} + r_{b'e}} + g_m . h_{re} . V_{ce}$$

But $$h_{oe} = \frac{I_C}{V_{ce}}$$

So dividing by V_{ce} and that $r_{b'c} >> r_{b'e}$, $r_{b'c} + r_{b'e} \simeq r_{b'c}$

$$\therefore \quad h_{oe} = \frac{1}{r_{ce}} + \frac{1}{r_{b'c}} + g_m \cdot h_{re}$$

$$= g_{ce} + g_{b'c} + g_m\, h_{re}$$

But $$g_{b'e} = \frac{g_m}{h_{fe}}$$

$$\therefore \quad g_m = g_{b'e} \cdot h_{fe}$$

$$h_{re} = \frac{r_{b'e}}{r_{b'e} + r_{b'c}} \approx \frac{r_{b'e}}{r_{b'c}} = \frac{g_{b'c}}{g_{b'e}}$$

$$\therefore \quad h_{oe} = g_{ce} + g_{b'c} + g_{b'e}\, h_{fe} \cdot \frac{g_{b'c}}{g_{b'e}}$$

or $$g_{ce} = h_{oe} - (1 + h_{fe}) \cdot g_{b'c}$$

If $$h_{fe} >> 1, \; 1 + h_{fe} \approx h_{fe}$$

$$\therefore \quad \boxed{\mathbf{g_{ce} = h_{oe} - h_{fe} \cdot g_{b'c}}}$$

But $$g_{b'c} = h_{re} \cdot g_{b'e}$$

$$\therefore \quad g_{ce} = h_{oe} - h_{fe} \cdot h_{re} \cdot g_{b'e}$$

But $$h_{fe} \cdot g_{b'e} = g_m$$

$$\therefore \quad g_{ce} = h_{oe} - g_m \cdot h_{re}$$

3.3.6 Hybrid - π Capacitances

In the hybrid - π equivalent circuit, there are two capacitances, the capacitance between the Collector-Base junction is the C_C or $C_{b'c}$. This is measured with input open i.e., $I_E = 0$, and is specified by the manufacturers as C_{0b}. 0 indicates that input is open. Collector junction is reverse biased.

$$C_C \; \alpha \; \frac{1}{(V_{CE})^n}$$

where $$n = \frac{1}{2} \text{ for abrupt junction}$$

$$= 1/3 \text{ for graded junction.}$$

C_e = Emitter diffusion capacitance C_{De} + Emitter junction capacitance C_{Te}

C_T = Transition capacitance.

C_D = Diffusion capacitance.

$C_{De} >> C_{Te}$

$\therefore \quad C_e \simeq C_{De}$

$C_{De} \propto I_E$ and is independent of Temperature T.

3.3.7 The Diffusion Capacitance

For pnp transistor, base is n-type and emitter is p-type. So if E-B junction is forward biased, holes are injected into the base. The distribution of these injected holes between E and C is as shown.

The collector is reverse biased. So the injected charge concentration p' at the collector junction is zero since they are attracted because of the negative potential at the collector. The base width W is assumed to be small compared to the diffusion length L_S of the minority carriers. If $W << L_B$, then p' varies almost linearly from the value $p'(0)$ at the emitter to zero at the collector. The stored charge in the base is the average concentration $\frac{p'(0)}{2}$ times the volume of the base W_A

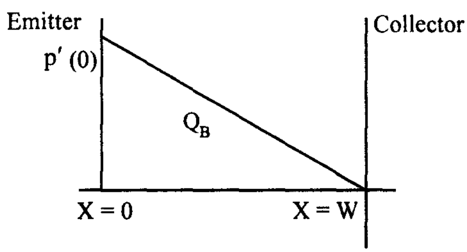


Fig. 3.5 Variation of charge in the base region

(where A is Cross Sectional Area), times charge Q.

W.A = Volume ;

W = Base width ;

A = cross sectional area of the junction.

Q = Charge

$\frac{p'(0)}{2}$ = Average concentration.

Diffusion current $I = -AQ \cdot D_B \cdot \frac{dp'}{dx} = -A\,Q\,D_B \frac{p'(0)}{W}$

D_B = diffusion constant for minority carriers in the base

$$\therefore \quad p'(0) = \frac{I.W}{AQD_B}$$

$$\therefore \qquad Q_B = \frac{1}{2} \times \frac{1 \times W}{AQD_B} . AQW$$

$$Q_B = \frac{W^2}{2D_B}$$

Emitter diffusion capacitance $C_{De} = \dfrac{dQ_B}{dV}$

$$C_{De} = \frac{W^2}{2D_B} . \frac{dI}{dV} = \frac{W^2}{2D_B} . \frac{1}{r_e}$$

But $$r_e = \frac{dV}{dI} = \frac{V_T}{I_E} \quad , \quad I_E = I_0 \left(e^{\frac{V}{\eta V_T}} \right)$$

$$\therefore \qquad \boxed{C_{De} = \frac{W^2 . I_E}{2D_B \, V_T} = g_m . \frac{W^2}{2D_B}}$$

In the above derivation, we have neglected the base width i.e, there is no possibility for recombination in the base hence $I_b = 0$. Then $I_E = I_C$. But actually it cannot be so. Hence, the hybrid-π model is valid only when change in V_{BE} is very small and so change in I_E is equal to change in I_C. i.e., *Hybrid-π model is valid only under dynamic conditions, wherein change in I_B is negligible.* So change in I_E is equal to change in I_C.

Giacoletto who proposed the hybrid - π model, has shown that the hybrid parameters are independent of frequency when

$$2\pi f . \frac{W^2}{6D_B} << 1 \qquad .....(1)$$

Where W = Base width

D_B = Diffusion constant for minority carriers in the base

f = Frequency of the input signal

But $$C_e = g_m . \frac{W^2}{2D_B} \qquad .....(2)$$

$$\frac{C_e}{g_m} = \frac{W^2}{2D_B}$$

$$\therefore \qquad \frac{W^2}{6D_B} = \frac{C_e}{3g_m}$$

$$C_e = \frac{g_m}{2\pi f_T}, \quad \frac{C_e}{g_m} = \frac{1}{2\pi f_T}$$

$\therefore$ $$\frac{W^2}{6D_B} = \frac{1}{6\pi f_T}$$

$\therefore$ Equation becomes, $\dfrac{2\pi f}{6\pi f_T} << 1$

or $f << 3\, f_T$

$\therefore$ *Hybrid π model is valid for frequencies upto $\simeq f_T/3$.*

3.4 Variation of Hybrid Parameters with $|I_C|$, $|V_{CE}|$ and T

3.4.1 Transconductance Amplifier or Mutual Conductance (g_m)

$$g_m = \frac{|I_C|}{V_T}$$

$\therefore$ g_m is $\propto I_C$

$V_T = T/11{,}600$

$\therefore$ $$g_m \propto \frac{1}{T}$$

g_m is independent of V_{CE}

Since in the active region of the transconductance, I_C is independent of V_{CE}.

3.4.2 Base Emitter Resistance ($r_{b'e}$)

$$r_{b'e} = \frac{h_{fe} \cdot V_T}{I_C}$$

$\therefore$ $$r_{b'e} \propto \frac{1}{I_C}$$

*$r_{b'e}$ increases as T increase*s since $r_{b'e} \propto V_T$

3.4.3 Emitter Capacitance (C_e)

$$C_e \simeq g_m \cdot \frac{W^2}{2D_B}$$

$g_m \propto I_C$ $\qquad\qquad$ $\therefore\ C_e \propto I_C$

As V_{Ce} increases, W the effective base width decreases

$\therefore$ *C_e decreases with V_{CE} (increasing)*

3.4.4 Collector Capacitance (C_C)

C_C depends on V_{CE}

$C_c \propto (V_{CE})^{-\eta}$

$\therefore$ *C_C is independent of I_C*

$\therefore$ *C_C is independent of T*

C_C decreases with increase in V_{CE}

3.4.5 Base Spread Resistance ($r_{bb'}$)

$r_{bb'}$ decreases with increase in I_C.

Since as I_C increases, conductivity increases. So $r_{bb'}$ decreases, because of conductivity modulation. But $r_{bb'}$ increases with increase in Temperature. Because as T increases, mobility of the carriers decreases. So conductivity decreases. So $r_{bb'}$ increases.

3.4.6 Collector Emitter Short Circuit Current Gain

Consider a single stage Common Emitter. Transistor amplifier circuit. The hybrid-π equivalent circuit is as shown :

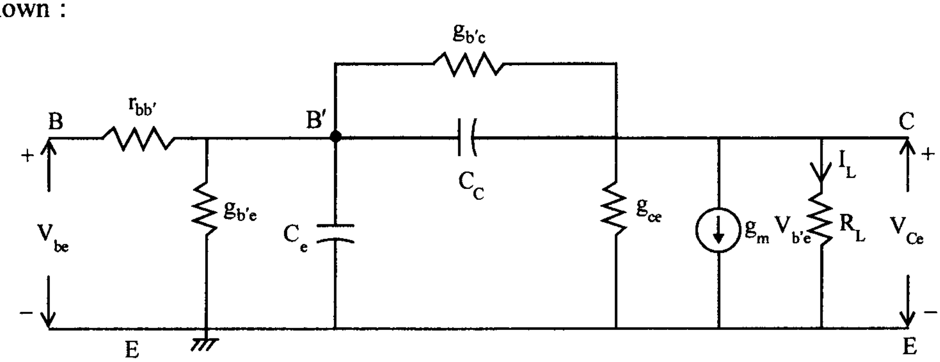


Fig. 3.6 Hybrid - π equivalent circuit in C E configuration

If the output is shorted i.e. $R_L = 0$, what will be the flow response of this circuit ? when $R_L = 0$, $V_0 = 0$. Hence $A_V = 0$. So the gain that we consider here is the current gain $I_L \mid I_C$. The simplified equivalent circuit with output shorted is,

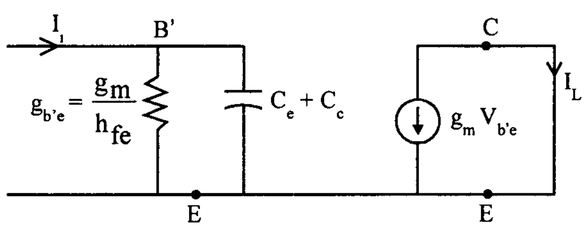


Fig. 3.7 Simplified equivalent circuit

A current source gives sinusoidal current I_C. Output current or load current is I_L. $g_{b'c}$ is neglected since $g_{b'c} << g_{b'e}$, g_{ce} is in shunt with short circuit R = 0. Therefore g_{ce} disappears. The current is delivered to the output directly through C_c and $g_{b'c}$ is also neglected since this will be very small.

$$I_L = -g_m V_{b'e}$$

$$V_{b'e} = \frac{I_i}{g_{b'e} + j\omega(C_e + C_c)}$$

A_i under short circuit condition is,

$$A_i = \frac{I_L}{I_i} = \frac{-g_m}{g_{b'e} + j\omega(C_e + C_c)}$$

But $$g_{b'e} = \frac{g_m}{h_{fe}}, \quad C_e + C_c \simeq C_e$$

$$C_e = \frac{g_m}{2\pi f_T}$$

$$= \frac{-g_m}{\frac{g_m}{h_{fe}} + \frac{j\,2\pi . g_m . f}{2\pi f_T}}$$

$\therefore$ $$A_i = \frac{-1}{\frac{1}{h_{fe}} + j\left(\frac{f}{f_T}\right)}$$

$$= \frac{-h_{fe}}{1 + j\,h_{fe}\left(\frac{f}{f_T}\right)}$$

$$A_i = \frac{-h_{fe}}{1 + j\left(\frac{f}{f_\beta}\right)}$$

But, $$\frac{f_T}{h_{fe}} = f_\beta$$

$\therefore$ $$|A_i| = \frac{h_{fe}}{\sqrt{1 + \left(\frac{f}{f_\beta}\right)^2}}$$

Where $$f_\beta = \frac{g_{b'e}}{2\pi(C_e + C_C)}$$

$$g_{b'e} = \frac{g_m}{h_{fe}}$$

$\therefore$ $$f_\beta = \frac{g_m}{h_{fe}\, 2\pi(Ce + C_c)}$$

At $f = f_\beta$, $A_i = \frac{1}{\sqrt{2}} = 0.707$ of h_{fe}.

The frequency range upto f_β *is referred to as the Bandwidth of the circuit.*

Note : *Common Emitter short circuit current gain was skipped out.*

3.5 The Parameters f_T

f_T is the frequency at which the short circuit Common Emitter current gain becomes unity.

i.e., $$A_i = 1, \quad \text{or} \quad \frac{h_{fe}}{\sqrt{1 + \left(\frac{f_T}{f_\beta}\right)^2}} = 1$$

Let at $f = f_T$, $A_i = 1$

or $$h_{fe} = \sqrt{1 + \left(\frac{f_T}{f_\beta}\right)^2}$$

$$(h_{fe})^2 = 1 + \left(\frac{f_T}{f_\beta}\right)^2 \cong \left(\frac{f_T}{f_\beta}\right)^2$$

$\therefore$ $$h_{fe} \simeq \frac{f_T}{f_\beta} \text{ when } Ai = 1$$

$\therefore$ $$\boxed{f_T \simeq h_{fe} \cdot f_\beta}$$

But $$f_\beta = \frac{g_m}{h_{fe}\{C_e + C_c\}}$$

$\therefore$ $$f_T = f_\beta \cdot h_{fe} = \frac{g_m}{2\pi(C_e + C_c)}$$

But $C_e >> C_c$

$\therefore$ $$\boxed{f_T \simeq \frac{g_m}{2\pi Ce}}$$

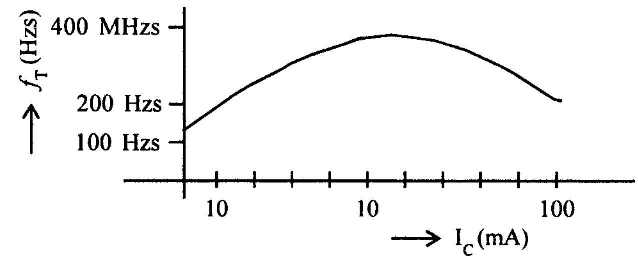


Fig. 3.8 Variation of I_C with frequency

f_T is very important parameter of the transistor. This indicates the high frequency performance of the transistor. f_T depends upon the operating point of the transistor. The variations of f_T with I_c is as shown,

$$f_T = h_{fe} \cdot f_\beta$$

h_{fe} is the short circuit current gain.

f_β is the frequency.

Therefore f_T is the short circuit current gain Bandwidth product. So if we have two transistors with same f_T, the transistor with low h_{fe} will have larger Bandwidth and vice versa.

3.5.1 Measurement of f_T

The value of f_T is very large of the order of *few hundred MHz*. To determine the f_T of a given transistor, we need CRO whose frequency range is of that order. Such a CRO is not common. So how to determine f_T with a practically available CRO which can respond upto any few MHz ?

$$A_i = \frac{h_{fe}}{\left[1+\left(\frac{f}{f_\beta}\right)^2\right]^{1/2}} ; \left(\frac{f}{f_\beta}\right)^2 >> 1$$

$$\therefore \qquad A_i = \frac{h_{fe}}{\sqrt{\left(\frac{f}{f_\beta}\right)^2}} = \frac{f_\beta . h_{fe}}{f}$$

$$\therefore \qquad |A_i|\ f \simeq f_\beta \cdot h_{fe} = f_T$$

If we determine A_i of the transistor at a frequency *f which is 3 or 4 times* f_β but much smaller than f_T, *the product of* A_i and f gives the value of f_T.

For a transistor with f_T = 80 MHz and f_β = 1.6 MHzs, the frequency f at which A_i is determined can be 5 times $f_\beta \doteq$ 8.0 MHz maximum. We can have CRO which can respond at 8 MHz but not 80 MHzs. Therefore f_T can be easily determined by measuring A_i at f = 8 MHz.

3.6 Expression for f_β

$$A_i = \frac{-g_m}{g_{b'e} + j\omega(C_e + C_c)}$$

Dividing by $g_{b'e}$, Numerator and Denominator,

$$A_i = \frac{-g_m / g_{b'e}}{1 + \frac{j2\pi f(C_e + C_c)}{g_{b'e}}}$$

we know that $g_{b'e} = \frac{g_m}{h_{fe}}$

$$\therefore \quad \frac{g_m}{g_{b'e}} = h_{fe}$$

$$A_i = \frac{-h_{fe}}{1 + jf\left[\frac{2\pi(C_e + C_c)}{g_{b'e}}\right]}$$

But we know that $A_i = \frac{-h_{fe}}{1 + j\frac{f}{f_\beta}}$

Comparing, $f_\beta = \frac{g_{b'e}}{2\pi(C_e + C_c)} = \frac{g_m}{h_{fe}.2\pi(C_e + C_c)} \quad \because \quad g_{b'e} = \frac{g_m}{h_{fe}}$

$$\therefore \quad \boxed{f_\beta = \frac{g_m}{h_{fe}.2\pi(C_e + C_c)}}$$

$$\boxed{f_T = \frac{g_m}{2\pi(C_e + C_c)}}$$

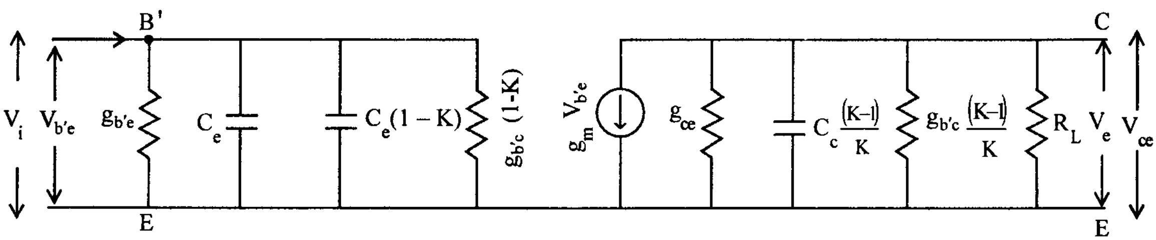


Fig. 3.9 Equivalent circuit

3.7 Current Gain with Resistance Load :

$$f_T = f_\beta \cdot h_{fe} = \frac{g_m}{2\pi\left(C_e + C_c\right)}$$

Considering the load resistance R_L,

$V_{b'e}$ is the input voltage and is equal to V_1

V_{ce} is the output voltage and is equal to V_2

$$K_2 = \frac{V_{ce}}{V_{b'e}}$$

This circuit is still complicated for analysis.

Because, there are two time constants associated with the input and the other associated with the output. The output time constant will be much smaller than the input time constant. So it can be neglected.

K = Voltage gain. It will be >> 1

$$\therefore \qquad g_{b'c}\left(\frac{K-1}{K}\right) \simeq g_{b'c}$$

$g_{b'c} < g_{ce} \quad \because \quad r_{b'c} \simeq 4\ \text{M}\Omega, \qquad r_{ce} = 80\ \text{K}$ (typical values)

So $g_{b'c}$ can be neglected in the equivalent circuit.

In a wide band amplifier R_L will not exceed 2KΩ, since $f_H \propto \frac{1}{R_L}$. If R_L is small f_H is large.

$$f_H = \frac{1}{2\pi C_S\left(R_C \parallel R_L\right)}$$

Therefore g_{ce} can be neglected compared with R_L

Therefore the output circuit consists of current generator gm $V_{b'e}$ feeding the load R_L so the Circuit simplifies as shown in Fig. 3.10.

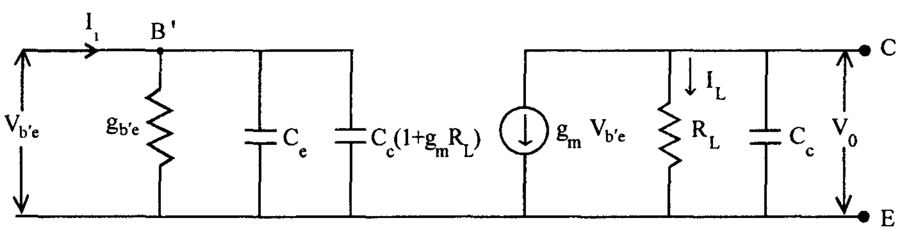


Fig. 3.10 Simplified equivalent circuit

$$K = \frac{V_{ce}}{V_{b'e}} = -g_m R_L; \qquad g_m = 50\ \text{mA\V}, \qquad R_L = 2\text{K}\Omega \text{ (typical values)}$$

$$K = -100$$

So the maximum value is $g_{b'c}(1-K) \simeq 0.02595$. So this can be neglected compared to $g_{b'e} \simeq 1$ mA/V.

R_L should not exceed 2KΩ, therefore if R_L > 2KΩ, C_c (1 + g_m R_L) becomes very large and so band pass becomes very small.

$$C_c = \left[\frac{K-1}{K}\right] \simeq C_c$$

when $\qquad R_L = 2K\Omega,$

the output time constant is,

$$R_L \cdot C_c = 2 \times 10^3 \times 3 \times 10^{-12} = 6 \times 10^{-9}\ S = 6\ \mu.sec. \text{ (typical values)}$$

Input time constant is,

$$r_{b'e}\ [C_e + C_c\,[1 + g_m R_L]] = 403\ \mu.sec. \text{ (typical values)}$$

So the band pass of the amplifier will be determined by the time constant of the input circuit.

The 3db frequency $f_M = \dfrac{1}{2\pi r_{b'e} C} = \dfrac{g_{b'e}}{2\pi C}$

where $\qquad C = C_e + C_c\,(1 + g_m R_L)$

3.8 Miller's Theorem

It states that if an impedance Z is connected between the input and output terminals, of a network, between which there is voltage gain, K, the same effect can be had by removing Z and connecting an impedance Z_i at the input = $\dfrac{Z}{(1-K)}$, and Z_0 across the output = $\dfrac{ZK}{(K-1)}$.

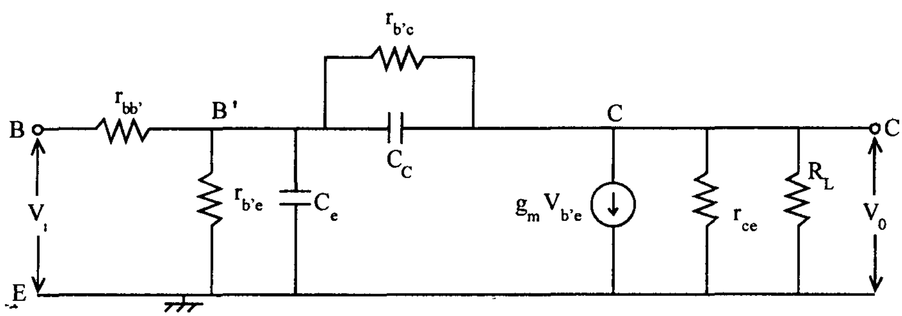


Fig. 3.11 High frequency equivalent circuit with resistive load R,

$$C_{b'c} = C_c$$

$r_{b'c}$ and C_c are between the input termed B' and output termed C. The voltage gain of the amplifier = $\dfrac{V_{ce}}{V_{b'e}}$ = K (> > 1). Therefore by Miller's theorem, C_c and $r_{b'c}$ can be connected between B' and E (input side) with values = $\dfrac{C_C}{1-K}$ and $r_{b'c}$ (1 – K) respectively. On the output side between collector and emitter as $C_C\dfrac{(K-1)}{K}$ and $\dfrac{r_{b'c} \cdot K}{(K-1)}$ resting .

Therefore high frequency equivalent circuit using Miller's theorem reduces to, (neglecting $r_{bb'}$)

$$K = \frac{V_{ce}}{V_{b'e}}$$

$V_{ce} = -I_C \cdot R_L$; Negative is used since current direction is opposite.

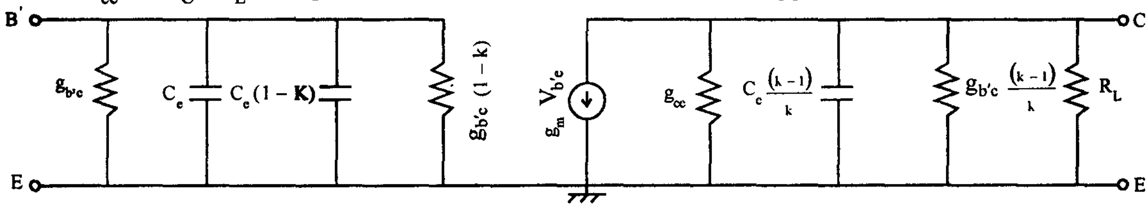


Fig. 3.12 Circuit after applying Millers' Theorem

$$K = \frac{-I_C.R_L}{V_{b'e}}$$

But $$\frac{I_C}{V_{b'e}} = g_m$$

$\therefore$ $$K = -g_m \cdot R_L$$

3.9 CE Short Circuit Current Gain

This is the circuit of transistor amplifier in common emitter configuration.

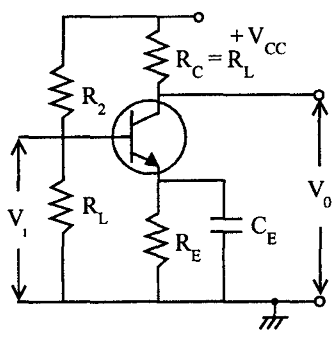


Fig. 3.13 C E Amplifier circuit

The approximate equivalent circuit at high frequencies, with output shorted is,

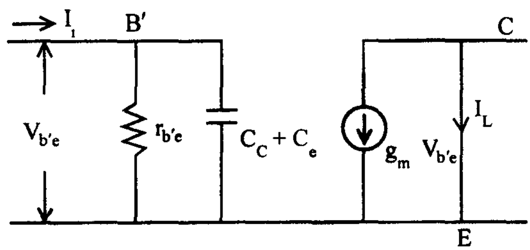


Fig. 3.14 Simplified equivalent circuit

$r_{b'e}$ is assumed to be very large. So it is open circuit.

r_{ce} disappears since it is in shunt with short circuited output.

$$I_L = -g_m \; V_{b'e}$$

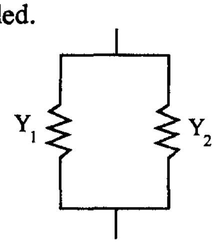
Negative sign taking the direction of current into acount. I_L is contributed by the current source only.

$$V_{b'e} = I \times Z \quad = I \times \frac{1}{Y}$$

$$V_{b'e} = \frac{I_i \times 1}{g_{b'e} + j\omega C_e}$$

$$\therefore \qquad I_L = \frac{-g_m \cdot I_i}{g_{b'e} + j\omega C_e}$$

Conductances in parallel get added.



$Y = Y_1 + Y_2$

Fig. 3.15 Conductances in parallel

Therefore current gain under short circuit conditions is,

$$A_i = \frac{I_L}{I_i} = \frac{-g_m}{g_{b'e} + j\omega C_e}$$

But

$$g_{b'e} = \frac{g_m}{h_{fe}}$$

$$C_e = \frac{g_m}{2\pi f_T}$$

$$\therefore \qquad A_i = \frac{I_L}{I_i} = \frac{-g_m}{\frac{g_m}{h_{fe}} + \frac{j\omega g_m}{2\pi f_T}}$$

$$\therefore \qquad A_i = \frac{-1}{\frac{1}{h_{fe}} + \frac{j2\pi f}{2\pi f_T}} = \frac{-h_{fe}}{1 + \frac{jh_{fe} \cdot f}{f_T}}$$

$$\frac{f_T}{h_{fe}} = f_\beta$$

$$\therefore \qquad \boxed{A_i = \frac{-h_{fe}}{1 + j\left(\frac{f}{f_\beta}\right)}}$$

when $f = f_\beta$, A_i falls by $\frac{1}{\sqrt{2}}$, or by 3db. The frequency range f_β is called Bandwidth of the amplifiers.

$\therefore$ f_β : Is the frequency at which the short circuit gain in common emitter configuration falls by 3 db.

f_T : This is defined as the frequency at which the common emitter shunt circuit current gain becomes 1.

$$A_i = \frac{-h_{fe}}{1 + j\left(\frac{f}{f_\beta}\right)}$$

Let $\qquad f = f_T, \qquad A_i = 1$

$$\therefore \qquad 1 = \frac{h_{fe}}{\sqrt{1 + \left(\frac{f_T}{f_\beta}\right)^2}}$$

$$\therefore \qquad 1 + \left(\frac{f_T}{f_\beta}\right)^2 = h_{fe}^2$$

$$\left(\frac{f_T}{f_\beta}\right)^2 = h_{fe}^2 - 1 \simeq h_{fe}^2 \qquad \because h_{fe} >> 1.$$

$$\therefore \qquad \boxed{f_T = f_\beta \cdot h_{fe}}$$

f_β is the Bandwidth of the transistor

h_{fe} is the current gain

$\therefore$ f_T is the current gain, Bandwidth product.

In Common Emitter configurations, $A_i >> 1$. But as frequency increases A_i falls. Why should A_i decrease ? $A_i = \frac{I_L}{I_i}$. As frequency increases, X_c increases. So, X_e increases. i.e., more and more number of carriers will be stored in the base region itself. Due to this, less number of carriers will reach collector. Storage of carriers at the base and emitter increases. So I_C decreases. Therefore I_L decreases i.e., g_m decreases. So $g_m V_{b'e}$ decreases or I_L decreases. Hence A_i decreases.

f_T depends on the operating point of the transistor. The graph of f_T V_s I_c for a transistor is as shown,

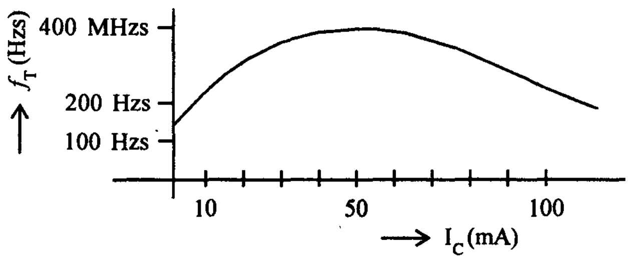


Fig. 3.16 Variation of I_C with frequency

For a typical transistor, $f_T = 80$ MHz

$f_\beta = 1.6$ MHz

Example : 3.1

Given a Germanium PNP transistor whose base wiuth is 10^{-4} cm. At room temperature and for a DC Emitter current of 2mA, find,

(a) Emitter diffusion capacitance

(b) f_T

Solution :

Given $D_B = 47$

$C_e \simeq C_{De}$ $\quad \because$ C_T is negligible,

$$\simeq g_m \frac{W^2}{2D_B}$$

But $g_m = \frac{|I_C|}{V_T}$ $\quad I_c \simeq I_E$

$$\therefore \quad C_e = \frac{I_E}{V_T} \times \frac{W^2}{2D_B}$$

$$= \frac{2\times10^{-3}\times10^{-8}}{26\times10^{-3}\times2\times47}$$

$$= 8.2 \text{ pf.}$$

$$f_T = \frac{g_m}{2\pi C_e}$$

$$= \frac{I_E}{V_T \cdot 2\pi C_e}$$

$$= 1500 \text{ MHz}$$

Example : 3.2

Given the following transistor measurements made at $I_C = 5$ mA ; $V_{CE} = 10$V and at room temperature $h_{fe} = 100$; $h_{ie} = 600\Omega$; $[A_{ie}] = 10$ at 10 MHz $C_c = 3$ pf.

Find f_β, f_T, C_e, $r_{b'e}$ and $r_{bb'}$.

Solution :

$$|A_{ie}| = \left| \frac{-h_{fe}}{1 + j\frac{f}{f_\beta}} \right| = \frac{h_{fe}}{\sqrt{1 + \left(\frac{f}{f_\beta}\right)^2}}$$

$$h_{fe} = 100, \quad A_{ie} = 10, \text{ at } f = 10 \text{ MHz}$$

$$\therefore \quad 10 = \frac{100}{\sqrt{1 + \left(\frac{f}{f_\beta}\right)^2}}$$

$$1 + \left(\frac{f}{f_\beta}\right)^2 = \frac{100 \times 100}{10 \times 10} = 100$$

$$\left(\frac{f}{f_\beta}\right)^2 = 100 - 1 = 99$$

$$\left(\frac{f}{f_\beta}\right)^2 = 99, \quad f = 10 \text{ MHz for use,}$$

$$\boxed{\therefore \ f_\beta = 1.005 \text{ MHz}}$$

$$f_T = h_{fe} \cdot f_\beta = 100 \times 1.005 \text{ MHz} = 100.5 \text{ MHz}$$

$$C_e = \frac{g_m}{2\pi f_T}; \quad g_m = \frac{|I_c|}{V_T}$$

$$\therefore \qquad C_e = \frac{|I_C|}{V_T.2\pi f_T}$$

$$C_e = \frac{5\times10^{-6}}{26\ 2\pi\times100.5} = 304\text{ pf}$$

$$r_{b'e} = \frac{h_{fe}}{g_m} = \frac{100}{5/26} = 520\Omega$$

$$r_{bb'} = h_{ie} - r_{b'e} = 600 - 520 = 80\Omega$$

Example : 3.3

A single stage Common Emitter amplifier is measured to have a voltage-gain bandwidth f_H of 5 MHzs with $R_L = 500\ \Omega$. Assume $h_{fe} = 100$, $g_m = 100$ mA/V, $r_{bb'} = 100\Omega$, $C_c = 1$ pf, and $f_T = 400$ MHzs.

Find the value of the source resistance that will give the required bandwidth.

Solution :

$$C_e = \frac{g_m}{2\pi f_T} = \frac{100\times10^{-3}}{628\times400\times10^6} = 0.0405\times10^{-9}\text{ Farads}$$

$$r_{b'e} = \frac{h_{fe}}{g_m} = 1\text{K}\ \Omega$$

$$C = C_e + C_c\,(1 + g_m R_L)$$

$$= 40 + 1\,(1 + 100\times10^{-3}\times\frac{1}{2}\times10^3) = 91\text{ pf}$$

Bandwidth $\simeq f_H$ since f_L is very small

$$f_H = \frac{1}{2\pi RC}$$

where $\quad R = R_S' \parallel r_{b'e}$ and $R_S' = R_S + r_{bb'}$

$$\therefore \qquad R = \frac{1}{2\pi f_H.C} = \frac{1}{6.28\times5\times10^6\times91\times10^{-12}}$$

$$= 0.35\times10^3 = 350\Omega$$

$$\therefore \qquad \frac{R_S'\times r_{b'e}}{R_S'+r_{b'e}} = 350\Omega\ ; \qquad r_{b'e} = 1\text{K}\Omega$$

$$\therefore \qquad R_S' = 539\Omega$$

$$\therefore \qquad R_S = R_S^1 - r_{bb'} = 539 - 100 = 439\Omega$$

Example : 3.4

Show that at low frequencies, the hybrid π - model with $r_{b'c}$ and r_{ce} taken as infinite reduces to the approximate CE h-parameter model.

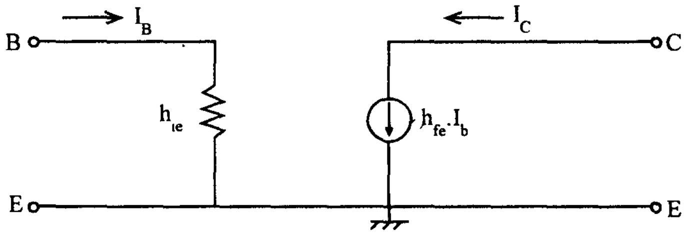


Fig. 3.17 Circuit diagram for Ex.3.4

Solution :

The h-parameters equivalent circuit in Common Emitter configuration is as shown in Fig. 1.49. We have to show that the hybrid π equivalent circuit will also be the same with the approximation given in the problem.

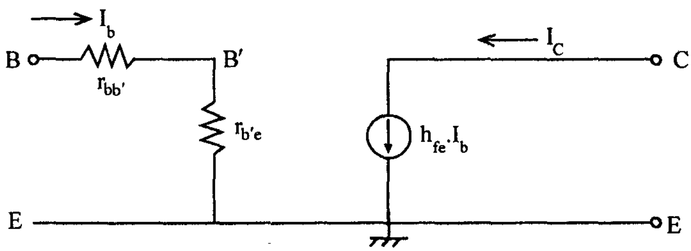


Fig. 3.18 Simplified circuit

If the expressions for the output current I and input impedance h_{ie} are same in the hybrid π equivalent circuit and h-parameter equivalent circuit, we can say that both the circuits are identical.

This is the hybrid - π equivalent circuit neglecting capacitances

$r_{b'e} = r_{ce} = \infty$ (since at low f, they are ∞).

$I = g_m \cdot V_{b'e}$;

$V_{b'e} = I_b \cdot r_{b'e}$

$\therefore$ $I = g_m \cdot I_b \cdot r_{b'e}$

we know that $r_{b'e}\, g_m = h_{fe}$ [in the derivation of $g_{b'e}$]

$\therefore$ $I = h_{fe} \cdot I_b$ [which is the same as in h-parameters circuit]

$h_{ie} = r_{bb'} + r_{b'e}$

Example : 3.5

The following low frequency parameters are known for a given transistors at I_C = 10 mA, V_{ce} = 10v and at room temperature $h_{ie} = 500\Omega$, $h_{oe} = 10^{-5}$ A/V, $h_{fe} = 100$, $h_{re} = 10^{-4}\mho$.

At the same operating point, f_T = 50 MHz, and C_{ob} = 3 pf, compute the values of all the hybrid - π parameters.

Solution :

$$g_m = \frac{|I_C|}{V_T} = \frac{10\,mA}{26\,mV} = 385 \text{ mA/V}$$

$$r_{b'e} = \frac{h_{fe}}{g_m} = \frac{100}{0.385} = 260\Omega$$

$$r_{bb'} = h_{ie} - r_{b'b} = 500 - 260 = 240\Omega$$

$$r_{b'c} = \frac{r_{b'e}}{h_{re}} = 260 \times 10^4 = 2.6 \text{ M}\Omega$$

$$g_{ce} = h_{oe} - (1 + h_{fe})\, g_{b'c}$$

$$= 4 \times 10^{-5} - \frac{101}{2.6\times10^6} = 0.120 \times 10^6$$

$$r_{ce} = \frac{1}{g_{ce}} = 833\text{K}\Omega$$

$$C_e = \frac{g_m}{2\pi f_T} = \frac{385\times10^{-3}}{2\pi\times50\times10^6} = 1224 \text{ pf}$$

$$C_c = 3 \text{ pf}$$

Example : 3.6

A single stage Common Emitter amplifier is measured to have a voltage gain bandwidth **product** f_H of 5 MHzs, with $R_L = 500\Omega$. Assume $h_{fe} = 100$, $g_m = 100$ mA/V, $r_{bb'} = 100\Omega$, $C_c = 1$ pf and $f_T = 400$ MHzs.

(a) Find the value of R_S that will give the required Bandwidth.

(b) With the value of R_S, determined in part (a), find the midband voltage gain V_0/V_S.

Solution :

$$C_e = \frac{g_m}{2\pi f_T} = \frac{100\times10^{-3}}{6.28\times400\times10^8} = 0.0405 \times 10^{-9} \text{ Farads}$$

$$r_{b'e} = \frac{h_{fe}}{g_m} = 1\text{K}\Omega$$

$$C = C_e + C_c\,(1 + g_m R_L) = 40 + 1\,(1 + 100 \times 10^{-3} \times \frac{1}{2} \times 10^3) = \mathbf{91\ pf}$$

Let $R_S{}'$ = total input resistance $= R_S + r_{bb'}$; R_S is the resistance of the source.

Let R be the equivalent input resistance $= R_S{}^1 \parallel r_{b'e}$

$$f_H = \text{Higher cut off frequency}$$

$$= \frac{1}{2\pi RC}$$

$$\therefore \qquad R = \frac{1}{2\pi f_H.C} = \frac{1}{2\times\pi\times5\times10^6\times91\times10^{-12}} = 0.35 \times 10^3 = 350\Omega$$

$$\therefore \qquad \frac{R'_S \times r_{b'e}}{R'_S \times r_{b'e}} = 350\Omega \; ; \; R_S{}^1 = 539\Omega \; ; \quad R_S = R_S{}^1 - r_{bb'} = 439\Omega$$

$$A_v \text{ in the midband region} = \frac{g_m R_L.G_S}{G'_S + g_{b'e}}; \quad G'_S = \frac{1}{R^1_S}$$

$$A_{VS} = -32.5$$

Redraw the Common Emitter hybrid-π equivalent circuit with the base as the common terminal and the output terminals, collectors and base short circuited.

Common Emitter Hybrid-π Equivalent Circuit

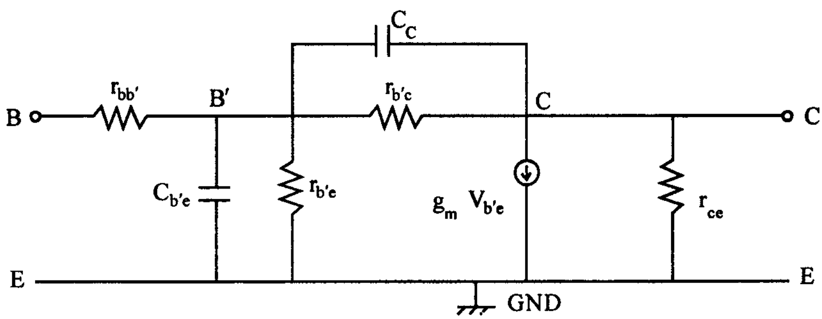


Fig. 3.19 CE Hybrid - π equivalent circuit

The base should be common terminal. So draw a line between base B and B'. We have $r_{bb'}$. So draw another line to indicate B'. Between B' and E, we have $C_{b'e}$ parallel with $r_{b'e}$. So draw these two in parallel and indicate point E. E and B are input points. C and B are output points. Between B' and C, we have $C_{b'e}$ and $r_{b'c}$. So draw these two in parallel and indicate the point at Collector. Between

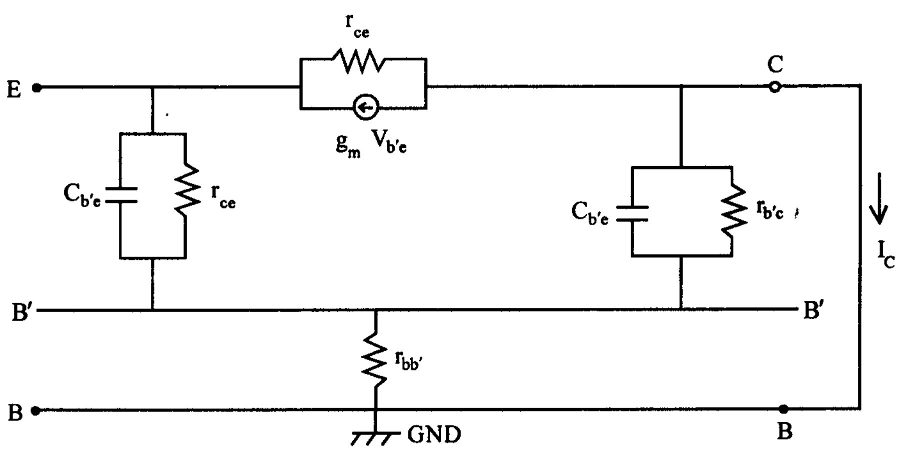


Fig. 3.20 With $r_{bb'}$, terminals B' and B shown separately

Collector and Emitter we have $g_m V_{b'e}$ in parallel with r_{ce}. So indicate these two between Emitter and Collector output terminals. Base and Collector are to be shorted. So short Collector and Base terminals. Therefore the voltage drop across the resistor

$$= R \times I = 24\ K\Omega \times 100\ mA$$

$$= 2400 \text{ volts !}$$

A very large value

DC powers dissipation $= I_{DC}^2 R = (100 \times 10^{-3})^2 \times 24 \times 10^3$

$$= 240000 \times 10^{-3}$$

$$= 240\ W$$

Such a resistor cannot be easily obtained. Hence replacing L by equivalent R can be done only when the output current is small.

3.10 Hybrid - π (pi) Parameters

To analyse the behaviour of transistor at high frequencies, a model based upon transmission line equation will be accurate. But the resulting circuit becomes very complicated. By making approximations, it becomes simple, but the analysis may not be accurate. So hybrid-π model is a compromise between the two.

3.10.1 Hybrid - π Common Emitter Model

Common Emitter model which is valid at high frequencies is called hybrid-π or Giacoletto model. It is as shown in Fig. 3.21.

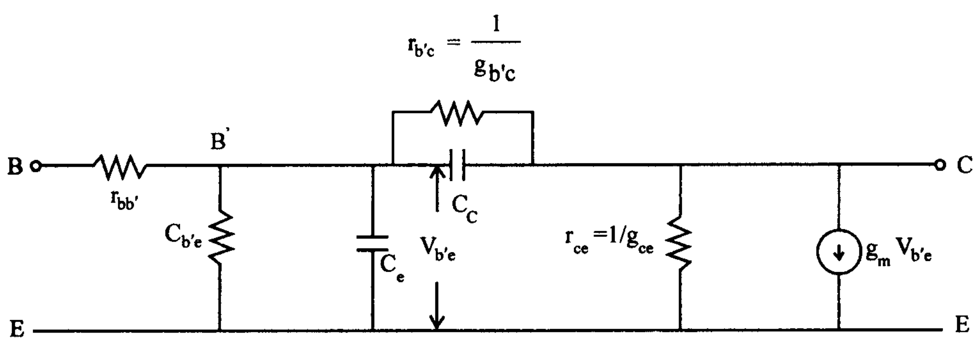


Fig. 3.21 Hybrid - π - C E Model

C_e = Diffusion Capacitance or Emitter Capacitance.

$r_{bb'}$ = Base spreading Resistance

$g_m V_{b'e}$ = current source

$g_{b'e}$ = conductance

C_c = collector junction barrier capacitance.

By analyzing the circuit we get results which will agree with practical results at all frequencies. *All the hybrid - π parameters are assumed to be independent of frequency.*

3.10.2 Discussion

Node B' is not accessible $r_{bb'}$ is base spreading resistance. Excess-minority carrier concentration injected into the base is proportional to $V_{b'e}$. So the small signal collector current with the collector shorted to the emitter is proportional to $V_{b'e}$. This effect accounts for the current generator $g_m V_{b'e}$. The increase in minority carriers in the base results in increased base current. This is taken into account by the conductance $g_{b'e}$ between B' and E. The excess minority carriers stored in the base is accounted for by the diffusion capacitance C_e. The feedback effect between input and output is taken into account by conductance $g_{b'c}$. C_c is collector junction barrier capacitance. Typical values of hybrid - π parameters are for I_c = 1.3 mA at room temperature :

g_m = 50 mA/V, $r_{bb'}$ = 100 Ω, $r_{b'e}$ = 1KΩ, C_e = 100 pf, C_c = 3 pf, r_{ce} = 80 KΩ

3.10.3 Transconductance : g_m

I_{C0} = Reverse saturation current.

Figure shows PNP transistor in CE configuration. Collector current $I_C = I_{C0} - \alpha_0 I_E$.

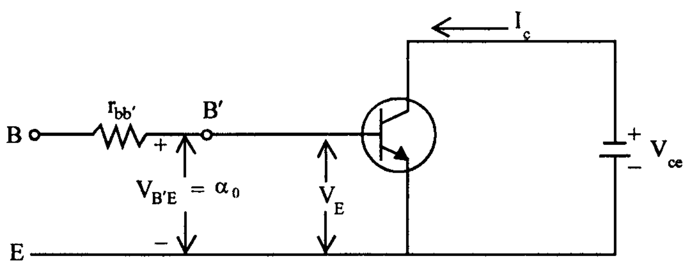


Fig. 3.22 PNP transistor circuit in CE configuration

$$\text{Transconductance} \quad g_m = \left.\frac{\partial I_C}{\partial V_{B'E}}\right|_{V_{CE}=K} = \alpha_0 \frac{\partial I_E}{\partial V_{B'E}} = +\alpha_0 \frac{\partial I_C}{\partial V_E} \quad \text{for PNP transistor.}$$

$V_E = V_{B'E}$ as shown in the above Fig. 3.22.

If the emitter diode resistance is r_e, then $r_e = \partial V_E | \partial I_E$

$$\therefore \qquad g_m = \frac{\alpha_0 - I_E}{V_T} = \frac{I_{C0} - I_C}{V_T} \qquad V_T = \text{voltage equivalent of temperature}$$

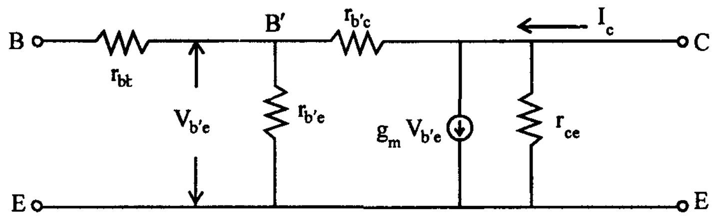
$$|I_c| >> I_{C0} \qquad \therefore\ g_m \sim \frac{|I_C|}{V_T}; \quad V_T = \frac{T}{11{,}600}$$

Since g_m, I_E depend on temperature. For PNP transistor, I_C is negative, for NPN I_C is positive.

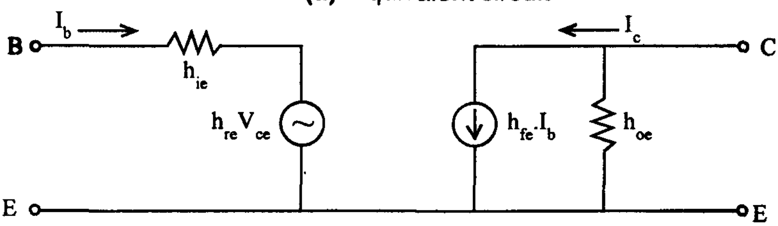
3.10.4 Input Conductance $g_{b'e}$

Fig. 3.23 (a) shows hybrid-π model valid at low frequency. Neglecting all the capacitances, Fig. 3.23 (b) shows the same using h-parameter equivalent circuit.

$$r_{b'e} >> r_{b'e} \qquad \therefore\ I_b \text{ flows into } r_{b'e} \qquad \therefore\ V_{b'e} \simeq I_b \cdot r_{b'e}$$



(a) Equivalent circuit



(b) Simplified circuit

Fig. 3.23

Short circuit collector current $I_c = g_m V_{b'e} \sim g_m I_b r_{b'e}$

Short circuit current gain $h_{fe} = \left.\dfrac{I_c}{I_b}\right|_{V_{CE}} = g_m r_{b'e}$

or $$r_{b'e} = \frac{h_{fe}}{g_m} = \frac{h_{fe} V_T}{|I_C|} \quad \text{or} \quad g_{b'e} = \frac{g_m}{h_{fe}}$$

$r_{b'e}$ is directly proportional to temperature and inversely proportional to current.

3.10.5 Feedback Conductance : $g_{b'c}$

With the input open circuited, h_{re} is defined as the reverse voltage gain. From Fig. 3.24(b), with $I_b = 0$,

$$h_{re} = \frac{V_{b'e}}{V_{ce}} = \frac{r_{b'e}}{r_{b'e} + r_{b'c}}$$

or $$r_{b'e} (1 - h_{re}) = h_{re} r_{b'c}$$

But $$r_{b'e} << 1, \quad r_{b'e} = h_{re} r_{b'c}$$

or $$g_{b'c} = h_{re} g_{b'e}$$

Identification of leads :

Transistor when held with leads upwards E is on left half side. The upper half semicircle is emitter.

Transistor case

Diode lead identifiation

Fig. 3.24 BJT and diode devices

$$h_{ie} = \text{Input } Z = \left.\frac{V_e}{I_e}\right| \text{ output shorted}$$

$$h_{oe} = \text{output admittance } \left.\frac{I_C}{V_C}\right| \text{ input open}$$

$$h_{re} = \text{reverse voltage d.c gain} = V_{b'e}\ V_{ce}$$

$$h_{fe} = \text{forward current gain} = \left.\frac{I_c}{I_B}\right| V_{ce} = k$$

3.10.6 Base Spreading Resistance $r_{bb'}$

The input resistance with the output shorted is h_{ie}. Under these conditions, $r_{b'e}$ is in parallel with $r_{b'c}$.

But $g_{b'c} = h_{re}\ g_{b'e}$ Since $r_{b'e} >> r_{b'e}$ Therefore Parallel combination

$$r_{b'e} \parallel r_{b'c} \sim r_{b'e}$$

$\therefore$ $h_{ie} = r_{bb'} + r_{b'e}$ or $r_{bb'} = h_{ie} - r_{b'e}$

$$h_{ie} = r_{bb'} + \frac{h_{fe} V_T}{(I_C)} \approx \frac{h_{fe} V_T}{|I_C|}$$

3.10.7 Output Conductance g_{ce}

With the input open circuited, the conductance is defined as h_{oe} for $I_b = 0$,

$$I_C = \frac{V_{ce}}{r_{ce}} + \frac{V_{ce}}{r_{b'c} + r_{b'c}} + g_m\ V_{b'e}$$

$$h_{re} = V_{b'e} | V_{ce} \qquad \therefore\ V_{b'e} = h_{re} V_{ce}$$

But $$h_{oe} = \frac{I_C}{V_C} = \frac{1}{r_{ce}} + \frac{1}{r_{b'c}} + g_m\ h_{re}$$

By substituting the equation $g_{b'e} = \dfrac{g_m}{h_{fe}}$, $g_{b'c} = h_{re}\ g_{b'e}$ above,

$$h_{oe} = g_{ce} + g_{bc} + g_{b'e}\ h_{fe}\ \frac{g_{b'c}}{h_{fe}}$$

or $g_{ce} = h_{oe} - (1 + h_{fe})\ g_{b'c}$.

If $h_{fe} >> 1, (1 + h_{fe}) \simeq h_{fe}$

$\therefore$ $g_{ce} = h_{oe} - h_{fe}\ g_{b'c}$

But $g_{b'c} = h_{re} \cdot g_{b'e}$

$\therefore$ $g_{ce} = h_{oe} - h_{fe}\ h_{re} \cdot g_{b'e}$

But $h_{fe} \cdot g_{b'e} = g_m$

$\therefore$ $\boxed{g_{ce} = h_{oe} - g_m \cdot h_{re}}$

3.10.8 Hybrid - π Capacitances

The hybrid - π model consists of two capacitances C_c and C_e.

C_c : The collector junction capacitance $C_c = C_{b'c}$. It is usually specified as C_{ob} by the manufacturers. In the active region, collector junction is reverse biased, C_c is the transition capacitance and varies as $(V_{CE})^{-n}$ where η is $\frac{1}{2}$ or $\frac{1}{3}$, for abrupt or graded junction.

C_e : It represents the sum of emitter diffusion capacitance C_{De} and emitter junction capacitance C_{Te}. For a forward biased emitter junction C_{De} is usually much larger than C_{Te},

$\therefore \quad C_{De} + C_{Te} \simeq C_{De}$.

Stored charge in the base $Q_B = \dfrac{I.W^2}{2\,D_B}$

D_B = Diffusion constant for minority carriers in the base
W = Base width
I = Diffusion current

Emitter diffusion capacitance $C_{De} = \dfrac{dQ_B}{dV}$ = rate of change of Q_B with V.

or
$$C_{De} = \frac{dQ_B}{dV} = \frac{W^2}{2D_B}.\frac{dI}{dV} = \frac{W^2}{2D_B}.\frac{1}{r_e}$$

where $r_e = \dfrac{dV}{dI} = \dfrac{V_T}{I_E}$ emitter junction incrematal resistance.

$$C_{De} = \frac{W^2 I_E}{2D_B.V_T}$$

$$g_m = \frac{W^2}{2D_B}$$

Therefore Diffusion capacitance is proportional to emitter bias current I_E.
Hybrid - π models are valid for frequencies upto $\approx f_T/3$.

f_T : It is defined as the frequency at which the common emitter short circuit current gain becomes 1.

h_{fe} = short circuit current gain

$$\boxed{f_T \approx h_{fe} \cdot f_\beta = \frac{g_m}{2\pi(C_e + C_c)} \approx \frac{g_m}{2\pi C_e}}$$

The graph of f_T vs (versus) I_C is as shown. It depends $V_{CE} = 5V$ upon operating conditions

$T = 20^0C$

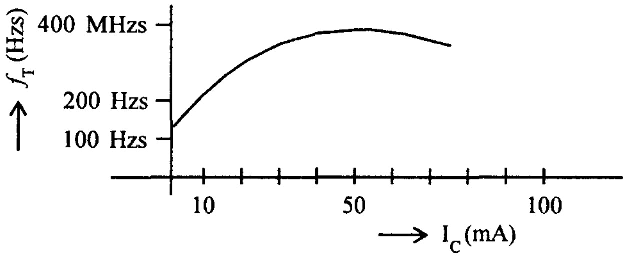


Fig. 3.25 f_T Vs I_C graph

3.11 Measurement of f_T

f_T is very high, to measure by experiments

$$|A_i| = \frac{h_{fe}}{\sqrt{1+\left(\frac{f}{f_\beta}\right)^2}} \quad A_i = \text{current amplification}$$

for $f >> f_\beta$, 1 can be neglected

$\therefore \quad |A_i| \cdot f = h_{fe} f_\beta$ or

$|A_i| \cdot f = h_{fe} f_\beta = f_T$

$\therefore \quad \boxed{f_T = h_{fe} \cdot f_\beta}$

$\therefore$ At some frequency f_1, measure gain $|A_i|$. Then

$f_T = f_1 \, |A_i|$

Ex : If f_T = 80 MHz, f_β = 1.6 MHz,

$f_1 = 5 \times 1.6 = 8$ MHz, which is convinient to measure than 80 MHz,

$\therefore$ At f_1 = 8 MHz, A_i = 10

$\therefore \quad f_T = f_1 (A_{i1}) = 80$

f_T can be used to measure C_e

$$\because \quad \boxed{C_e = \frac{g_m}{2\pi f_T}}$$

3.12 Variation of Hybrid-π Parameter with Voltage, Current and Temperature

1. $g_m = \frac{q|I_C|}{KT}$. As I_C increases g_m various linearly. It is independent of V_{CE}. It varies inversely with temperature. Incremental transconductance of a transistor.

2. C_c : V_{CE}^{-n}
3. β_0 : Low frequency value of β

   $\beta_0 = g_m \, r_{b'e}$

   Independent of I_C.

   Increases steadily with V_{CE}

   Increases with temperature T.

   r_π = Incrematal resistance in hybrid -π model.

3.12.1 Determination of Hybrid - π Parameters from Data Sheets

Suppose we want to determine the hybrid - π parameters for a 2N 3564 NPN silicon transistor at the operating point of I_C = 5 mA and V_{CE} = 5V. Make reasonable assumptions.

Table 3.1 Characteristics of 2N 3564 NPN silicon transistor at T = 25^{0}C.

Symbol	Parameter	Min.	Max.	Units	Test conditions
h_{fe}	Low frequency current gain at f = 1KHz	20	80	-	I_C = 15 mA, V_{CE} = 10V
h_{fe}	High frequency current gain f = 100 MHz	4	7.5	-	I_C = 15 mA, V_{CE} = 10V
$r_{b'}$	Real part of h_{ie} open circuit output	-	30	Ω	I_C = 15 mA, V_{CE} = 10V
C_{obo}	Capacitance		2.5	pf	V_{CB} = 10V, I_E = 0

At the desired operating point of 5mA,

$$\text{Trans Conductance} \quad g_m = \frac{q|I_C|}{KT} = \frac{|I_C|mA}{25} = \frac{5}{25} \quad = 0.2 \text{ mhos } (\mho).$$

$$\frac{1}{V_T} = \frac{q}{KT} = \frac{1}{25}$$

$\therefore$ r_π = Incremental **resistance** in the hybrid - π model = $r_{b'e}$.

$$r_{b'e} = \frac{h_{fe}}{g_m} = \frac{80}{0.2} = 400\ \Omega$$

From the Table 3.1 $C_{ob'}$ open circuit output capacitance = 2.5 pf at V_{CB} = 10V. (C_c) = C_μ will also be the same at 10V. Therefore to calculate C_C at the desired operating point of 5V, we have

$$C_c = C_\mu \approx (V_{CB})^{-1/3}$$

$$n = \frac{1}{3} \text{ for junction diode.}$$

$$\therefore \qquad C_{\mu} = C_C = 2.5 \times \left(\frac{5}{10}\right)^{-\frac{1}{3}} = 2.5 \times \left(\frac{10}{5}\right)^{+\frac{1}{3}} = 2.5\ \sqrt[3]{2} = 3.16 \text{ pf.}$$

To find C_e, (C_π), incremantal capacitance in hybrid - π model.

$$\omega_T = 2\,\pi f_T = \omega[h_{fe}(\omega)]$$

$$\therefore \qquad f_T = f(h_{fe})$$

$$h_{fe} = 7.5 \text{ at } f = 100 \text{ MHz}$$

$$\therefore \qquad f_T = 7.5 \times 100 = 750 \text{ MHz at } I_C = 15 \text{ mA}$$

$$C_e = \frac{g_m}{W_T} - C_C$$

$$C_e = C_\pi$$

$$\therefore \qquad C_\pi = \frac{g_m}{W_T} - C_C$$

$$= \left(\frac{600}{0.75 \times 2\pi}\right) - 2.5 = 126 \text{ pf at operating point of 10V}$$

$$C = C_e + C_C = \frac{g_m}{2\pi f_T}$$

$$\because \qquad g_m = \frac{q}{KT} \times I_c \text{ mA} \quad \frac{q}{KT} = \frac{1}{25}$$

$$I_C = 15 \text{ mA}, \qquad \therefore \qquad g_m = \frac{15}{25} = \frac{3}{5} = 0.6 \text{ mho } (\mho).$$

$$\therefore \qquad C_\pi = C_e = \frac{0.6}{2\pi \times 750 \times 10^6} - 2.5$$

$$= 128.5 - 2.5$$

$$= 126 \text{ pf}$$

To convert this to the desired operating point of I_C = 5mA, since (C_e varies linearly with I_C).

$$C_e = 126 \times \frac{5}{15}$$

$$= 42 \text{ pf}$$

Example : 3.7

Find wherever possible, appropriate values for the hybrid - π parameters at $I_C = 5$ mA, $V_{CE} = 4V$ for a 2N 1613 transistor (BJT) using the data listed below. Use typical values. Make reasonable approximations.

Characteristics of 2N 1613 at T = 25^{0}C

Symbol	Characteristics	Minimum	Typical	Maximum	Units	Test Conditions
h_{fe}	Low frequency f= 1KMHz gain	35	80	-	-	$I_C = 10$ mA $V_{CE} = 10V$
$\|h_{fe}\|$	High frequency and gain f= 20MHz	3	4	-	-	$I_C = 50$ mA $V_{CE} = 10V$
C_{ob}	output capacitance	-	18	25	pf	$I_E = 0$ $V_{CB} = 10V$
r_b'	Real part of h_{ie} at f= 350 MHz	-	30	-	Ω	$I_C = 10$ mA $V_{CE} = 10$ V

Transconductance : g_m

$$g_m = \frac{q|I_C|}{KT} \qquad \frac{KT}{q} \text{ at } T = 25^0C = 25$$

$$= \frac{5}{25} = 0.2 \text{ mhos } (\mho).$$

From low frequency h_{fe} data we know that $\beta_0 = 80$ at I_C =10 mA. We can assume that at $I_C = 5$ mA, β will be the same.

$$\therefore \qquad r_\pi = \frac{\beta_0}{g_m} = \frac{80}{0.2} = 400 \text{ ohms } (\Omega).$$

Incremantal resistance in hybrid - π model.

Feed back capacitance $C_\mu = 2.5 \left(\frac{10}{5}\right)^{+\frac{1}{3}} = 3.16$ pf at $V_{CB} = 5V \simeq V_{CE}$.

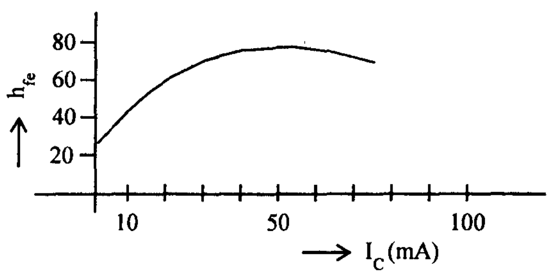


Fig. 3.26 Variation of h_{fe} with I_C

f_T : Frequency at which Current Gain = 1

$$\omega_T = \omega\, |h_{fe}(\omega)|$$

or $$f_T = f\, |h_{fe}(f)|$$

At $$f = 20 \text{ MHz}, \quad h_{fe} = 4$$

$\therefore$ $$f_T = 4 \times 20 = 80 \text{ MHz}$$

Capacitance in Hybrid - π Model

$$C_\pi = \frac{g_m}{\omega_T} - C_u$$

C_π is in pf. If we take g_m in KΩ, C_μ in pf, and ωT in nano seconds.

$$= \frac{0.2}{2 \times \pi \times 80 \times 10^6} - 3.16 \times 10^{-12}$$

$$= \frac{10^6 \times 0.1}{3.14 \times 80} - 3.16 \text{ pf}$$

$$= \frac{10^5}{251.20} - 3.16 \text{ pf}$$

$$\simeq 100 - 3.16 \text{ pf}$$

$$= 96.84 \text{ pf.}$$

Now we must convert it to the desired operating point of $I_C = 5$ mA, $V_{CE} = 4$V.

$$C_\pi \simeq C_b$$

C_π varies linerly with I_C.

$\therefore$ C_π at $I_c = 5$ mA, $V_{CE} = 10$V,

$$= 96.84 \times \frac{5}{10} = 48.42 \text{ pf}$$

To convert C_π to $V_{CE} = 4$V, instead of 10, we need to know the relation between ω **and** V_{CE}. As it is not known we assume that C_π remains the same at $V_{CE} = 4$V also.

$\mathbf{r_{bb'}}$ **:** $r_{bb'}$ at $I_C = 10$ mA, $V_{CE} = 10\text{V} = 30\Omega$

At $I_C = 4$ mA $\quad r_{bb'} \simeq 30\ \Omega$

3.13 Specification of Amplifiers

The Specification parameters and ideal values of an amplifier circuit are given below :

Parameters	Ideal Values	Typical Values
1. Bandwidth (BW)	∞	100 KHz
2. Volgate gain (A_V)	∞	600
3. Current gain (A_I)	∞	10
4. Power gain (A_P)	∞	6000
5. Figure of merit (Gain - BW product)	∞	1000 KHz
6. Input Impedance	∞	5.6 KΩ
7. Output Impedance	0	900 Ω
8. Frequency Roll-off	∞	2 db/decade; 8 db/octave

Example 3.8

If β = 150, what are the cutoff frequencies of the input and output lead networks of the given circuit ?

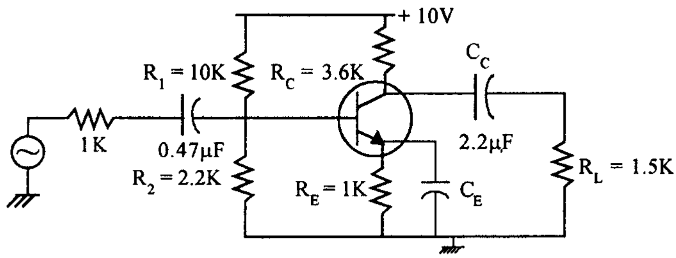


Fig. 3.27 CE amplifier circuit

When β value is given, and not h_{ie} of the transistor, the input impedance of the transistor can be determined.

$$Z_{in} = \frac{V_{in}}{i_b}$$

$$V_{in} = i_e r_e' \qquad i_e \cong i_C = \beta i_b$$

$$\therefore \quad V_{in} \cong \beta i_b . r_e'$$

$$\therefore \quad Z_{in} = \frac{\beta i_b . r_e}{i_b} = \beta . r_e'$$

$$R_{in} = R_1 \parallel R_2 \parallel \beta . r_e'$$

$$\beta r_e' = 150 \times 22.7 = 3.14\ K\Omega$$

$$R_{in} = 10K \parallel 2.2K \parallel 3.14\ K = 1.18K\Omega$$

$$R_0 = R_C = 3.6K$$

$$f_{in} = \frac{1}{2\pi(R_S + R_{in})C_{in}}$$

Cutoff frequences of input network (HPF)

$$f_0 = \frac{1}{2\pi(R_0 + R_L)C_0}$$

$$f_{in} = f_H = \frac{1}{2\pi(1K\Omega + 1.18K\Omega)(0.47\mu F)}$$

$$= 155 \text{ Hz.}$$

$$f_0 = f_L = \frac{1}{2\pi(3.6K + 1.5K\Omega)(2.2\mu F)}$$

$$= 14.2 \text{ Hz}$$

14.2 Hz is LPF cutoff frequency of output network.

3.14 Design of High Frequency Amplifiers

Broad band transistor (BJT) amplifiers use shunt feedback and series feedback methods so as to get large Gain – Band width (BW) product. If number of amplifier stages are cascaded, the output current is made up from several transistors and the individual device operating point canbe made to correspond to the optimem Gain - B.W. product of emitter current.

A single section of a multi stage amplifier is shown in Fig. 3.28. The input impedance of the amplifier circuit is low compared to the impedance of the parallel R-C network.

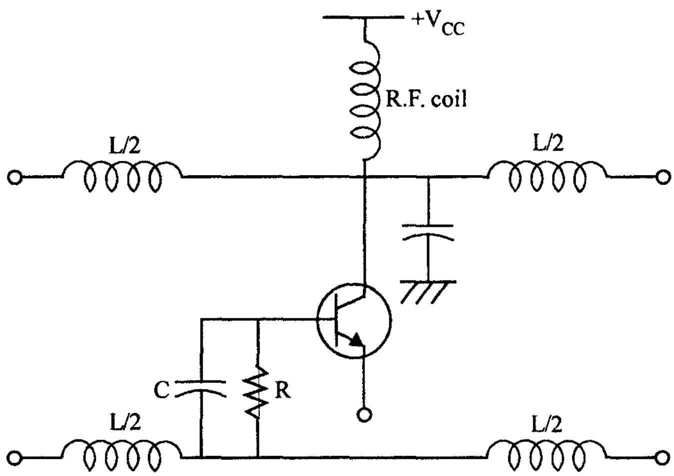


Fig. 3.28 One stage of multistage amplifier.

$$f_\beta = \frac{1}{2\pi RC}$$

where f_β is the β cut-off frequency of the transistor.

Now consider 3 such stages cascaded as shown in Fig. 3.29. R is the series resistor and h_{ie} is the transistor low frequency input impedance. h_{re} of the BJT is small and so it can be neglected.

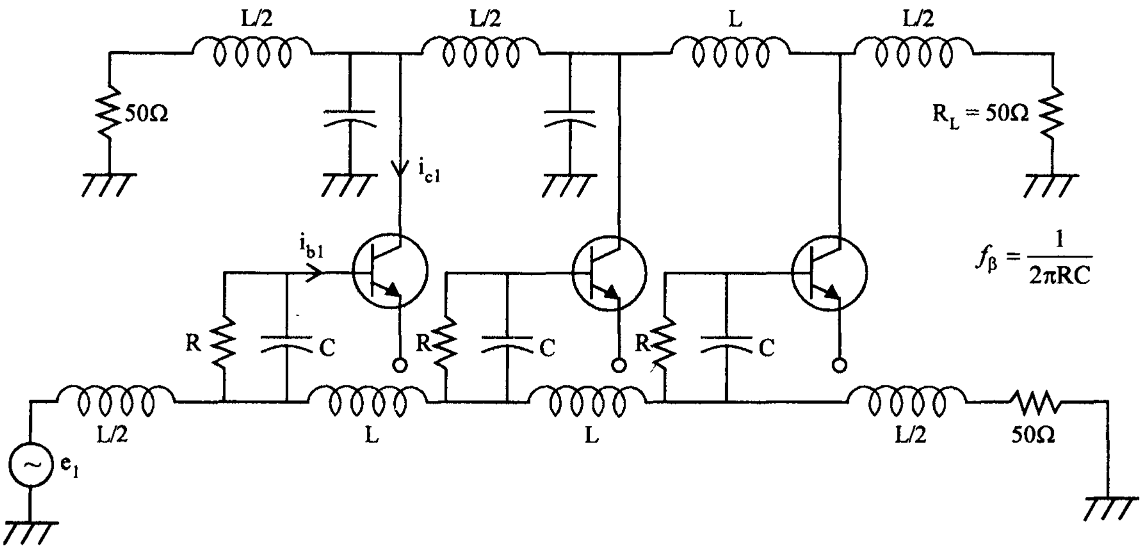


Fig. 3.29 Three stage cascaded amplifier.

e_1 is the input voltage

$$i_{b1} = \frac{e_1}{(R + h_{ie})} \simeq \frac{e_1}{R}$$

Since h_{ie} of the BJT is small compared to R.

R_L is a 50 Ω load for the circuit.

The voltage gain gets multiplied for each stage. So for n-stages,

$$e_0 = (n.\ i_c)\left(\frac{R_L}{2}\right) = n.\ \beta_o\, i_b \left(\frac{R_L}{2}\right)$$

$$= \frac{n.\ \beta_0 .\ e_1 .\ R_L}{2R}$$

where β_0 is the low frequency current gain (β) of the BJT.
n = number of cascaded stages.

The Voltage Gain for 'm' cascaded stages is, (V.G) m

$$(V.\ G)_m = \left[\frac{n.\ R_L .\ \beta_0}{2R}\right]^m$$

Typically, a single stage will have a 3-db frequency of 200 MHzs in high frequency amplifiers.

Effect of Emitter Degeneration :

The approximate high frequency equivalent circuit for a BJT operating in C.E. configuration is shown in Fig. 3.30

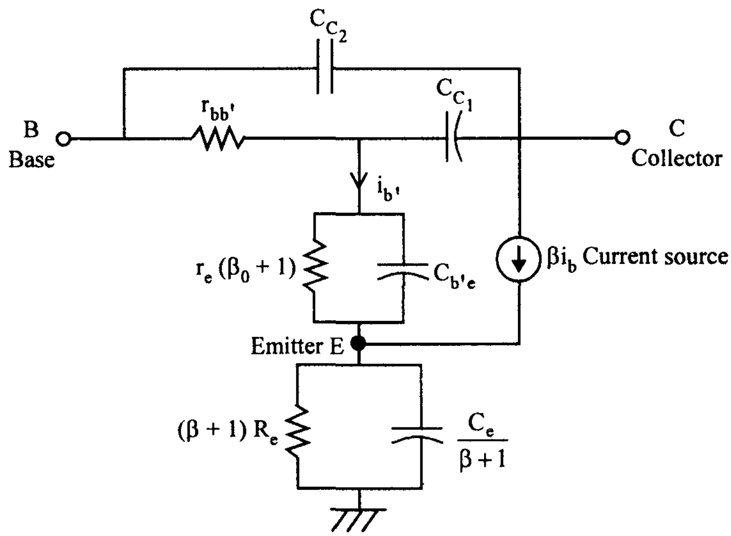


Fig. 3.30 High frequency equivalent circuit for a BJT.

$r_{bb'}$ = Base spread resistance

C_{C_1} = Collector emitter capacitance

C_{C2} = Collector-base capacitance

r_e = Emitter resistance = $\frac{VT}{J_e} = \left(\frac{25}{I_e}\right)$ Ω at 25 °C.

T = Temperature in OK; (273 + 25) = 298 ^{0}K for 25 °C.

k = Boltzmans' constant.

$C_{b'e}$ = Diffusion capacitance

Let β be the current gain at any frequency *f*.

Then
$$\beta = \frac{\beta_0}{1 + j\left(\frac{f}{f_\beta}\right)}$$

where β_0 = Low frequency current gain

f_β = Beta cutoff frequency

Typical values of these parameters are, for $V_{CE} = 10V$, $I_E = 10mA$

$r_{bb'} = 70\ \Omega$

$C_{C1} = 1pf$

$C_{C2} = 2\ pf$

$\beta_0 = 100$

$f_\beta = 6$ MHZs

$r_e = 4\ \Omega$

$C_{b'e} = 130\ pf$

If $f >> f_\beta$, the input circuit can be simplified as, (Fig. 3.31)

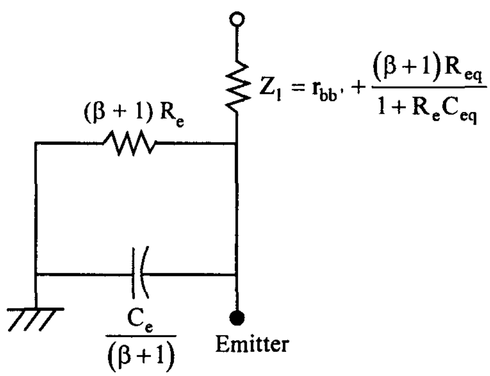


Fig. 3.31 Simplified input circuit.

The equivalent input impedance of the R-C combination on the input side along with transistor capacitances is shown in Fig. 3.31.

If the frequency range of consideration is such that X_{ce1} and X_{ce2} can be neglected and 'f' is greater than f_β,

$f > f_\beta$ but X_{ce1} and X_{ce2} are negligible,

$$Z_1 \simeq r_{bb'} + \frac{(\beta+1)R_e}{(1+j\omega R_eC_e)}$$

But,
$$\beta = \frac{\beta_0}{\left(1+j\frac{f}{f_\beta}\right)}$$

$$= \frac{\beta_0}{\left(1+j\frac{\omega}{\omega_\beta}\right)}$$

Upper cut-off frequency $f_2 = \dfrac{1}{2\pi R_e C_e}$

for frequencies below f_2,

$$Z_1 \simeq \frac{(r_{bb'} + R_e) + R_e\ \beta_0}{1 + \dfrac{j\omega}{\omega_\beta}}$$

with a parallel R-C network inserted in the base,

we have, $$Z_T = \left[\frac{R}{1 + j\omega CR}\right] + (r_{bb'} + R_e) + \frac{\beta_0 R_e}{1 + j\dfrac{\omega}{\omega_\beta}}$$

If the R-C combination has the same 3-dB points as f_β, then $f_\beta = \dfrac{1}{2\pi RC}$

so that $$Z_T = \frac{R + \beta_0 R_e}{1 + \left(\dfrac{j\omega}{\omega_\beta}\right)} \cdot [r_{bb'} + R_e]$$

If $f > f_\beta$ but less than f_2, $\left(f_2 = \dfrac{1}{2\pi R_e C_e}\right)$, the input impedance of the delay line comprises a resistance $(r_{bb'} + R_e)$ in series with a parallel combination of R_{eq} and C_{eq}.

Calculation of R_e and C_e for a required Gain - B.W value (for uncompensated case)

The voltage gain A_v of one section at low frequencies is given by,

$$A_V = \frac{\beta_0\ R_L}{2\left[(R + \beta_0 R_e) + (r_{bb'} + R_e)\right]}$$

$$= \frac{\beta_0\ R_L}{2(R + \beta_0 R_e)}$$

For uncompensated case, $C_e = 0$.

The Bandwidth B.W is given as,

$$B.W = \frac{1}{2\pi\ C_{eq}(R_e + r_{bb'})}$$

where $$C_{eq} = \frac{1}{2\pi f_\beta (R + \beta_0\ R_e)}$$

$\therefore$ $$B.W \simeq f_2$$

Gain Band width product = $\dfrac{f_\beta \cdot \beta_0 R_L}{2(r_{bb'} + R_e)}$

For compensated case, $C_e \neq 0$

$$\therefore \qquad Z_T = \frac{R}{\left(1 + j\dfrac{\omega}{\omega_\beta}\right)} + r_{bb'} + \frac{R_e}{1 + j\omega R_e C_e} + \frac{\beta_0 R_e}{\left(1 + j\dfrac{\omega}{\omega_\beta}\right)(1 + j\omega R_e C_e)}$$

In order to have good compasation, $R_e C_e$ must be chosen such that the break frequency is same as in the case of uncompensated Band width.

$\therefore$ we have, $\qquad f_{2u} = f_2$ of uncompensated circuit,

$$f_{2u} = \frac{1}{2\pi C_e R_e}$$

The value of f_{2c}, the upper cut-off frequency for compensated circuit can be obtained by equating the real and imaginary parts of Z_T at f_{2c}.

Since $\qquad f_{2c} > f_\beta$,

We have $\qquad 1 + \left(\dfrac{j\omega}{\omega_\beta}\right) \simeq \dfrac{j\omega}{\omega_\beta}$

Also, $\qquad \omega C_e R_e = 1$

$\therefore \qquad Z_T$ at $f = f_{2c}$.

$$= -j\left[R + \{(\beta_0 R_e (1+j))\}\left(\frac{\omega_\beta}{\omega_{2c}}\right) + r_{bb'} + \left(\frac{R_e}{1+j}\right)\right]$$

$$= \left[r_{bb'} + \left(\frac{R_e}{2}\right) - \left(\frac{j\beta\, \beta_0 R_e}{2f_{2c}}\right)\right] - j\left[\frac{f_\beta(\beta_0 R_e + 2R)}{2f_{2c}} + \left(\frac{R_e}{2}\right)\right]$$

Equating real and Imaginary parts,

$$f_{2c} = \frac{f_\beta(R_0 + \beta_0 R_e)}{r_{bb'}}$$

The B.W improvement factor 'k' is,

$$k = \frac{f_{2c}}{f_{2u}} = 1 + \left(\frac{R_e}{r_{bb'}}\right)$$

L_0 and C_0 can be determined, using the transmission line equation,

$$Z_0 = \sqrt{(L_0 / C_0)\left[1 - \left(\frac{f}{f_{\text{cut-off}}}\right)^2\right]}$$

$$f_{cut\text{-}off} = \frac{1}{2\pi\sqrt{L_0 C_0}}$$

C is usually chosen as 2 or 3 times C_0

R is computed to correspond to $R = \dfrac{1}{2\pi\, C f_\beta}$.

R_e can be calculated from the equation for f_{2c}.

C_e is obtained from the equation for f_{2u}.

Typical values are :

$$f_{cut\text{-}off} = 250 \text{ MHz}$$
$$Z_0 = 48\ \Omega$$
$$L_0 = 0.05\ \mu H$$
$$C_0 = 19\ pf$$
$$(R + \beta_0 R_e) = 2.5\ k\Omega$$
$$R_e = 30\ \Omega$$
$$C_e = 50\ pf$$

Problem 3.9 : Find Z_i, Z_0 and A_v in the case of an emitter follower given that,

$$C_{be'} = 1000\ pf \quad C_{b'c} = 10\ pF$$
$$r_{b'e} = 100\ \Omega \quad r_{bb'} = 30\ \Omega$$
$$h_{fe} = 100 \quad R'_e = 100\ \Omega$$
$$R_i^1 = 190\ \Omega$$

Expression for midband input impedance is,

$$Z_i\ (\text{midband}) = r_{bb'} + r_{b'e} + (1 + h_{fe}) R_{e'}$$
$$= 30 + 100 + (100 + 1)\ 100$$
$$= 130 + (101)\ (100)$$
$$Z_i\ (\text{midband}) \simeq 10k\Omega$$
$$(r_{b'}e + h_{fe} R_{e'}) >> R_{e'}$$

We have
$$C^1 = \frac{C_{b'e}}{1 + g_m R_{e'}}$$
$$= \frac{1000 \times 10^{-12}}{(1 + 100)}$$
$$\simeq 10pF$$

$$\omega_1 = \frac{1}{(r_{b'e} + h_{fe}R_e')(C_{b'c} + C')}$$

$$= \frac{1}{(100 + 10^4)\ (10 + 10)10^{-12}}$$

$$\omega_1 = 5 \times 10^6 \text{ rad/sec}$$

for emitter follower $A_v < 1$.

Problem 3.10 : Design a single stage I.F. amplifier to have carrier frequency f_c = 455 kHZs, B.W = 10 kHZs, $V_{cc} = -9V$, $I_c = -1mA$. The small signal hybrid π parameters are :

$r_{bb'} = 70\ \Omega$ $\quad C_{b'e} = 1550\ pf$

$g_{b'e} = 800\ \mu v$ $\quad C_{b'e} = 9\ pf$

$g_{ce} = 8.6\ \mu\Omega$ $\quad g_m = 38.6\ m\mho$

$g_{b'e} = 0.25\ \mu\Omega$

Solution : The circuit diagram is shown below

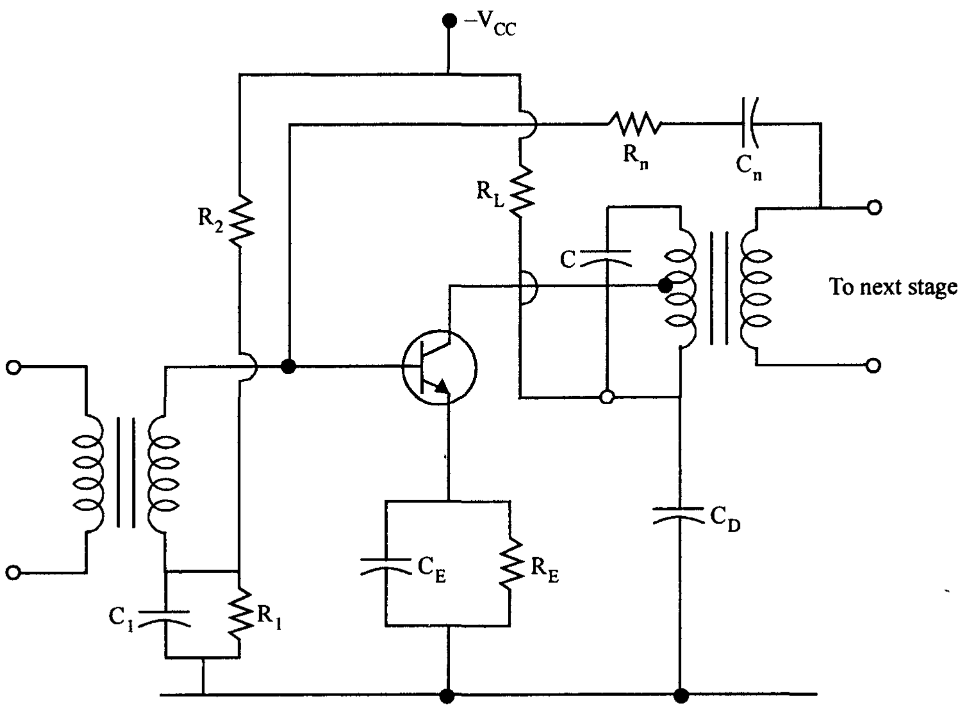


Fig. 3.32 I.F. amplifier single stage.

$$r_{b'e} = \frac{1}{g\,b'e} = 1.25\text{ k}\Omega$$

$$r_{ce} = \frac{1}{g_{ce}} = 120\text{ k}\Omega$$

$$r_{b'c} = \frac{1}{g\,b'c} = 4\text{ M}\Omega$$

$$g_{bb'} = 0.133\text{ m℧}$$

$$\omega_r = 2\pi f_r = 2.8\text{ rad/sec}$$

Choose R_1 and R_2 such that $I_c = 1$mA.

Since $X_{C1} << R_1$, if $R_1 = 5\text{k}\Omega$, than $C_1 = 0.05\ \mu$F

If $R_1 = 1\text{k}\Omega$, then $C_1 = 0.1\mu$F.

Let $R_L = 500\ \Omega$ and $C_D = 0.05\ \mu$F

Substituting in the expression for R_i and R_o,

$$R_i = 526\ \Omega \qquad R_o = 32.4\text{ k}\Omega.$$

$$C_i = 1268\text{ pF} \qquad C_o = 33\text{ pF}$$

$$G_m = 34.6\text{ mA/V}.$$

R_y is calculated as 12.4 kΩ. C_y is calculated as 9 pF. R_0 must be matched with the load (R_i of the next stage). So the transformer turns ratio must be,

$$n = \sqrt{\frac{R_o}{R_i}} = \sqrt{\frac{32.4 \times 10^3}{526}}$$

$$= 7.8 : 1$$

The feedback components, resistor R_n and capacitor C_n can be determined as,

$$R_n = \left(\frac{R_y}{n}\right) = \frac{12.7\text{k}\Omega}{7.8} = 1640\Omega$$

$$C_n = n.\ C_y = 7.8 \times 9 \times 10^{-12} = 70.2\ pf$$

The equivalent circuit is shown in Fig. 3.33.

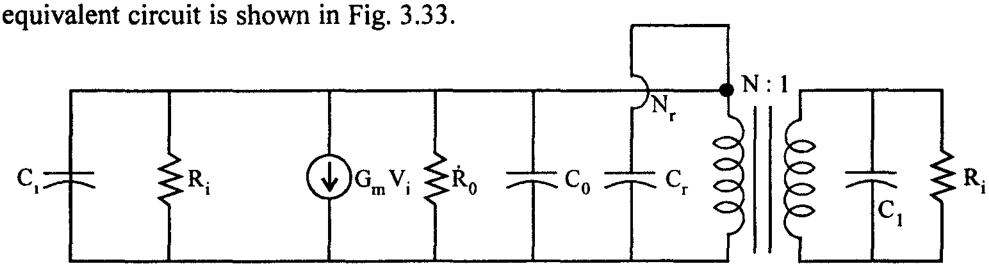


Fig. 3.33 Equivalent circuit.

$$P_i = \frac{V_i^2}{R_i}; \quad R_L = R_o = n^2 R_i$$

$$I_L = I_o$$

$$\therefore \quad P_o = I_o^2 . R_L = I_o^2 R_o = \left(\frac{G_m V_i}{2}\right)^2 . R_o$$

$$\text{Power gain } A_p = \frac{P_o}{P_i} = \left(\frac{G_m^2 . R_o R_I}{4}\right)$$

$$= \frac{\left(34.8 \times 10^{-3}\right)^2 . 32.4 \times 10^3 \times 528}{4}$$

$$= 5200$$

Power gain in dB = 10 log (5200) = 37.16 dB

$$\text{Q factor} = \frac{f_r}{B} = \frac{455 \times 10^3}{10 \times 10^3} = 45.5$$

with a coil having $Q_c = 100$,

The inductance of the coil is,

$$L = \frac{R_o (Q_c - Q)}{2\omega r\, Q.Q_c}$$

$$= \frac{32.4 \times 10^3 (100 - 45.5)}{2 \times 2.86 \times 10^6 \times 45.5 \times 100}$$

$$= 67 \ \mu H$$

Parallel tuning capacitance

$$C = \frac{1}{\omega r^2 L}$$

$$= \frac{1}{\left(8.18 \times 10^{12}\right)^2 . \left(68 \times 10^{-6}\right)} \simeq 1800 pF$$

The total transformer primary inductance L_T is,

$$L_T = \frac{1}{\omega r^2 c} = \frac{1}{\left(8.18 \times 10^{12}\right)^2 \left(206.2 \times 10^{-12}\right)}$$

$$L_T = 590 \ \mu H$$

Problem 3.11 : Design a JFET Single Tuned Narrow Band amplifier with a centre frequency of 5.0 MHZs, Q = 40, B.W = 100 KHZs midband gain A_{mid} = 150. Given, for the JFET, C_{DG} = 20 PF, C_{GS} = 50PF, V_{DD} = 15V, V_P = – 2V.

Solution : Given

f_0 = 5 MHZs	L = ?
Q = 40	C = ?
A_{mid} = 150	R_D = ?
C_{DG} = 20 pF	
C_{GS} = 50 pF	
V_{DD} = 15 V	
V_p = –2 V	
g_n = 10 m℧	
r_0 = 1 MW	

Circuit Diagram :

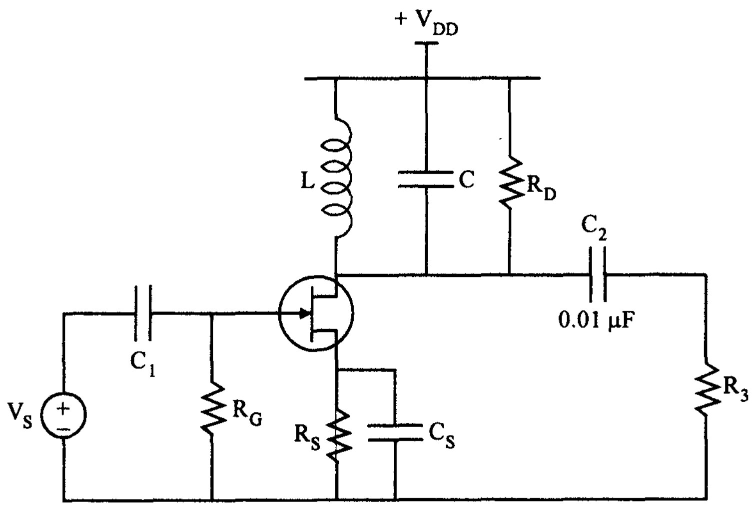


Fig. 3.34 Circuit diagram for Problem 3.11.

Expression for $A_v(s) \simeq A_{mid} \dfrac{s\left(\dfrac{\omega_0}{Q}\right)}{s^2 + s\left(\dfrac{\omega_0}{Q}\right) + \omega_0^2}$

Centre frequency $\omega_0 = \dfrac{1}{\sqrt{L(C + C_{GD})}}$

Quantity factor $Q = \omega_0 R_p (C + C_{GD}) = \dfrac{R_p}{\omega_0 L}$; $A_{mid} = g_m \cdot R_p$

where R_0 is the parallel resistance,

$$R_p = (r_0 \parallel R_D \parallel R_3)$$

The maximum value of $R_p = r_0$.

$$f_0 = 5 \text{ MHZs}$$

$$\omega_0 = 2\pi f_0 = 2 \times 3.14 \times 5 \times 10^6 = 31.4 \text{ MHZs}$$

$$\omega_0 = \frac{1}{\sqrt{L(C + C_{GD})}}$$

$$31.4 \times 10^6 = \frac{1}{\sqrt{L\left(C + 20 \times 10^{-12}\right)}} \qquad .....(1)$$

$$Q = \frac{R_p}{\omega_0 L}$$

$$40 = \frac{R_p}{31.4 \times 10^6 \times L} \qquad .....(2)$$

$$A_{mid} = g_m \cdot R_p \qquad .....(3)$$

$$150 = 10 \times 10^{-3} \times R_p$$

$$\therefore \quad R_p = \frac{150}{10 \times 10^{-3}} = 15\text{k}\Omega;$$

$$R_p = 15\text{k}\Omega$$

$$40 = \frac{15 \times 10^3}{31.4 \times 10^6 L}$$

$$\therefore \quad L = \frac{15 \times 10^3}{31.4 \times 10^6 \times 40} = 0.012 \times 10^{-3} \text{ H} = 0.012\text{mH}$$

$$\omega_0 = \frac{1}{\sqrt{L(C + C_{GD})}}$$

$$\therefore \quad 31.4 \times 10^6 = \frac{1}{\sqrt{0.012 \times 10^{-3}(C + 20pf)}}$$

$$(31.4 \times 10^6)^2 = \frac{1}{0.012 \times 10^{-3}(C + 20pf)}$$

$$0.012 \times 10^{-3} (C + 20 \text{ pF}) = \frac{1}{\left(31.4 \times 10^6\right)^2} = 0.001 \times 10^{-12} = 10^{-15}$$

$$(C + 20 \text{ pF}) = \frac{10^{-15}}{0.012 \times 10^{-3}} = 83.3 \times 10^{-12} = 83.3 \text{ pF}$$

$$\therefore \quad C = 83.3 - 20 = 63.3 \text{ pF}$$

$$\therefore \quad L = 0.012 \text{ mH}$$

$$C = 83.3 \text{ pF}$$

Let $R_s = 100 \text{ k}\Omega \qquad R_p = r_0 \parallel R_D \parallel R_3$

$r_0 = 1\text{M}\Omega$

$R_p = 15\text{k}\Omega \quad \therefore \; R_D = ?$

$$r_0 \parallel R_3 = \frac{1\text{M}\Omega \times 100\text{k}\Omega}{(1\text{M}\Omega + 100\text{k}\Omega)} = \frac{10 \times 10^5 \times 10^5}{\left(10 \times 10^5 + 10^5\right)}$$

$$r_0 \parallel R_3 = \frac{10^{11}}{11 \times 10^5} = \frac{10^6}{11}$$

$$R_p = \frac{10^6}{11} \parallel R_D$$

$$15 \times 10^3 = \frac{\frac{10^6}{11} \times R_D}{\frac{10^6}{11} + R_D} = \frac{10^6 R_D}{\left(10^6 + 11R_D\right)}$$

$$15 \times 10^9 + 165 \times 10^3 R_D = 10^6 R_D$$

$$15 \times 10^9 = 10^3 R_D (1000 - 165)$$

$$15 \times 10^9 = 10^3 \times R_D \times 835$$

$$R_D = \frac{15 \times 10^9}{10^3 \times 835} = 0.012 \times 10^6 = 12\text{k}\Omega$$

$\therefore$ $R_D = 12\text{k}\Omega$

Objective Type Questions

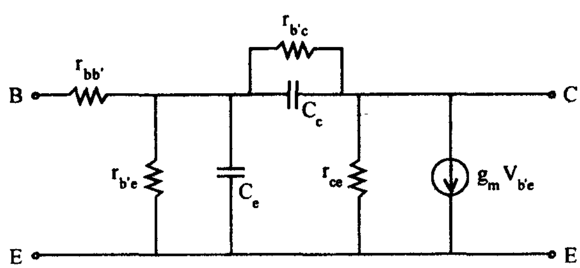
1. Hybrid - π model is also known as model ________________ model.
2. Hybrid - π circuit is so named because ________________.
3. b' to denote Base spread resistance $r_{bb'}$ is ________________ terminal of the transistor.
4. Transconductance g_m in Hybrid - π model is defined as ________________.
5. Typical value of $r_{bb'}$ is ________________.
6. Expression for $g_{b'e}$ = ________________.
7. Expression for h_{ie} in terms of h_{fe} and I_C is, ________________.
8. f_T is the frequency at which Common Emitter short circuit current gain ________________.
9. Relation between f_T, h_{fe} and f_β is ________________.
10. Expression for C_e interms of g_m and f_T is, ________________.
11. Typical value of $C_{ob'}$ output capacitance is ________________.
12. r_π in Hybrid - π equivalent circuit is ________________.
13. If h_{fe} = 100, g_m = 0.5 mhos, determine the value of $r_{b'e}$.
14. Hybrid π capacitance C_π is of the order of ________________.
15. Relation between f_T, f_β and h_{fe} is, ________________.
16. Classify amplifiers depending on the position of the quiescent point of each amplifier.
17. Draw the hybrid -π model for a transistor in CE configuration.
18. What is f_T ?
19. What is the significance of the gain bandwidth product ?
20. What would you neglect while drawing a low frequency model ?
21. How does the trans conductance (g_m) depend on current ?
22. How does the trans conductance (g_m) depend on temperature ?
23. Write the expression for r_{be} in terms of g_m and h_{fe}.
24. How does the diffusion capacitance depend on current and temp ?
25. Write the expression for C_{De} in terms of g_m, W, D_B.
26. When is the hybrid - π model valid ? (at what frequencies)
27. What is an emitter follower ?
28. Which time constant is considered for the bandwidth ?
29. What is the expression for β cutoff frequency ?
30. How are f_β and f_T related ?

Essay Type Questions

1. Draw the high frequency equivalent circuit of a BJT and explain the same.
2. Give the typical values of various Hybrid - π parameters.
3. Derive the expressions for Hybrid - π parameters., C_e, $r_{bb'}$, $r_{b'e}$, C_C
4. Derive the expression for the Hybrid - π parameters g_m, r_{ce}, C_e and $r_{b'c}$, g_{ce}.
5. Explain about Hybrid - π capacitances. How do Hybrid - π parameters vary with temperature ?
6. Obtain the expressions for f_β and f_T of a transistor.
7. Draw the circuit and derive the expression for CE short circuit current gain A_i interms of at any frequency 'f' and f_β of the BJT.
8. Explain how f_β and f_T of a BJT can be determined ? Obtain the expression for the Gain - Bandwidth product of a transistor.

Answers to Objective Type Questions

1. Giacoletto model
2. The parameters are of different units (Hybrid) Ω ,℧, constants etc. The shape of the circuit is in π - shape.
3. Fictitious terminal
4. $g_m = \left.\dfrac{\delta I_C}{\delta V_{B'E}}\right| V_{CE} = K.$
5. 100 Ω
6. $g_{b'e} = g_m / h_{fe}$
7. $h_{ie} = \dfrac{h_{fe} V_T}{|I_C|}$
8. becomes unity
9. $f_T = h_{feo} f_\beta$
10. $C_e = g_m / 2\pi f_T$.
11. 2.5 pf.
12. Incremental resistance.
13. $r_{b'e} = h_{fe} / g_m = 200\ \Omega$.
14. Picofarads
15. $f_T = h_{fe} f_\beta$
16. Class A, B, AB, C
17.



18. Frequency at which short circuit current gain is unity.

19. Tradeoff b/w gain and BW.

20. Capacitances.

21. g_m directly depends on current. or $g_m = \dfrac{|I_C|}{V_T}$ or $g_m = \dfrac{|I_C|}{26}$ mt.

22. g_m inversely proportional to temp.

23. $g_{b'e} = \dfrac{g_m}{h_{fe}} \Rightarrow r_{b'e} = \dfrac{h_{fe}}{g_m}$.

24. C_{de} α current α T^n

25. $C_{De} = g_m \dfrac{W^2}{2D_B}$

26. $2\pi f \dfrac{W^2}{6D_B} << 1$ or $f << 3f_T$ or $f = \dfrac{f_T}{3}$

27. CC

28. input time constant.

29. $f_\beta = \dfrac{1}{h_{fe}} \dfrac{g_m}{2\pi(C_e + C_c)}$

30. $f_T = h_{fe} f_\beta$

UNIT - 4

Power Amplifiers

In this Unit,

- Power amplifiers - Class A, Class B, Class C, Class AB and other types of amplifiers are analyzed.
- Advantages and Disadvantages of different types are discussed.
- Thermal considerations and use of heat sinks is also explained.

4.1 Introduction

When the output to be delivered is large, much greater than mW range and is of the order of few watts or more watts, conventional transistor (BJT) amplifiers cannot be used. Such electronic amplifier circuits, delivering significant output power to the load (in watts range) are termed as *Power Amplifiers*. Since the input to this type of amplifier circuits is also *large*, they are termed as *Large Signal Amplifiers*. In order to improve the circuit efficiency, which is the ratio of output power delivered to the load P_0 to input power, the device is operated in varying conduction angles of 360^0, 180^0 less than 180^0 etc. Based on the variation of conduction angle, the amplifier circuits are classified as Class A, Class B, Class C, Class AB, Class D, and Class S.

4.1.1 Power Amplifier

Large input signals are used to obtain appreciable power output from amplifiers. But if the input signal is large in magnitude, the operating point is driven over a considerable portion of the output characteristic of the transistor (BJT). The transfer characteristic of a transistor which is a plot between the output current I_C and input voltage V_{BE} is not linear. The transfer characteristic indicates the change in i_c when V_b or I_B is changed. For equal increments of V_{BE}, increase in I_C will not be uniform since output characteristics are not linear (for equal increments of V_{BE}, I_C will not increase by the same current). So the transfer characteristic is not linear. Hence because of this, when the magnitude of the input signal is very large, distortion is introduced in the output in large signal power amplifiers. To eliminate distortion in the output, pushpull connection and negative feedback are employed.

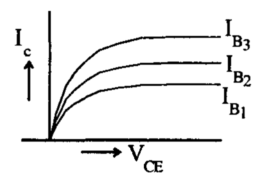


Fig. 4.1 Output characteristics of BJT in CE mode

For simplicity let us assume that the dynamic characteristic of the transistor is linear.

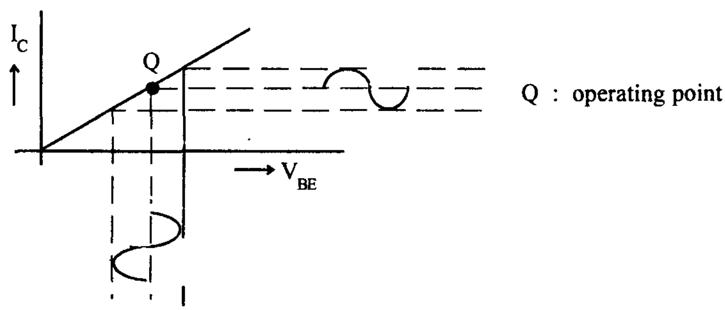


Fig. 4.2 Transfer characteristics of BJT

4.1.2 Class A Operation

If the *Q point is placed near the centre of the linear region of the* dynamic curve, class A operation results. Because the transistor will conduct for the complete 360^0, distortion is low for small signals and conversion efficiency (η) is low.

4.1.3 Class B Operation

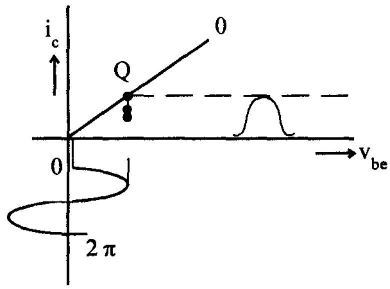


Fig. 4.3 Transfer curve

For class B operation the Q point is set near cutoff. So output power will be more and conversion efficiency (η) is more. Conduction is only for 180^0, from π - 2π. Since the transistor Q point is beyond cutoff, the output is zero or the transistor will not conduct. Output power is more because the complete linear region is available for an operating signal excursion, resulting from one half of the input wave. The other half of input wave gives no output, because it drives the transistor below cutoff.

4.1.4 Class C Operation

Here Q point is set well beyond cutoff and the device conducts for less than *180^0*. The conversion efficiency (η) can theoretically reach 100%. Distortion is very high. These are used in radio frequency circuits where resonant circuit may be used to filter the output waveform. Class A and class B amplifiers are used in the audio frequency range. Class B and class C are used in Radio Frequency range where conversion efficiency is important.

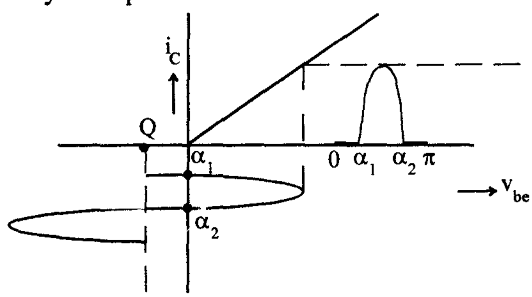


Fig. 4.4 Transter curve

4.1.5 Large Signal Amplifiers

With respect to the input signal, the amplifier circuits are classified as

(i) Small signal amplifiers (ii) Large signal amplifiers

4.1.6 Small Signal Amplifiers

Here the magnitude of the input signal is very small, slightly deviating from the operating point. But always the operation is in the active region only. The characteristics of the device can be assumed to be linear. We can draw the equivalent circuit and analyse the performance. The magnitude of the signal may be few mV, in single digits. The operating point or Quiescent point Q swings with the input signal. Because the input signal magnitude is small, the operating point is in the active region only.

4.1.7 Large Signal Amplifiers

Here the magnitude of the input signal is very large and deviation from the operating point on both sides is very wide. So because of this, the device performance cannot be assumed to be linear. Because of the large swing of the input signal, the non linear portion of the transistor characteristics are also to be considered. Hence the linear equivalent circuit analysis is not valid. So for large signal amplifiers only graphical analysis is employed.

Power amplifiers, class A, class B, class C amplifiers, push-pull amplifier are of this type. Large signal amplifiers are used where the output *power requirement is large.* If we use small signal amplifiers, the number of stages to be cascaded will be large, complicating the circuit.

Factors to be considered in large signal amplifiers :

1. Output power
2. Distortion
3. Operating region
4. Thermal considerations
5. Efficiency (η)

Amplifier circuits may be classified in terms of the portion of the cycle for which the active device conducts.

Class A	:	It is one, in which the active device conducts for the full 360^0. The device is biased in that way.
Class B	:	Conduction for 180^o
Class C	:	Conduction for $< 180^o$
Class AB	:	Conduction angle is between 180^o and 360^o

4.2 Class A Power Amplifier

The circuit for class A amplifier considering only load resistance R_L is as shown, in Fig. 4.5.

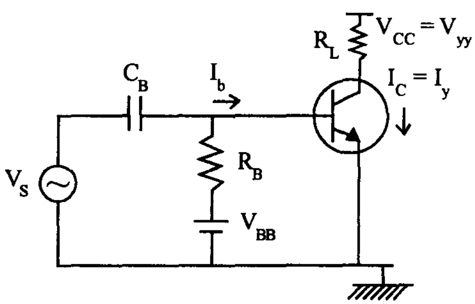


Fig. 4.5 Class A power amplifier

There are two types of operations :

1. Series fed 2. Transformer coupled

4.2.1 Series fed

There is no transformer in the circuit. R_L is in series with V_{cc}. There is DC power drop across R_L. Therefore efficiency (η) = 25% (maximum).

4.2.2 Transformer Coupled

The load is coupled through a transformer. DC drop across the primary of the transformer is negligible. There is no DC drop across R_L. Therefore η = 50% maximum.

V_y and I_y are the root mean square (rms) values of voltage and current.

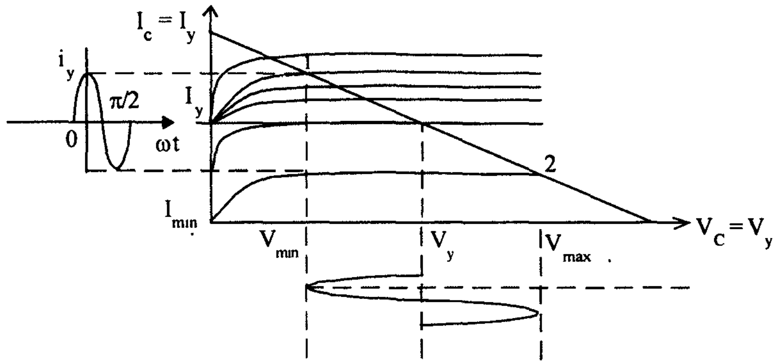


Fig. 4.6 Output characteristics

In class A amplifier, the conduction is for full 360^0. Therefore the operating point lies in the active region only. Let us assume that the static output characteristic of the transistor are ideal and linear. So if the input is a sinusoidal signal, then the output will also be sinusoidal.

Let us use the subscripts y for output and x for input. Therefore $i_c = i_y$. Output is on y-axis. So subscript y is used. Input is on x-axis. So subscript 'x' is used.

The output power P_y can be found graphically.

V_y = (rms) output voltage

I_y = (rms) output current

Subscript 'y' for output

Subscript 'x' for input

$$P = V_y I_y = I_y^2 R_L.$$

$$I_m = \text{Peak value fo the current} = \left(\frac{I_{max} - I_{min}}{2}\right)$$

$$I_{rms} = I_m/\sqrt{2} = I_y$$

$$I_y = \frac{I_m}{\sqrt{2}} = \frac{I_{max} - I_{min}}{2\sqrt{2}}$$

$\because$ $(I_{max} - I_{min})$ = Peak to peak value

$$\therefore \quad I_m = I_y = \frac{I_{p-p}}{2\sqrt{2}}$$

$$V_y = \frac{V_m}{\sqrt{2}} = \frac{V_{max} - V_{min}}{2\sqrt{2}}$$

Therefore output power $P = \frac{V_m . I_m}{2} = \frac{(V_{max} - V_{min})(I_{max} - I_{min})}{8}$

$$= \left(\frac{V_m}{\sqrt{2}} . \frac{I_m}{\sqrt{2}}\right)$$

$$= \left(\frac{V_m . I_m}{2}\right)$$

4.2.3 Efficiency of Amplifier Circuits

Let V_{yy} is the DC voltage being supplied to the circuit and I_y is the DC current drawn by the circuit. Therefore the DC power input to the circuit is V_{yy}. I_y. Let R_L be the load resistance. Therefore *DC power* absorbed by the load is $(I_y^2 . R_L + I_y V_y)$ where I_y and V_y (with small subscripts y) are the rms current and voltages absorbed by the load and I_Y (capital Y) is the DC current absorbed by the load. In addition to the DC drop across the load and AC drop across the load there is thermal power dissipation P_D across the device, since it gets heated. According to the law of conservation of energy, the input power should be equal to AC power, + DC power loss across the load and thermal dissipation.

$\therefore$ $V_{yy} I_y = I_y^2, R_L + I_y V_y + P_D$

$V_{yy} . I_y$ = Total input power

$I_y^2 . R_L$ = DC power drop in the load

$I_y . V_y$ = AC power in the load

But $V_{yy} = V_y + I_y R_L$

V_Y = DC voltage, I_Y = DC current

$\therefore$ $P_D = (V_y + I_y R_L) I_y = I_y^2 R_L + I_y V_y + P_D$

P_D = Thermal power dissipation.

$\therefore$ $P_D = V_y I_y - v_y i_y$

If the load is not a pure resistance, $V_y I_y$ should be replaced by $V_y I_y \cos \theta$. The total AC input power + Input DC power = DC drop across the load + AC output voltage + thermal dissipated power. Now if there is no AC output power i.e, the device is not conducting, then the rest of the power should be dissipated as heat. Therefore if AC power output is zero, ie., AC input signal is zero, then P_D is maximum. and has its maximum value $V_y I_y$. Therefore the device is cooler when delivering power to a load than when there is no such AC power transfer. When there is power drop across the device itself, it gets heated.

4.3 Maximum Value of Efficiency of Class A : Amplifier

Certain assumptions are made in the derivation, which will simplify the estimation of the efficiency (η). Because of this some errors will be there and the expression is approximate.

The assumption is that the static output characteristic of the transistors are equally spaced, in the region of the load line for equal increments in the base current. If i_b is increased by 1 μA, i_c will increase by 1mA, and if i_b is increased by 3 μA, i_c will increase by 3mA. Thus for the load line shown in the Fig. 4.7 the distance from 1 to Q is the same as that from Q to 2.

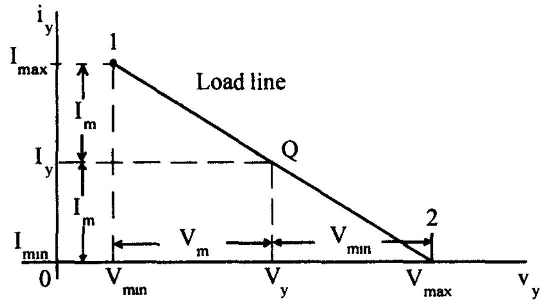


Fig. 4.7 Transfer Curve

In the case of transformer coupled amplifier, supply voltage is only V_y and not V_{max}, since the DC drop across transformer can be neglected. In the case of series fed amplifiers, supply voltage V_{yy} is V_{max}.

$$I_y = I_m$$

I_m is the current corresponding to the operating point.
V_m is the voltage corresponding to the operating point.

$$V_m = I_m Z_m = \frac{V_{max} - V_{min}}{2}$$

The general expression for conversion efficiency is

$$\eta = \frac{\text{Signal power delivered to load}}{\text{DC power supplied to output circuit}} \times 100$$

$$P_{ac} = V_m \cdot I_m/2 \qquad P_{DC} = V_{yy} I_y$$

V_m is the peak value or maximum value. Since rms value $= \dfrac{V_m}{\sqrt{2}}$ $\qquad I_m = \dfrac{I_m}{\sqrt{2}}$

$$V_{rms} = \frac{V_m}{\sqrt{2}}$$

$$I_{rms} = \frac{I_m}{\sqrt{2}}$$

$$\therefore \qquad P_{ac} = \frac{(V_m I_m)}{2}$$

$$\eta = \frac{\frac{1}{2} V_m . I_m}{V_{yy} . I_y} \times 100\% \quad = 50 \frac{V_m \, I_m}{V_{yy} \, I_y} \%$$

$$V_m = \text{Peak value} = \frac{1}{2} \text{ (Peak to peak value)}$$

$$V_m = \left(\frac{V_{max} - V_{min}}{2}\right), \; V_{rms} = \frac{V_m}{\sqrt{2}}$$

$$V_m \cdot I_m = \left(\frac{V_{max} - V_{min}}{2}\right) I_y \quad \because I_m = I_y, I_m = \left(\frac{I_{max} - I_{min}}{2}\right); I_{min} = 0$$

$$\eta = \frac{50\left(V_{max} - V_{min}\right) I_y}{V_{yy}\, I_y \times 2}$$

$$= \frac{25\left(V_{max} - V_{min}\right)}{V_{yy}} \%$$

$$\eta = \frac{V_m I_m / 2}{V_{yy}\, I_y} \times 100\%$$

$I_m = I_y$, since transistor will not conduct, if $I_{min} = 0$.

$$P_0 = \frac{(V_{CC} - V_{CE}) I_C}{2}$$

$$I_C = \frac{V_{CC} - V_{CE}}{R_L'} \qquad R_L' = \text{Load resistance referred to primary.}$$

$$P_0 = (V_{CC} - V_{CE})^2 / 2 R_L'$$

$$P_{DC} = V_{CC} \times I_C$$

$$= V_{CC} \left(\frac{V_{CC} - V_{CE}}{R_L'}\right)$$

$$\eta = \frac{P_0}{P_{DC}} \times 100$$

$$= 50 \left\{1 - \frac{V_{CE}}{V_{CC}}\right\}$$

If it is a transformer coupled amplifier, V_Y is the DC voltage. Since Q point is chosen in the middle of the load line, graphically,

$$V_y = \frac{V_{max} - V_{min}}{2}$$

for a transformer coupled amplifier, there is no DC drop across the transformer.

$\therefore \qquad V_{CC} \simeq V_{CE} = V_y$

$\therefore \qquad$ DC input power $= V_y . I_y$

$$V_{yy} = \frac{V_{max} + V_{min}}{2}$$

$$\eta = \frac{25(V_{max} - V_{min}) \times 2}{(V_{max} + V_{min})}$$

$$= \frac{50(V_{max} - V_{min})}{(V_{max} + V_{min})}$$

V_{yy} will be the quiescent voltage itself for transformer coupled amplifier. Since there is no DC voltage drop across the transformer.

If $V_{min} = 0$, maximum efficiency = *50% for class A transformer coupled amplifier.*

For series fed amplifier, $V_{yy} = V_{max} = 2\ V_m$

$\therefore \qquad \eta = \dfrac{25\ (V_{max} - V_{min})}{V_{max}}\%$. If $V_{max} = 0$, maximum $\eta = 25\%$

Therefore for a transformer coupled amplifier conversion η is twice. (50% compared to 25% for series fed amplifier)

4.4 Transformer Coupled Amplifier

In AC amplifier circuits, the input AC signal should be coupled to the amplifier and output of the amplifier should be coupled to the load resistance. The coupling device should be such that, it allows only the AC signal to the amplifier circuits and blocks the DC components present in the signal generator, because we are interested in amplifying only AC signals. For this purpose a capacitor can be used for coupling.

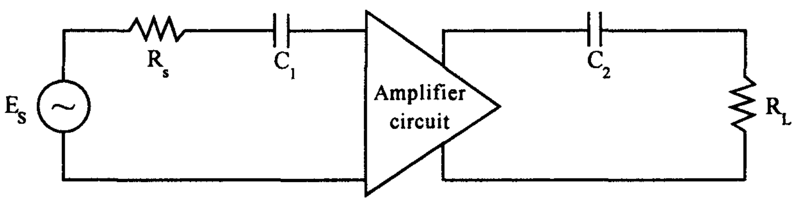


Fig. 4.8 Coupling in amplifier circuits

Types of coupling :

1. Capacitor coupled amplifier 2. Transformer coupled amplifier 3. RC coupled amplifier
4. Direct coupled amplifier 5. Inductor or Tuned amplifier

E_S is the AC signal generator and R_S its source resistance. C_1 and C_2 are the coupling capacitors. They are chosen such that, for the lowest frequency signal to be amplified, X_{C_1} and X_{C_2} are short circuits. But because of these reactive coupling elements, as signal frequency decreases X_C increases. Hence there will be large voltage drop across the capacitor and so the actual input to the amplifier reduces and hence gain decreases. Similarly at high frequencies because of the shunting capacitance C_S, gain falls. Therefore there is a particular frequency range in which gain is of desirable value only.

Instead of capacitors, transformer can also be used for coupling.

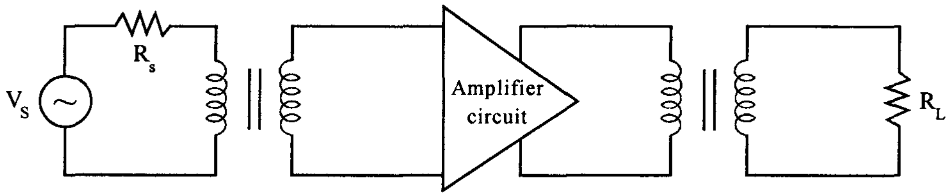


Fig. 4.9 Transformer coupling

Transformer does not respond to DC. Therefore only AC signals from source to the amplifier circuit and from the amplifier to the load will be coupled. But what is the advantage of the transformer coupling ? Suppose, the load resistance R_L is very small $\simeq 4\Omega$, 8Ω or 15Ω as in the case of a loud speaker. The output impedance R_0 of the transistor amplifier is much larger (for common emitter and common base configuration A_V, $A_i >> 1$). Therefore impedance matching will not be there and so maximum power will not be transferred. Even if capacitive coupling is used, impedance matching cannot be achieved. But this can be done using a transformer.

$$R_0 = \left(\frac{N_1}{N_2}\right)^2 .R_L$$

$$\left(\frac{N_1}{N_2}\right) = \text{Turns ratio of transformer}$$

N_1 = Number of turns on primary side.

N_2 = Number of turns on secondary side.

R_0 is much larger than R_L. Therefore $\left(\frac{N_1}{N_2}\right) > 1$ or the transformer that should be used should be a *Stepdown transformer*. Therefore the output voltage at the secondary of the transformer will be much smaller compared to the input voltage since stepping down action is taking place. [This is the case with class A and class B power amplifiers in the case of lab experiment]. But the current amplification will be there and because of Z matching, maximum power will be transferred to the load. Similar to resistive capacitor coupled amplifier, we have the frequency response which depends upon the inductance of the primary and secondary. The transformer on the primary side is chosen such that the source resistance of the generator matches with the input Z of the amplifier circuit. Transformer coupled amplifiers are used in low audio frequency range only because at higher frequencies the X_L of the transformer will be large and so the gain falls.

Another advantage with the transformer coupled amplifiers is the AC current passing through the load resistance R_L results in only wastage of power, since we are interested in only AC output power. Moreover passing DC current through the loudspeaker coil is not desirable since it produces hum or noise. Therefore if transformer coupling is done, DC component of current passing through the transformer can be avoided.

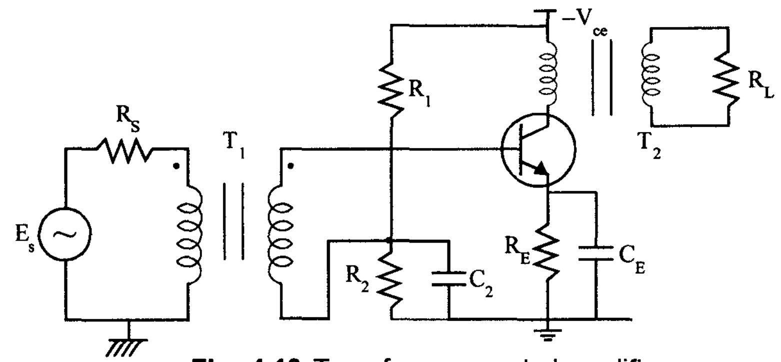


Fig. 4.10 Transformer coupled amplifier

$$\frac{V_1}{V_2} = \frac{I_2}{I_1}; \quad n = \frac{N_2}{N_1} \qquad \text{(For a transformer with usual notation.)}$$

$$V_1 = \left(\frac{N_1}{N_2}\right) V_2; \quad I_1 = \left(\frac{N_2}{N_1}\right) I_2.$$

$$V_1 = \frac{1}{n}.V_2; \; I_1 = n \,.\, I_2 \qquad \text{Therefore } \frac{V_1}{I_1} = \frac{1}{n^2}.\frac{V_2}{I_2}$$

R_1, R_2, R_E are chosen depending upon the biasing point. C_E is emitter bypass resistor. Transformer T_1 is chosen to match R_i of the circuit with R_S and transformer T_2 is chosen for R_0 of the circuit to match with R_L.

$$\therefore \qquad R_L' = \frac{1}{n^2}.R_L$$

C_2 is also a bypass capacitor. For AC it is short circuit.

The equivalent circuit, in terms of h-parameters neglecting the biasing resistors and capacitors, also neglecting the input transformer and considering base and emitter as the input ports.

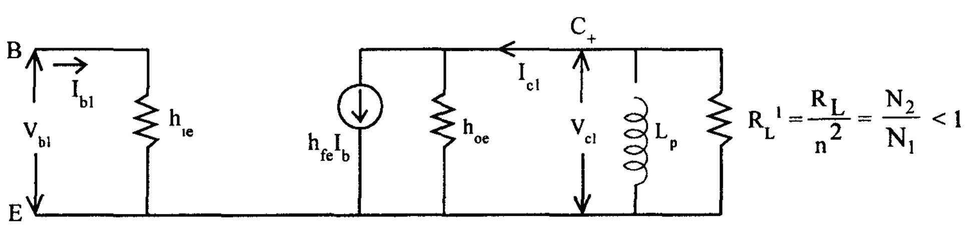


Fig. 4.11 Equivalent Circuit

The transistor is replaced by its h-parameter equivalent circuit. The load resistance R_L is referred to primary and so $R_L' = \frac{R_L}{n^2}$ where $n = \frac{N_2}{N_1}$. Since it is a stepdown transformer, $n < 1$; L_p is the inductance of the primary winding (Since we are considering load referred to primary).

4.4.1 Mid Frequency Range

In the mid frequency range, the inductive reactance X_{LP} is high. f is large and so it can be regarded as an open circuit (or very large compared to R_L'). Therefore it will not affect the response. $h_{fe}\, I_b$ is the current source. When impedance matching is done, the output Z of the circuit and the load resistance R_L will be equal. Therefore the current will get divided between R_L and the circuit equally. The total current is $h_{fe}\, I_b$. Therefore the current through the primary of the transformer (or in other words the current through the collector circuit) is $\frac{h_{fe}.I_b}{2} = I_{C1}$.

But since T_2 is a step down transformer the current through R_L will be stepped up by $\left(\frac{N_1}{N_2}\right)$ due to transformer action $\frac{N_1}{N_2} > 1$.

$$\therefore \qquad I_L = \left(\frac{N_1}{N_2}\right) I_{C1} = \frac{h_{fe}.I_b}{2} \cdot \left(\frac{N_1}{N_2}\right)$$

$$\therefore \text{ Current gain} \qquad \frac{I_L}{I_b} = A_I = \frac{N_1}{N_2} \times \frac{h_{fe}}{2}$$

4.4.2 Voltage Gain

$$A_V = \frac{V_L}{V_b}; \; V_b = \text{base voltage input voltage}$$

$$V_{C_1} = \frac{h_{fe}\, I_b}{2} R_L \left(\frac{N_1}{N_2}\right)^2$$

$$\therefore \qquad \frac{V_{C1}}{V_{b1}} = -\frac{h_{fe}}{2} \times \frac{R_L}{h_{ie}} \left(\frac{N_1}{N_2}\right)^2$$

$$\text{But} \qquad \frac{V_C}{V_L} = \frac{N_1}{N_2}$$

V_C = voltage on primary side of transformer
V_L = voltage on secondary side of transformer

$$\therefore \qquad A_V = \frac{V_L}{V_b} = -\frac{h_{fe}}{2} \times \frac{R_L}{h_{ie}} \times \frac{N_1}{N_2}$$

In the low frequency range shunting effect of L_p will reduce the effective load resistance. Lower 3db frequency is reached when,

$$2\pi f_1 L_p = R$$

or
$$f_1 = \frac{R}{2\pi L_p}$$

where R is the parallel combination of $\frac{1}{h_{oe}}$ and $\left(\frac{N_1}{N_2}\right)^2 . R_L$

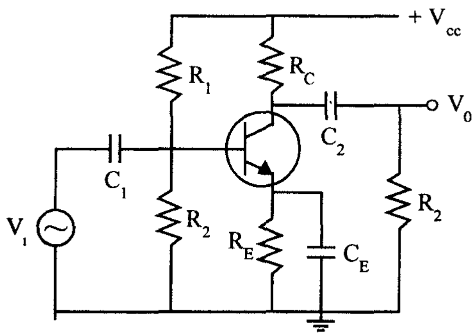


Fig. 4.12 Class A power amplifier circuit

The transformer coupled amplifier circuit is similar to a circuit, like this. Instead of having coupling capacitors C_1 and C_2, we have transformer, coupling. The primary of transformer T_2 acts as R_C. C_2 across R_2 helps in making Emitter of transistor at the ground point for AC. Because of C_E, emitter is at ground potential for AC. Therefore secondary voltage of transformer is applied between base and emitter of transistor.

4.5 Transformer Coupled Audio Amplifier

Audio amplifier	:	40Hz to 20 KHz
Video	:	5-8 MHz
R.F	:	20 KHz

Classification of Radio Waves.

Very low frequency(VLF)	10-30 K Hz
Low frequency (LF)	30-300 K Hz
Medium frequency (MF)	300-3,000 K Hz
High frequency (HF)	3-30 MHz
VHF	30-300 MHz
Ultra high frequency (UHF)	300-3000 MHz
Super high frequency (SHF)	3000-30,000 MHz

An amplifying system usually consists of several stages in cascade. The input and intermediate stages operate in a small signal class-A mode. Their function is to amplify the small excitation to a large value to drive the final device. This output stage feeds a transducer such as CRT, loud speaker, servo motor etc. So the output stage must be capable of delivering a large voltage or current or large power. Bias stabilization techniques and thermal runaways are very important with power amplifiers.

If the load resistance is connected directly in the output circuit as shown in Fig.4.13 (a), the quiescent current passes through R_L. This results in waste of power since it won't contribute to the AC power signal. In the case of loud speakers it is not desirable to pass DC current through the voice coil. So an arrangement is to be made using an output transformer.

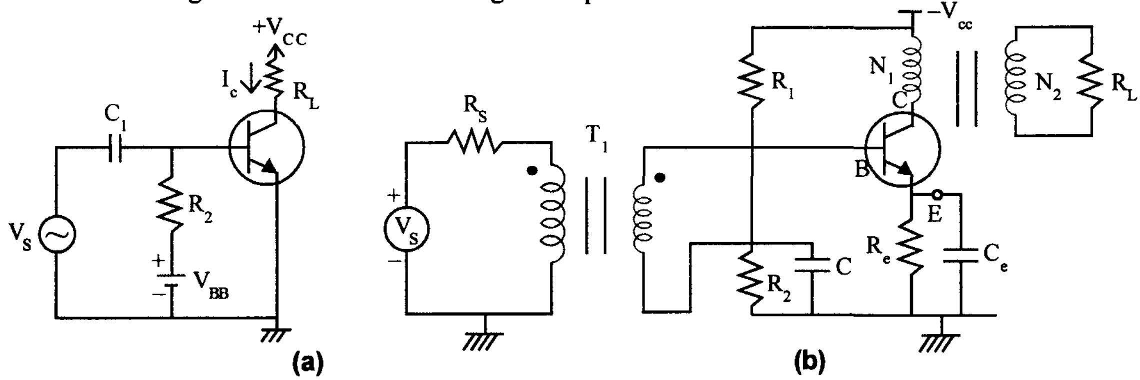


Fig. 4.13 Transformer coupled amplifiers

4.5.1 Impedance Matching

To transfer significant power to a load such as loud speaker with a voice-coil resistance of 5-15Ω it is necessary to use an output matching transformer. The impedance matching properties of an ideal transformer are :

$$\frac{V_1}{V_2} = \frac{N_1}{N_2}; \quad \frac{I_2}{I_1} = \frac{N_1}{N_2}$$

Let $$\frac{N_2}{N_1} = n \text{ turns ratio.}$$

If $N_2 < N_1$ the transformer reduces the output voltage, and steps up the current by the same ratio.

Impedance matching is required because the internal impedance of the device will be much higher than 5-15Ω of voice coil of a speaker. So power will be lost. Hence output matching transformer is required.

$$V_1 = \frac{N_1}{N_2} . V_2 \qquad I_1 = \frac{N_2}{N_1} . I_2$$

$$V_1 = \frac{1}{n} . V_2 \qquad I_2 = n . I_2$$

Now $$\frac{V_1}{I_1} = \frac{1}{n^2} . \frac{V_2}{I_2}$$

$$\frac{V_1}{I_1} = \text{Effective input resistance } R_L'$$

$$\frac{V_2}{I_2} = \text{Effective output resistance } R_L'$$

$$\therefore \qquad R_L' = \frac{1}{n^2} \cdot R_L$$

4.5.2 Maximum Power Output

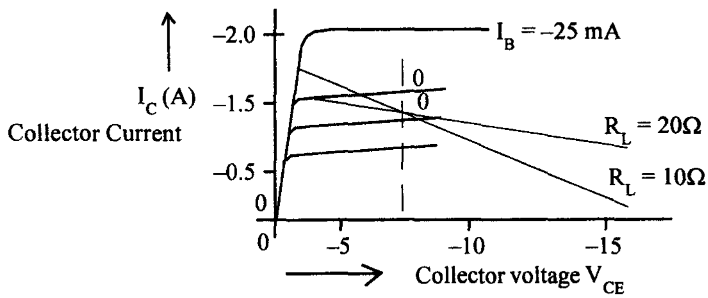


Fig. 4.14 (a) Output characteristics

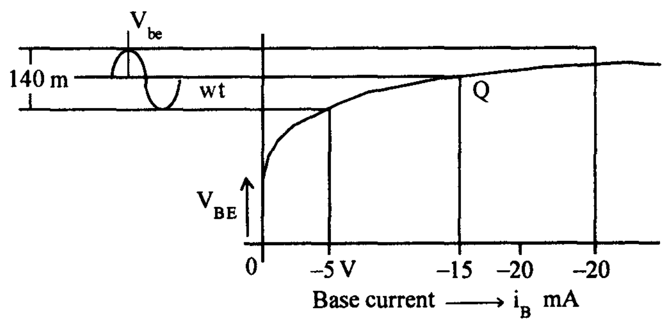


Fig. 4.14 (b) Input characteristics

To find n, for a given R_L, so that power output is maximum is solved graphically. First operating point Q is located $I_C = \frac{V_{CC}}{R_C}$;

P_c = collector dissipation

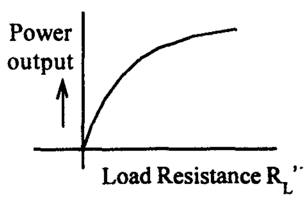


Fig. 4.15 Variation of P_0 with R'_L

V_C = quiescent collector voltage. Peak to peak voltage must be limited to a suitable value such that there is no distortion. From the input characteristic I_{Bmax} to I_{Bmin} can be noted. A series of load lines are drawn through 'Q' point for different values of R_L'. From these two graphs, power output versus load resistance R_L is drawn from the graph, R_L' is chosen that power is maximum and distortion is minimum.

4.5.3 Efficiency

Suppose the amplifier is supplying power to pure resistive load.

Power input from DC supply = $V_{cc}\ I_c$

Power absorbed by output circuit = $I_C^2\ R_1 + i_C^2\ V_C$

R_1 is static load i_C and V_C are rms output current and voltage. If P_D is average power dissipated by the active device.

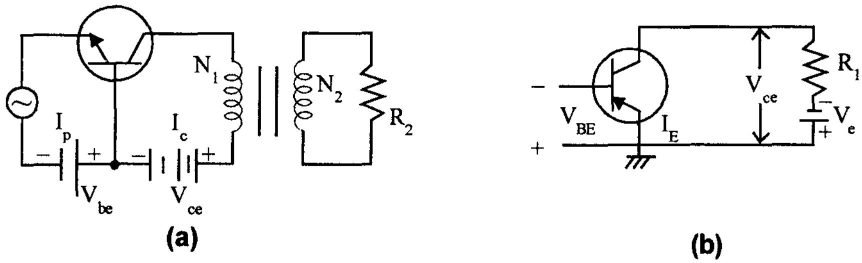


Fig. 4.16 Power amplifier circuit

$$V_{CC}\ I_C = I_C^2\ R_1 + i_C\ v_C + P_D$$

But $$V_{CC} = V_C + I_C\ R_1;$$

$$P_D = V_{CC} \cdot I_C - I_C^2\ R_1 - I_C^2\ V_C$$

$\therefore$ $$P_D = V_C\ I_C + R_1\ I_C^2 - i_C\ v_C$$

$$P_D = V_C\ I_C - i_C\ v_C$$

If the load is not pure resistance, $i_C\ v_C$ must be replaced by $i_C\ v_C \cos\theta$, where $\cos\theta$ is power factor of load.

4.5.4 Conversion Efficiency, η

An amplifier is essentially a frequency converter, changing DC power to AC power.

A measure of the ability of an active device to convert DC power of the supply into AC power delivered to the load is called *conversion (η)* or *theoretical efficiency (η)*. It is also called *collector circuit (η)* for transistor amplifier.

$$\eta \equiv \frac{\text{Signal power delivered to load}}{\text{DC power supplied to input circuit}} \times 100\%$$

In general, $$\eta = \frac{\frac{1}{2} \cdot B_1^2 \cdot R_L'}{V_{CC}(I_C + B_0)} \times 100\%$$

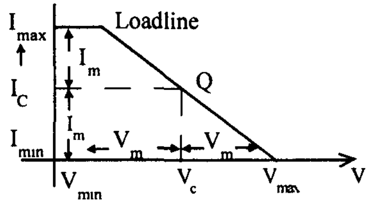


Fig. 4.17 Transfer curve

where B_0 and B_1 are constants in the expression

$$i_C = I_C + B_0 + B_1 \text{ Cos } \omega t + B_2 \text{ Cos } 2\omega t + ...$$

Expression for instantaneous total current.

If distortion components are negligible,

$$\eta = \frac{\frac{1}{2} V_m I_m}{V_{Ce} I_C} \times 100\%$$

$$= \frac{50 V_m I_m}{V_{Ce} I_C} \times 100\%$$

Maximum Value of (η)

In the case of *series fed amplifiers, the supply voltage* V_{CC} is equal to V_{max}. In the transformer coupled amplifier V_{CC} is equal to the quiescent voltage V_C.

Under ideal conditions,

$$I_C = I_m$$

and $$V_m = \frac{V_{max} - V_{min}}{2}$$

$\therefore$ $$\eta = 50 \frac{V_m . I_m}{V_{cc} I_c}$$

$$= \frac{50 \times \left(\frac{V_{max} - V_{min}}{2} \right) \times I_c}{V_{cc} I_c}$$

$$\boxed{\eta = \frac{25 (V_{max} - V_{min})}{V_{cc}} \%}$$

For series fed amplifier, $V_{max} = V_{cc}$

$\therefore$ η for series fed amplifiers

$$= \frac{25(V_{max} - V_{min})}{V_{max}} \%$$

$\therefore$ *Maximum possible value = 25%*

In the case of transformer coupled amplifier.

$$V_{ce} = V_c = \frac{V_{max} + V_{min}}{2}$$

$$\therefore \quad \boxed{\eta = 50\left(\frac{V_{max} - V_{min}}{V_{max} + V_{min}}\right)\%}$$

So the Maximum Possible Value of η is 50% for transformer coupled amplifier

Thus transformer coupled amplifier have twice the maximum η compared to series fed amplifiers. For *transformer circuits* occurs near saturation, therefore $V_{min} << V_{max}$ and η can be 50%.

PNP Transistor Amplifier with AC Signal

Emitter is forward biased. Collector is *reverse biased.*

AC is superimposed at the input, we get AC output across R_L. (Fig. 4.18)

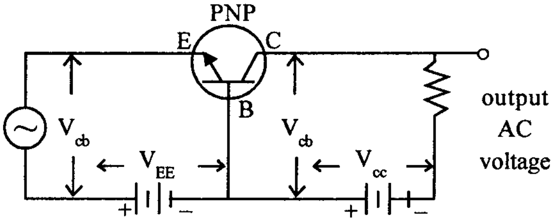


Fig. 4.18 Circuit with PNP transistor

4.6 Push Pull Amplifiers

R_1 and R_2 are provided to prevent cross over distortion. Because of R_1 and R_2 the B-E junctions of the two transistors are forward biased so that cut in voltage V_r will not come into the picture. But because of R_1 and R_2, the operation will be slightly class AB operation and not pure class B operation. For a given transistor, the dynamic characteristics are not exactly linear, that is, for some changes in the values of i_b, i_c will not change by the same amount that is. If i_b is increasing by 5 μA, i_c increases by 1mA. For 10 μA increase in i_b, i_c will not increase by 2 mA but something different. So the graph of

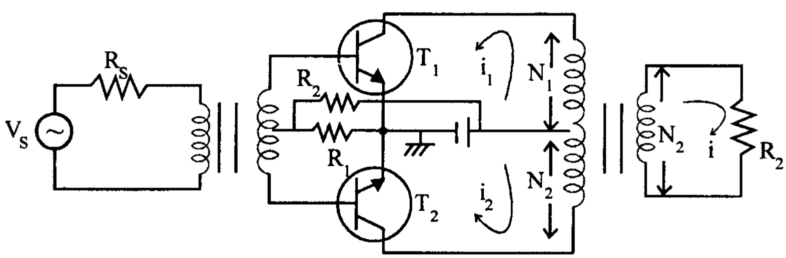


Fig. 4.19 (a) Push Pull amplifier circuit

i_b, V_S i_c is nonlinear. Therefore for uniform changes in the input, the output will not change uniformly. Hence distortion will be introduced in the output waveform. This can be eliminated by pushpull connection.

The efficiency (η) for class A amplifier is 25% and for transformer coupled class A amplifier is 50%. Therefore class A amplifier because of poor η is used for low output power requirement and where conductance should be for complete 360^0. (eg. for the driver stage of the last power stage).

Suppose for the transistor Q_1, the input (base current) is a Cosine wave $x_1 = X_m \cos \omega t$. The output current at the collector $i_1 = I_c + B_0 + B_1 \text{Cos}\ \omega t + B_2 \text{Cos}\ 2\omega t + B_3 \text{Cos}\ 3\omega t$ where I_c is the DC current due to biasing, B_0 is the DC component in the Fourier series of the AC input, B_1 is fundamental component C_m (Transformer T_1 provides phase shift to the inputs. T_2 joins the two outputs. For the second transistor, the input is given from the centre tapped transformer which introduces a phase shift of 180^0.

$\therefore \qquad x_2 = -x_1 = X_m \{\text{Cos}\ (\omega t + \pi)\}$

The output current of this transistor i_2 is obtained by replacing ωt by $(\omega t + \pi)$ in the expression for i_1.

i.e.,
$$i_2\ (\omega t) = i_1\ (\omega t + \pi)$$
$$i_2 = I_C + B_0 + B_1 \text{Cos}\ (\omega t + \pi) + B_2 \text{Cos}\ 2\ (\omega t + \pi) \ .....$$
$$= I_C + B_0 - B_1 \text{Cos}\ \omega t + B_2 \text{Cos}\ 2\omega t - B_3 \text{Cos}\ 3\ \omega t \ .....$$

Therefore i_1 and i_2 are out of phase by 180^0. So they flow in the opposite direction through the output transformer primary windings. Therefore the total output current i is proportional to $(i_1 - i_2)$. Since the net output current depends on the turns ratio of the transformer i is the current flowing through R_L.

$$\therefore \qquad i = K\ (i_1 - i_2) = 2\ K\ (B_1 \text{Cos}\ \omega t + B_3 \text{Cos}\ 3\ \omega t) \ .....$$

This expression shows that all the even harmonic terms $B_2 \text{Cos}\ 2\ \omega t$, $B_4 \text{Cos}\ 4\ \omega t$ are eliminated. The only harmonic component predominant is $B_3 \text{Cos}\ 3\ \omega t$, the III (third) harmonic terms. Higher harmonics can be neglected. $B_1 \text{Cos}\ \omega t$ is the original signal. Therefore *Harmonic distortion will be less for pushpull amplifiers*. This is under the assumption that both the transistors have identical characteristics. If not, some even harmonics may also be present.

Pushpull amplifier is said to possess mirror symmetry.

Mirror symmetry means, mathematically,

$$i\ (\omega t) = -\ i\ (\omega t + \pi)$$

The output current i for pushpull amplifier is,

$$i = 2\ K\ (B_1 \text{Cos}\ \omega t + B_3 \text{Cos}\ 3\ \omega t + \ .....)$$

If ωt is replaced by $(\omega t + \pi)$, the above equation holds good.

This is also called as halfwave symmetry. It means that the bottom loop of the wave when shifted by 180^0 along the axis will be the mirror image of the top. This is so because only odd harmonic terms are there in the output.

The maximum instantaneous reverse voltage across each transistor occurs when it is not conducting and is equal to 2 V_t. Because when Q_1 is conducting, maximum $V_{CE} = 0$ and so voltage across the upper half winding of output transformer primary is V_{CC}. Due to induction some voltage will appear across the lower half also. Q_2 is not conducting. Therefore the transistor voltage across Q_2 collector and emitter is $V_{CC} + V_{Ce} = 2\ V_{CE}$.

It is called as *push pull amplifier* since, the input to the two transistors are out of phase by 180^0. (Since centre tapped transformer is used). Therefore when one transistor is conducting the other is not or when the output current of one transistor is increasing, for the other it is decreasing. This is known as *push pull action*. When one transformer current is being pushed up, the other is being pulled down.

4.6.1 Class B Amplifiers

A transistor circuit is in class B operation, if the emitter is shorted to base (for DC). The transistor will be at cut off. Therefore in the circuit for class B pushpull amplifier, R_2 should be zero. The conduction angle is 180^0.

4.6.2 Advantages of Class B Push Pull Circuit AMPLIFIER

1. More output power ; η = 78.5%. Max.
2. η is higher. Since the transistor conducts only for 180^0, when it is not conducting, it will not draw DC current.
3. Negligible power loss at no signal.

4.6.3 Disadvantages of Class B Push Pull Circuit AMPLIFIER

1. Supply voltage V_{CC} should have good regulation. Since if V_{CC} changes, the operating point changes (Since I_C changes). Therefore transistor may not be at cut off.
2. Harmonic distortion is higher. (This can be minimized by pushpull connection).

Therefore Class B amplifiers are used in a *system* where the power supply is limited, and is to be conserved such as circuits operating from *Solar cells or battery, Battery Cells, air borne, space and telemetry applications*.

4.6.4 Conversion η

$$P_0 = \frac{I_m}{\sqrt{2}} \times \frac{V_m}{\sqrt{2}} = \frac{I_m\ V_m}{2} = \frac{I_m}{2}\left(V_{CC} - V_{min}\right)$$

$V_m = V_{CC} - V_{min}$ (Since operating point is chosen to be at cut off $V_{CC} = V_{max}$)

Because in pushpull circuit, there are two transistors conducting, each for 180^0.

Therefore total conduction is for 360^0. $\left(\therefore P_0 = \frac{I_m V_m}{2}\right)$ Corresponding to Q point,

the voltage is V_{CE}. Neglecting the *dissipation across* emitter, $V_{CC} \simeq V_{CE}$.

$P_{DC} = I_{DC} \cdot V_{CC}$. DC current is drawn by the transistor only when it is conducting. V_{CC} is always present. One transistor conducts for 0-π only. I_{DC} drawn by each transistor is the average value of half wave rectified DC (equal to I_m/π). But there are two transistors.

$\therefore$ Total $\qquad I_{DC} = \dfrac{2I_m}{\pi}$

$$P_{DC} = V_{CC} \cdot \frac{2I_m}{\pi}$$

$$\therefore \qquad \eta = \frac{P_0}{P_{DC}} \times 100$$

$$= \frac{I_m}{2} \frac{(V_{CC} - V_{min})\pi}{V_{CC}.2I_m} \times 100$$

$$= 100 \times \frac{\pi}{4} \frac{(V_{CC} - V_{min})}{V_{CC}}$$

$$\eta = 25 \times \pi \left(1 - \frac{V_{min}}{V_{cc}}\right)\%$$

If $$\frac{V_{max}}{V_{min}} = 1, \qquad \text{Max } \eta = 78.5\%$$

4.6.5 Dissipation of Transistors in Class B Operation

The DC input power to the transistors in class B configuration is

$$P_{DC} = \frac{2I_m.V_{CC}}{\pi}$$

[Since the transistor is conducting for 180^0 only. So it draws DC current only during that period. Therefore average value of i_C is $\frac{I_m}{\pi}$. There are two transistors each conducting for 180^0, from $0 - \pi$ and $\pi - 2\pi$ respectively).

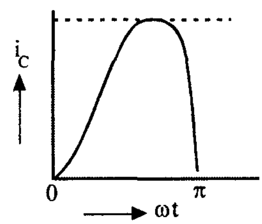


Fig. 4.19 (b) Current cycle

$\therefore$ Total DC current = $2\ I_m/\pi$

$$P_{DC} = \frac{2I_m}{\pi}.V_{CC}$$

But $I_m = \frac{V_m}{R_L'}$ where R_L' is the effective load resistance of the circuit, without considering the secondary of the transformer.

$$\therefore \qquad P_i = \frac{2\,V_m.\,V_{CC}}{\pi R_L'}$$

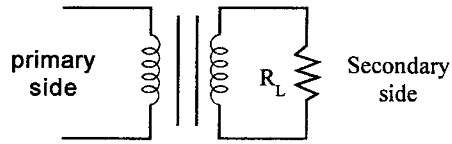


Fig. 4.20 Transformer on load side

The collector dissipation P_C (in both transistors) is the difference between the power input (P_i or P_{DC}) to the collector circuit, and the power delivered to the load. (Both are in watts). Though DC and AC powers.

Output power delivered to load P_0,

$$P_0 = \frac{V^2}{R} = \left(\frac{V_m}{\sqrt{2}}\right)^2 \Big/ R_L'$$

$$= \frac{Vm^2}{2R_L'}$$

$$\therefore \qquad P_C = P_i - P_0 = \left[\frac{2}{\pi}.\frac{V_{CC}V_m}{R_L'}\right] - \left(\frac{V_m^2}{2R_L'}\right)$$

(V_m is the peak value of the AC input).

The above equations shows that at no AC signal, (i.e., $V_m = 0$) the collector dissipation is zero, and as the signal magnitude increases, P_C increases. As V_m increases P_C also increases, P_C is maximum when $V_m = \frac{2V_{CC}}{\pi}$.

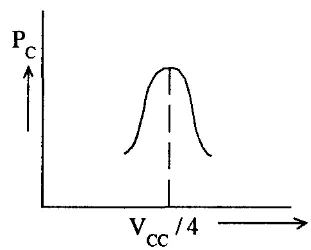


Fig. 4.21 Power output

A graph can be plotted between P_C and V_m

The maximum dissipation

$$P_{C\,max} = \frac{2V_{cc}^2}{\pi^2 R_L'}$$

P_C is maximum, when $V_m = \frac{2V_{CC}}{\pi}$

P_0 is maximum, when $V_m = V_{CC}$

$$\therefore \qquad P_{0\,(max)} = \frac{V_{CC}^{\,2}}{2R_L'} \qquad \text{Since } P_0 = \frac{V_m^2}{2R_L}$$

P_0 is maximum $\quad V_m = V_{CC}$

$$\therefore \qquad P_{C\,(max)} = \frac{4}{\pi^2}\,(P_0 \max)$$

$$\boxed{P_{C\,(max)} = 0.4\,P_{0\,(max)}}$$

$\therefore$ If we want to deliver 10-W of output by a class B pushpull amplifier, the collector of the transistor or the collector dissipation should be $0.4 \times 10 = 4$W. This is for the entire circuit. Therefore each transistor (Since there are two transistors in class B pushpull) should be capable of dissipating 2W of power as heat.

4.6.6 Graphical Construction for Class B Amplifier

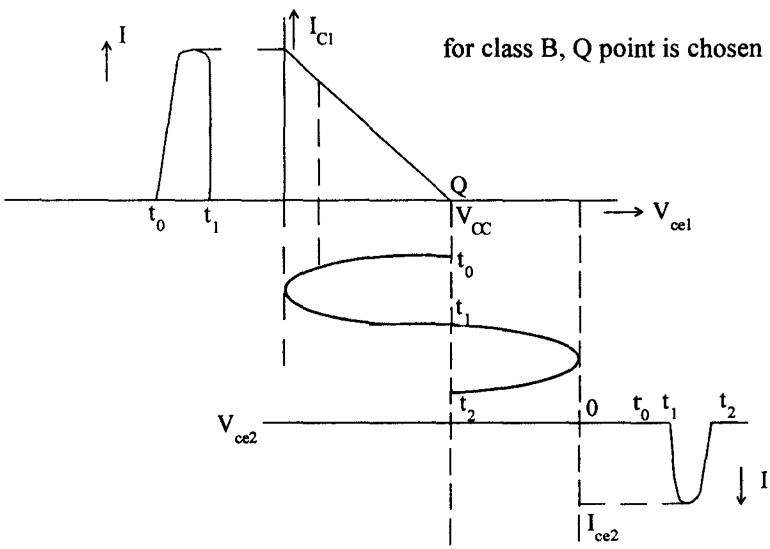


Fig. 4.22 Class B operation

4.6.7 Distortion

Let i_{b_1}, V_C, V_{b_1} be the input characteristic of the first transistor and i_{b_2}, V_S, V_{b_2} is the input characteristic of the second transistor. V_γ is the cut in voltage. These are the two transistors of the class B pushpull amplifier. Now the base input voltage being given to the transistor is sinusoidal, i.e., base drive is sinusoidal. So because of the *cut in voltage*, eventhough input voltage is present, output will not be transmitted or there is distortion in the output current of the transistor. This is known as *crossover distortion.* But this will not occur if the base current drive is sinusoidal. Since in the graphical analysis the input current is taken in the I quadrant. No distortion if the operating point is in the active region. Cross-over distortion can also be eliminated in class AB operation. A small stand by current flows at zero excitation. The input signal is shifted by constant DC bias so that the input signal is shifted by an amount V_γ.

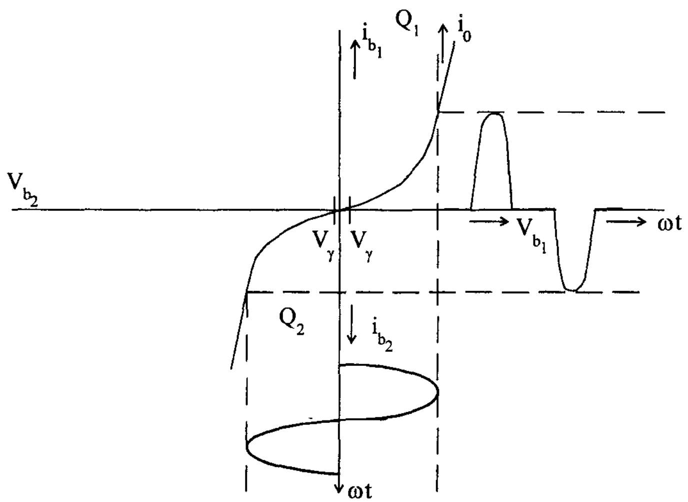
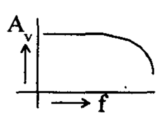
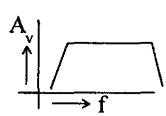
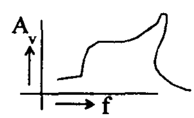


Fig. 4.23 Cross Over Distortion

Table 4.1 Comparison of amplifiers based on the type of Coupling.

	Direct coupled	**R.C. coupled**	**Transformer coupled**
Frequency range :	D.C to medium range	High	A.F. range
f_1 (Lower cutoff frequency	0 Hz (D.C)	50–100 Hz and above	100 Hz and above
f_2 (Upper cutoff frequency)	Limited	Can be more	Limited to A.F range
Cost	Less No R and C No transformer	Medium (Due to R and C)	High (Due to transformer)
Size	Less	Medium	High
Frequency response			 (due to L of tansformer spike occurs)
|Z| matching	Not good	Not good	Excellent

4.7 Complimentary Symmetry Circuits (Transformer Less Class B Power Amplifier)

The standard class B push-pull amplifier requires a centre tapped transformer, since only one transistor conducts for 180^0, so that if two transistors were to conduct for complete 360^o, there should be a centre tapped transformer. Otherwise there should be a phase inverter. Complementary symmetry circuits need only one phase. They don't require a centre tapped transformer. But their requirement is a pair of closely matched. Oppositely doped (pnp and npn) transistors. Till recently it was different to get such transistors. But now the technology has improved and pnp and npn transistors with identical circuits, can be manufactured.

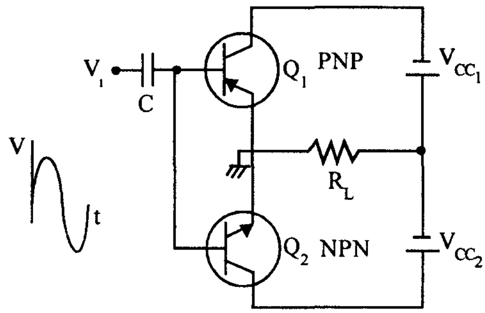


Fig. 4.24 Complimentary Symmetry

The circuit shows a basic complimentary circuits in class B. It is class B operation since the operating point is at cutoff. Emitter and base are shorted or $V_{BE} = 0$. The input is capacitance coupled. The output is direct coupled since output is taken directly across R_L. One end of R_L is grounded with no input signal present. Both transistors won't conduct. Therefore current through $R_L = 0$. When the signal (input) is positive going, the transistor Q_1 is cutoff (since it is pnp), base is n type. Therefore. Emitter-Base junction is reverse biased). Q_2 conducts, since it is NPN transistor, base input is positive. So it conducts.

The resulting current flows through R_L and develops a negative going voltage at point relative to ground. When the signal is negative going Q_2 goes off and Q_1 turns on. Current flows through R_L in such a direction as to make point positive with respect to ground. *There is no DC current through R_L. Hence an electromagnetic load such a loud speaker can be connected* directly without introducing saturation problems.

The difficulty with the above circuit is, the transistor will not conduct till the input signal magnitude exceeds the cut in voltage V_v. So cross over distortion will be present output of the

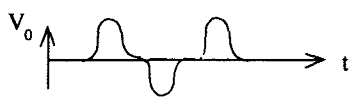


Fig. 4.25 Output with crossover Distortion

So DC bias should be provided to overcome the threshold voltage for each base-emitter junction. Therefore the circuit is as shown in Fig. 4.26(a). The voltage developed across R_2 forward biases both the transistors, E-B junctions. R_2 is normally so small as not to produce any significant loss in drive to Q_2.

This circuit needs only one V_{CC} Q_1 is NPN transistor. Therefore its collector is reverse biased, since V_{CE} is positive.

Q_2 is PNP, its collector is negative with respect to V_{CE} since grounded. Therefore its collector is also reverse biased. The drop across R_3 reverse biases the common base junction of Q_2 and the drop across R_1 reverse biases the Common Base junction of Q_1. This circuit requires only one DC supply and is commonly referred to as the "*Totem pole*" configuration. When the input is positive, Q_1 is turned on and Q_2 is turned off. When the input goes negative, Q_1 turns off while Q_2 conducts.

4.8 Phase Inverters

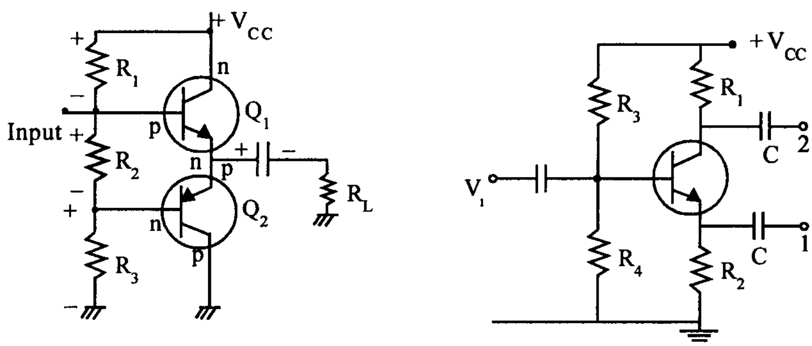
These circuits are used to drive push pull amplifiers since a pushpull amplifier requires two equal inputs with 180^0 phase difference. *The centre tapped* transformers are *bulky and costly.* Therefore Phase inverter circuits with transistors are used.

Phase inverter circuits are also known as *Paraphase amplifiers*. The criterion is, from a single input, we must get two equal outputs with a phase shift of 180^0.

$$V_{01} = -V_{02}$$

The circuit is as shown in Fig. 4.26(b), emitter followers with a collector load R_1 is used.

R_3 and R_4 are bias resistors. R_1 is the collector load. R_2 is the emitter load. Output is taken after the capacitor 'C' to block DC. V_i is AC input. The outputs at points 2 and 1 will be out of phase



(a) (b)

Fig. 4.26 Phase Inverter Circuits

by 180^0. With $R_1 = R_2$ output voltages will be the same. The output impedance of the circuit from point 1 is that of a common collector configuration (Since output is taken across R_2. So it is common collector configuration).

The output impedance at terminal 2 is that of common emitter configuration. So both will not be the same since $R_{OE} \neq R_{OC}$, since output voltages at points 1 and 2 will not be the same. So for that, another transistor is used to match the gains and source impedances for common emitter collector. There is phase shift of 180^0. Therefore V_{02} will be with phase shift for common capacitor configuration there is no phase shift. Therefore V_{01} is in phase. Therefore V_{01} and V_{02} are out of phase by 180^0.

Example : 4.1

The amplifier shown is made up of an NPN and PNP transistors. The h-parameters of the two transistors are identical and are given as $h_{ie} = 1\ K\Omega$, $h_{fe} = 100$, $h_{oe} = 0$ $h_{re} = 0$.

Find overall voltage gain $A_V = V_0/V_i$

Both the transistors are in common emitter configuration. For Q_2 the output is taken across 5 KΩ the collector resistor R_{C_2} which is actually the load resistor.

$$R_{C_1} = R_{L_1} = 2\ k\Omega$$

$$R_{C_1} = 1\ k\Omega$$

$$A_I = \frac{I_C}{I_b} = -\frac{h_{fe}.I_C}{I_C} = -h_{fe}$$

$\therefore$ $R_0 = h_{ie} + (1 + h_{fe})\, R_e \qquad (1 + h_{fe})\, R_e >> h_{ie}$

$$R_i = \frac{V_i}{I_b} = h_{ie} + (1 + h_{fe})\, R_e$$

$$[(1 + h_{fe})\, R_e >> h_{ie}]$$

$\therefore$ $R_i = (1 + h_{fe})\, R_e$

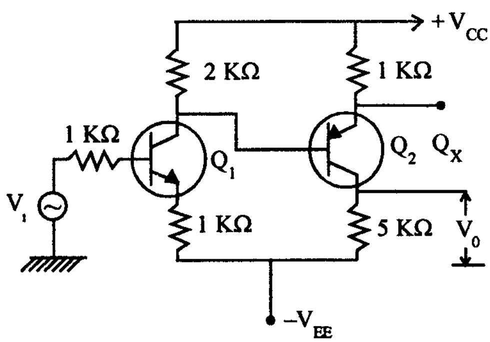


Fig. 4.27 Circuit for Ex : 4.1

$$A_V = \frac{A_I.R_L}{R_i}; \quad A_I = h_{fe}$$

$\therefore$ $A_V = \frac{-h_{fe}.R_L}{(1 + h_{fe})R_e} \quad [1 + h_{fe} \simeq h_{fe}]$

$$A_V = \frac{R_L}{R_e} = \frac{R_L}{R_e}$$

$$A_{V_2} = \frac{R_{L_2}}{R_{C_2}} = \frac{-5K\Omega}{1K\Omega} = 5$$

$$A_{V_1} = \frac{2K\Omega}{1K\Omega} = \frac{R_{L_1}}{R_{C_1}} = 2$$

$\therefore$ $A_V = A_{V_1} \times A_{V_2} = 5 \times 2 = 10$

Example : 4.2

Design a class B power amplifier to deliver 30W to a load resistor $R_L = 4\Omega$ using a transformer coupling. $V_m = 30V = V_{CC}$. Assume reasonable data wherever necessary.

Solution :

The power to be delivered is 30W. Assume 10% losses in the transformer windings, and design the circuit for 20% over load i.e., even by mistake, if excess current is being drawn or even voltage applied, the transistor must with stand this.

∴ P_0 is taken as 40W. 30 + 7W (overload) + 3W (transformer losses)

∴ The collector dissipation of the transistor

$$P_C\,(max) = 0.4\, P_0\,(max)$$

∴ The transistor to be chosen must be capable of dissipating $P_C\,(max) = 0.4 \times 40 = 16$ W

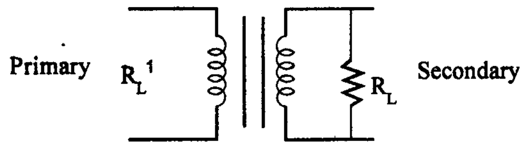


Fig. 4.28 Circuit for Ex : 4.2

$$P_0 = \frac{V_m^2}{2R_L'}$$

$$40 = \frac{(30)^2}{2 \times R_L'}$$

$$\therefore \quad R_L' = \frac{(30)^2}{2 \times 40}$$

$$\therefore \quad R_L = 11.25\ \Omega$$

∴ R_L is the resistance of transformer secondary referred to primary.

$$\frac{R_L'}{R_L} = \left(\frac{N_1}{N_2}\right)^2$$

$$\because \quad V_P I_P = V_S I_S$$

$$\frac{V_P}{V_S} = \frac{I_S}{I_P} = \frac{N_1}{N_2}$$

∴ The turns ratio of the output transformer is,

$$\frac{N_1}{N_2} = n = \left(\frac{R_L^1}{R_L}\right)^{1/2} = \left(\frac{11.25}{4}\right)^{1/2} = 1.7$$

Peak collector current swing

$$I_m = \frac{V_m}{R_L} = \frac{V_{CC}}{R_L} = \frac{30}{11.25} = 2.666 \text{ Amperes}$$

Example : 4.3

Design a class A transformer coupled amplifier, using the transistor, to deliver 75 mW of audio power into a 4Ω load. At the operating point, $I_B = 250\ \mu A$, $V_{CC} = 16V$. The collector dissipation should not exceed 250 mW. $R_L' = 900\ \Omega$. Make reasonable approximations wherever necessary.

$V_{CE} = \frac{V_{CC}}{2}$ for biasing in normal amplifier. If it is transformer coupled, $V_{CE} \simeq V_{Ce}$

Collection dissipation = $I_C \cdot V_{CE}$ (I_C is the collector current at operating point).

$$V_{CE} \cdot I_C \simeq P_{D\,max}$$

or $$V_{CC} \cdot I_C \simeq P_{D\,max}$$

$$I_C \simeq \frac{P_{D\,min}}{(V_{CC} - IV)};$$

Because, the DC. drop across the transformer $V_{CC} \simeq V_{CE}$ can be neglected. The drop across R_E is small $\simeq$ IV. Therefore $V_{CE} \simeq V_{CC} - V = 15$ V.

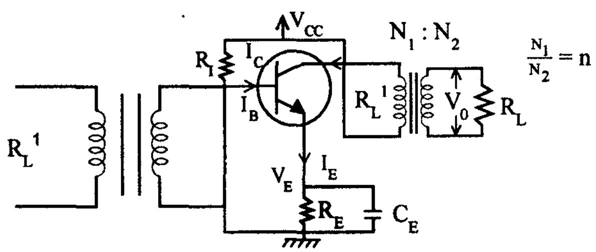


Fig. 4.29 Circuit for Ex : 4.3

$V_{CE} = 16V$. There will be some voltage drop across R_E and the primary winding of the transformer. Therefore V_{CE} can be approximately taken as 15V.

$$\therefore \quad I_C = \frac{P_{D\,min}}{V_{CE}} = \frac{250}{15}$$

$$= 16.66 \text{ mA}$$

Assuming that transformer primary resistance negligible,

$$V_E = V_{CC} - V_{CE}$$

$$= 16 - 15 = IV\ (DC)$$

$$I_E \simeq I_C = 16.66 \text{ mA (DC)}$$

$$\therefore \quad R_B = \frac{V_E}{I_E} = \frac{IV(DC)}{16.66\,mA} = 60\Omega$$

At $f = 50$ Hz, $X_E = \dfrac{R_E}{10} = \dfrac{60}{10} = 6\Omega$

$$\therefore \quad C_E = \frac{1}{2\pi f X_E} = \frac{1}{2\times3.14\times50\times6} \simeq 53\ \mu f$$

$R_L' = 900\ \Omega \qquad R_L = 4\ \Omega$

$\therefore$ Transformer turns ratio

$$= \sqrt{\left(\frac{R_L'}{R_L}\right)}$$

$$n = \frac{N_1}{N_2} = \sqrt{\left(\frac{900}{4}\right)} = 15$$

$\because$ It is Germanium transistor, $V_{BE} = 0.25V$

$$\therefore \quad V_B = V_E + V_{BE} = 1 + 0.25 = 1.25V$$

Assuming that the current through R_1 is 10 I_B,

$$I_{R_1} = 250\ \mu A \times 10 = 2.5\ mA$$

Neglecting the loading effect due to base of the transistor and assuming that I_B, flows through R_L also

$$R_2 \simeq \frac{V_B}{I_{R_1}} = \frac{1.25}{2.5 mA} = 0.5\ K\Omega$$

$$R_1 = \frac{V_{CC} - V_B}{I_{R_1}} = \frac{16-1.25}{2.5\ mA} = 5.9\ K\Omega$$

4.9 Class D : Operation

These are used in *transmitters* because their efficiency (η) is high $\simeq$ 100%.

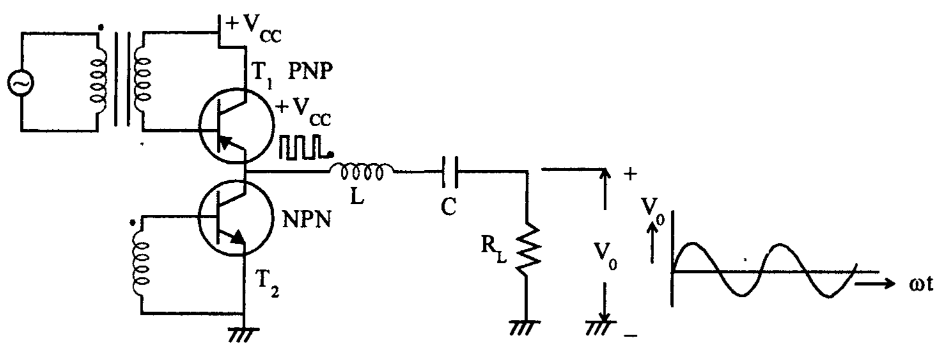


Fig. 4.30 Class D amplifier circuit

A pushpull connection of two transistors in common emitter configuration of complementary transistors (one pnp the other npn) is employed. When the input is positive, T_1 is cut off and T_2 saturates. During the negative half cycle of the input, T_1 saturates and T_2 is cutoff. Therefore the output voltage is a square wave with voltage changing between 0 and V_{CC}.

The dot convention for transformer is, when input is positive, the dotted end of the primary is positive. At the same time, the dotted end of upper secondary winding is positive and dotted end of lower secondary winding is positive. So when the input is positive, T_1 base which is n type (pnp) gets positive voltage. So T_1 is cutoff. Therefore $V = V_{CC}$. When input is negative, T_2 base which is p type (npn) will get negative voltage. So T_2 is cutoff T_1 saturates.

In this circuit, each transistor is saturated for almost 180^0 of the cycle. So each transistor acts like a switch rather than like a current source. When the transistor saturates, the power dissipation.

$$P_D = V_{CE\,(sat)}\; I_{C\,(sat)}$$

It is very small, since $V_{CE\,(sat)}$ is near zero. When the transistor is cutoff, $P_D \simeq 0$. Therefore average power dissipation over the cycle is very small. Therefore $\eta \simeq 100\%$. 

The output of the collectors of transistors, is a square wave with 0 - V_{CC} voltages. This is given to a *series resonant* circuit. So the output will be a sine wave (like oscillator circuits).

4.10 Class S : Operation

Switching regulators are based on class 'S' operation.

In class S operation, a string of pulses are used as the input signal. The pulses have a width 'W', and a period 'T'. Therefore duty cycle $= \dfrac{W}{T} = D$.

4.10.1 Circuit

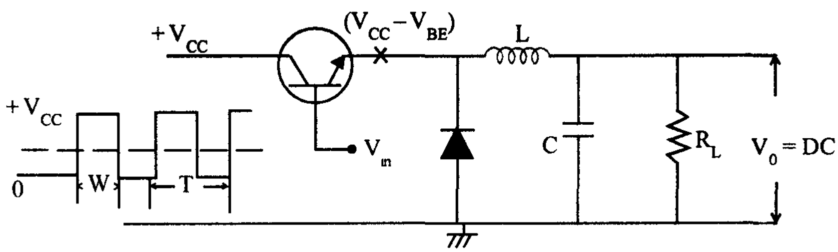


Fig. 4.31 Class S amplifier

The transistor is an emitter follower driven by a train of pulses. Because of the V_{BE} drop, the voltage driving the LC filter is a train of pulses with an amplitude of

$$V_{CC} - V_{BE}. \qquad \text{If } X_L > X_C$$

$$V_{DC} = D\,(V_{CC} - V_{BE})$$

where $$D = \frac{W}{T} = \text{Duty cycle}$$

The higher, the duty cycle, the larger, the DC output. By varying the duty cycle, we can control the a.c. output. So this is class 'S' operation. Because the transistor is cutoff or in saturation its power dissipation is much lower than that in a series regulator. So heat sinks can be small.

Diode rectifies and L, C combination filters the output. So the output is rectified and filtered.

Class A : Conduction of plate current is for complete 360^0, it depends upon operating point.

Class B : Conduction of plate for only 180^0 because the grid is more negative during negative cycle of the signal.

Class C : Conduction is for less than 180^0.

Class AB : Conduction is between 360 and 180^0

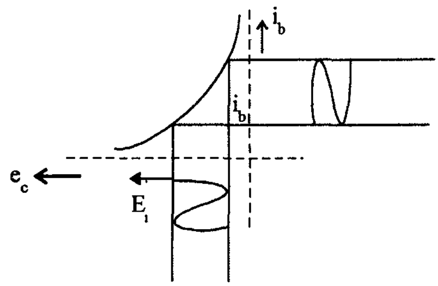


Fig. 4.32 Input output waveforms

Class A	Class B
Less power	More power
Lesser η	More η upto 78.5%
Less Harmonic distortion	Harmonic distortion is more

Example : 4.4

Design a class A power amplifier to deliver 5V rms to a load of 8 Ohms using a transformer coupling. Assume that a supply of 12V is available. The resistance of the primary winding of the transformer also should be considered.

Solution :

1. **First select a suitable transistor**

The power output required is

$$= \frac{(V_{orms})^2}{R_L} = \frac{5 \times 5}{8} = \frac{25}{8} = 3.125\text{W}$$

Assuming a transformer efficiency, η, of 90%, we have, the power required of the amplifier

$= P_0 / \eta$

$= 3.125/0.9 = 3.47\text{W}$

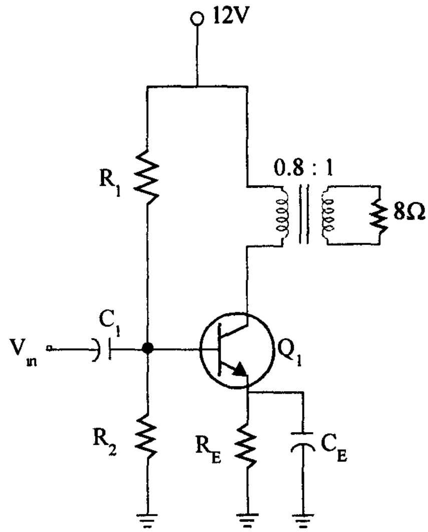


Fig. 4.33 Class A Power Amplifier

Therefore, we shall have to design the amplifier for 3.47W. Since the maximum efficiency of the transformer-coupled power amplifier is 50%, the power dissipation capability of the transistor should be at least 3 to 4 times the power required to be developed.

For the transistor, therefore, the $P_{d(max)}$ should be

$$= 3.47W \times 3$$

$$= \text{about } 10.41W$$

Let us select a transistor, EC3054, for the purpose.

This transistor has

$$P_{d(max)} = 30W \text{ at } 25^0C$$

$$I_{c(max)} = 4A$$

$$V_{CE(sat)} = 1V.$$

2. Choosing Q-point

For transformer coupled amplifier, ideally, $V_{CEQ} = V_{CC}$. We shall assume the voltage across the resistance R_E as about 20% of the supply voltage, i.e.,

$$V_E = 0.2 \times 12 = 2.4V$$

Since $V_{CE\,(sat)} = 1V$, and also to avoid the distortion near the saturation region, we shall take the quiescent point voltage.

$$= V_{CEQ} = \text{about } 2/3\text{rd } V_{CC}, \text{ giving us}$$

$$V_{CEQ} = 8V$$

The maximum swing available will be about 1V less ($V_{CE\,(sat)} = 1V$) than the supply voltage of 12 volts.

Hence for a power of 3.47W, we have,

$$3.47 = \frac{V_P}{\sqrt{2}} \times \frac{I_P}{\sqrt{2}}$$

giving $I_P = 1.21$ Amps.

Therefore, the Q-point is at 8V, 1.21A.

3. Choosing R_E

We have assumed voltage across the resistance R_E as equal to 2.4V, being about 20% of the supply voltage V_{CC}.

Therefore,
$$R_E = \frac{V_{RE}}{I_{CQ}} = \frac{2.4V}{1.12A}$$
$$= 2.2\Omega.$$

which is the nearest available standard value of the resistance. Let us recalculate the voltage across the resistance R_E.

The voltage $\quad V_{RE} = 1.21A \times 2.2\Omega = 2.662$ Volts

The power dissipation of the resistance

$$R_E = (1.21\ A)^2 \times 2.2\Omega$$
$$= 3.22 \text{ Watts.}$$

Hence, we select the resistance

$$R_E = 2.2 \text{ Ohms, 10 Watts.}$$

4. Turns Ratio of Transformer

Secondary voltage = 6V (rms).

Let us calculate the primary voltage and, hence, the turns ratio. At Q-point, the DC voltage across the primary is

$$= V_{CC} - V_{CEQ} - (I_{CQ} \times R_E)$$
$$= 12 - 8 - (1.21 \times 2.2)$$
$$= 1.4V.$$

Giving DC resistance of the transformer

$$R_{primary} = 1.4V/1.21A$$
$$= 1.16 \text{ ohms.}$$

The equivalent resistance on the primary of the transformer is equal to $R_{ac} - R_{primary}$

$$= \frac{V_P}{I_P} - R_{primary}$$
$$= (11 / 1.21) - 1.16$$
$$= 7.93 \text{ Ohms}$$

The turns ratio $= \dfrac{6}{7.93}$

$= 0.76 \simeq 0.8.$

5. Choosing Resistance R_1 and R_2

Assuming $R_B = 10$ times R_E, for good stability, we have,

$$\frac{R_1 \times R_2}{R_1 + R_2} = 10\ R_E \qquad .....(1)$$

Also, since $V_E = 2.4V,\ V_B = 3V$

we have $\quad 3 = \dfrac{R_2}{R_1 + R_2} \times 12$

or $\quad R_1 = = 3\ R_2 \qquad .....(ii)$

From equations (i) and (ii) above, we have

$R_1 = 88\ \Omega.$

$R_2 = 28.6\ \Omega.$

We select the nearest available values, as

$R_1 = 100\ \Omega.$

$R_2 = 33\ \Omega.$

The power rating of these resistances are as under,

For $\quad R_1 = \dfrac{(V_{R1})^2}{R_1} = \dfrac{(18-3)^2}{100} = 2.25W$

For $\quad R_2 = \dfrac{(V_{B2})^2}{R_2} = \dfrac{3^2}{33} = 0.27\ W$

Hence, we select, $R_1 = 100$ Ohms, 5 Watts.

$R_2 = 33$ Ohms, 1 Watts.

Let us calculate the maximum undistorted power available, which is equal to $\left(V_p / \sqrt{2}\right) \times \left(I_p / \sqrt{2}\right)$

$= \left(11/\sqrt{2}\right) \times \left(1.21/\sqrt{2}\right)$

$= 6.66$ Watts, which is more than the required values.

The circuit efficiency :

Useful power output $= 6.66$ Watts.

Power input $= V_{CC} \times I_{CQ} + \dfrac{(V_{CC})^2}{R_1 + R_2}$

$= 14.52 + 1.082 = 15.60$ Watts.

The circuit efficiency, is, therefore,

$= (6.66 / 15.6) \times 100$

$= 42.7\%$

Likewise, let us calculate the transistor power dissipation when no signal is applied, which is

$= V_{CEQ} \times I_{CQ}$

$= 8V \times 1.21A$

$= 10W \simeq$ Watts.

The power dissipation when the rated power is delivered

$= 10W - 6.66W$

$= 4W$

4.11 Heat Sinks

The purpose of heat sinks is to keep the operating temperature of the transistor low, to prevent thermal breakdown. Due to increase in temperature, I_{CO} increases. Due to increase in I_{CO}, I_C increases and hence power dissipation increases. Due to this, temperature increases and thus it is a cummulative process. Due to this, the transistor will fail or breakdown occurs. To prevent this, heat sinks are used to dissipate power to the surroundings and keep the temperature low.

The heat is transferred from the die to the surface of the package or casing of the ambient by convention, from the surface to the ambient by convention and radiation. If heat sink is used, the heat is transferred from the package to heat sink and from heat sink to the ambient. Heat sink expedites the power dissipation and prevents breakdown of the device.

The rise in temperature due to power dissipation is expressed as *Thermal Resistance* expressed in ^{0}C/w, and is symbolically represented as θ. It is the rise in temperature in ^{0}C due to 1W of power dissipation. The equations governing this are,

$$\theta_{ja} = \theta_{jc} + \theta_{cn} + \theta_{na}$$
$$\theta_{jc} = (T_j - T_c) / P$$
$$\theta_{cs} = (T_c - T_s) / P$$
$$\theta_{sa} = (T_s - T_a) / P$$

θ_{ja} = Junction to ambient thermal resistance

θ_{jc} = Junction to casing thermal resistance

θ_{cs} = Casing to heat sink thermal resistance

θ_{sa} = Heat sink to ambient thermal resistance

T_j = Average junction temperature

T_c = Average case temperature

T_{sa} = Average heat sink temperature

T_a = Ambient temperature

P = Power dissipated in Watts.

Example : 4.5

What is the junction to ambient thermal resistance for a device dissipating 600 mW into an ambient of 60^0C and operating at a junction temperature of 120^0C.

Solution :

Here heat sink is not considered.

$$\therefore \qquad \theta_{ja} = \theta_{jc} + \theta_{ca}$$

$$\theta_{ja} = \frac{T_j - T_C}{P} + \frac{T_C - T_a}{P}$$

or
$$\theta_{ja} = \frac{T_j - T_C + T_c - T_a}{P} = \frac{T_j - T_a}{P}$$

$$\theta_{ja} = \frac{120 - 60}{0.6} = \frac{60}{0.6}$$

$$= \mathbf{100\ {}^0C/W}$$

For Transistor devices, the heat sinks are broadly classified as :

1. Low Power Transistor Type.
2. High Power Transistor Type.

Low Power Transistors can be mounted directly on the metal chassis to increase the heat dissipation capability. The casing of the transistor must be insulated from the metal chassis to prevent shorting.

Beryllium oxide insulating washers are used for insulating casing from the chassis. They have good thermal conduetivity.

Zinc oxide film silicon compound between washer and chassis, improves the heat transfer from the semiconductor device to case to the chassis.

High Power Transistor heat sinks.

re TO-3 and TO-66 types. These are diamond shaped. For power transistors, usually, the ease itself in the collector convention and radiation is shown in Fig. 4.34. The thermal resistance of the heat sinks will be typically $3^0C/W$.

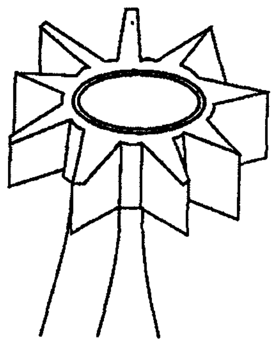


Fig. 4.34 Fin-type heat sink

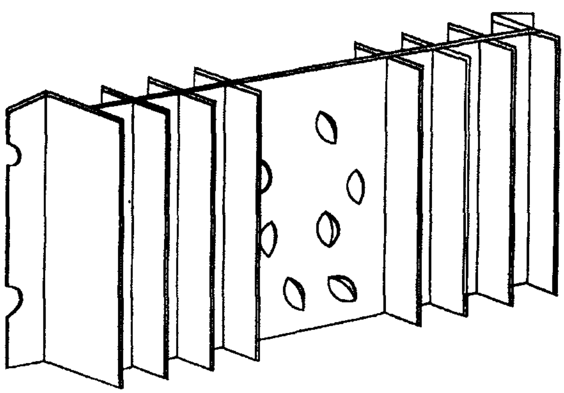


Fig. 4.35 Power transistor heat sink

Objective Type Questions

1. Amplifiers are classified based on
   (a) (b) (c) (d)
2. If the magnitude of signal is small and operating point swing is within the active region, that amplifier is classified as ______________.
3. Different types of coupling employed in amplifier circuits are
   (a) (b) (c) (d)
4. Due to the input signal swing, if the operating point shifts into cut off and saturation regions, that amplifier is classified as ______________.
5. Conduction angles of large signal amplifiers are ______________________.
   (a) Class A ______________ (b) Class B ______________
   (c) Class AB ______________ (d) Class C ______________
6. In class A power amplifiers the operating point Q is in ______________ of dynamic transfer curve of the active device.
7. In class B amplifiers, the Q point is set ______________.
8. In class C amplifiers the operating point is set ______________.
9. Maximum theoretical efficiency of series fed amplifiers is ______________.
10. Maximum efficiency of transformer coupled amplifiers is ______________.
11. The frequency range in which transformer coupled amplifiers are used is ______________.
12. The maximum theoretical efficiency of class B push pull amplifier is ______________.
13. For mirror symmetry or half wave symmetry, the mathematical equation is ______________.
14. In push pull configuration, type of harmonics eliminated are ______________.
15. In class B amplifiers, relation between maximum collector power dissipation P_C (Max) and maximum output power dissipation P_O (Max) is ______________.
16. Cross over distortion occurs because of ______________ characteristic of E - B junction of the transistors.
17. Transformerless class B power amplifier circuit is ______________.
18. Complimentary symmetry circuit is so named because ______________.
19. The complimentary symmetry circuit with single d.c. bias supply circuit is also called ______________.
20. Phase Inverter circuits are also called ______________.

21. What is the mode of operation of a last stage in a cascade ?
22. Derive an expression for second harmonic distortion interms of I_{max}, I_{min}, I_e.
23. What is the expression for total harmonic distortion interms of second, third harmomic ______________.
24. What is impedance matching ?
25. Why do we go for transformer coupled power amplifier ?
26. What is the equivalent load resistance of a transformer coupled amplifier interms of turms ratio ?
27. Is the equivalent load resistance increasing or decreasing if n greaterthan 1 ?
28. What is conversion efficiency ?
29. What is the maximum value of efficiency for the series fed load ?
30. What is the maximum value of efficiency for a transformer coupled load ?
31. How will the input signals be in a push pull amplifier ?
32. What are the advantages of a push pull configuration ?
33. Draw the waveforms to explain the class B operation.
34. What is the maximum efficiency of a class B amplifier ?

Essay Type Questions

1. What are the different methods of clarifying electronic amplifiers ? How arethey classified, based on the type of coupling ? Explain.

2. Compare the characteristic features of Direct coupled, resistive capacitor coupled, and Transformer coupled amplifiers.

3. Distinguish between small signal and large signal amplifiers. How are the power amplifiers classified ? Describe their characteristics.

4. Derive the general expression for the ouput power in the case of a class A power amplifier. Draw the circuit and explain the movement of operating point on the load line for a given input signal.

5. Derive the expressions for maximum. Theoretical efficiency·for maximum.
   (i) Transformer coupled
   (ii) Serves fed amplifier what are thier advantages and disadvantages.

6. Show that in the case of a class A transforms coupled amplifier, with inpedence matching, the expression for voltage gain AV is given as

$$A_V = -\left(\frac{h_{fe}}{2}\right) \cdot \frac{R_L}{h_{ie}} \cdot \frac{N_1}{N_2} \text{ with usual notation}$$

7. What are the advantages and disadvantages of transformer coupling ?

8. Show that class B push pull amplifiers exhibit halfwave symmetry.

9. Derive the expression for Max. Theoretical efficiency in the case of class B push pull amplifier. Why is it named so ? What are its advantages and disadvantages ?

10. Draw the circuit for composite tune amplifiers and explain its operation.

11. What are phase inverter circuits ? Draw a typical circuit and explain its working.

12. Draw the pentode pushpull amplifier and explain its operation.

13. Explain about Class D and Class S power amplifiers. Mention their salient features and applications.

14. How are the tuned amplifiers classified ? Explain the salient features of each one of them.

15. Draw the circuit for single tuned capacitance coupled amplifier explain its operation.

Answers of Objective Type Questions

1. (a) Frequency range (b) Type of coupling
   (c) Output - power/conduction angle (d) Magnitude of signal.
2. Small signal amplifier
3. (a) Direct coupling (b) R - C coupling
   (c) Transformer coupling (d) L - C tuned coupling (e) series fed
4. Large signal amplifier
5. (a) Class A 360° (b) Class B 180°
   (c) Class AB 180 to 360° (d) Class C $< 180^\circ$
6. The centre of linear region of the
7. Near cut off of the active device.
8. Beyond cut off
9. 25 %
10. 50 %
11. Audio frequency range 20 Hzs to 20 KHzs.
12. 78.5 %
13. $i\,(wt) = -\,i\,(wt + \pi)$
14. Even Harmonics
15. P_C (Max) = 0.4 P_O (Max)
16. Cut in voltage or threshold voltage.
17. Complimentary symmetry circuit.
18. Both PNP and NPN transistors are used.
19. Totempole circuit
20. Paraphase amplifiers.
21. Since for the last stage, the input signal has a high amplitude, the mode of operation will be other than class A.
22. Refer to the derivation.

23. $T_D = \sqrt{D_2^2 + D_3^2 + D_4^2 + ...}$

24. For maximum power transfer to the load, the load impedance should be conjugate of the effective impedance.

25. For impedance matching and hence higher efficiency.

26. $R_L' = \frac{1}{n^2} R_L$ where n is the turns ratio.

27. R_L' decreases

28. $\eta = \frac{\text{Signal power delivered to the load}}{\text{dc power absorbed.}}$

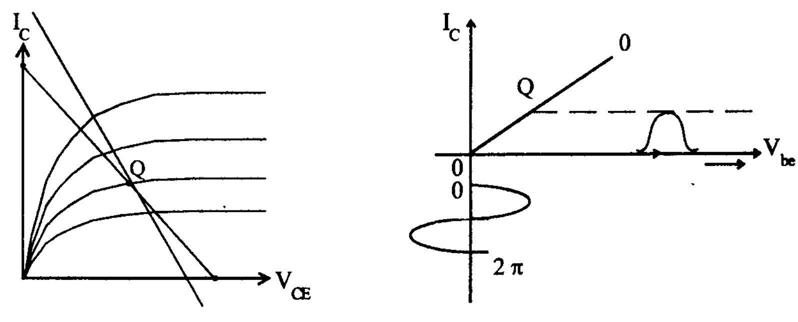
29. $\eta = 25\%$

30. $\eta = 50\%$

31. The input signals are both 180° out of phase.

32. Less harmonic distortion, More efficiency, Ripples in power supply are reduced, Magnetic effects are reduced.

33.



34. 78.5%

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UNIT - 5

Tuned Amplifiers - I

In this Unit,

- Different types of Tuned amplifier circuits are analyzed.
- Equivalent circuits of the output stages are given.
- FET Tuned R.F. amplifier circuits, wideband amplifier circuits, shunt compensation aspects are also explained.

5.1 Introduction

A tuned amplifier is one, which uses a parallel tuned circuit, as its load impedance. A parallel tuned *circuit, is also known as anti resonant circuit.* The characteristics of such an anti resonant circuit is that its |Z| is high, at the resonant frequency, and falls off sharply as the frequency departs from the resonant frequency. So the gain versus frequency characteristics of a tuned amplifier will also be similar to the |Z| characteristics of the resonant circuit. When |Z| is maximum, V_0 will also be maximum. This is for AC. |Z| is considered.

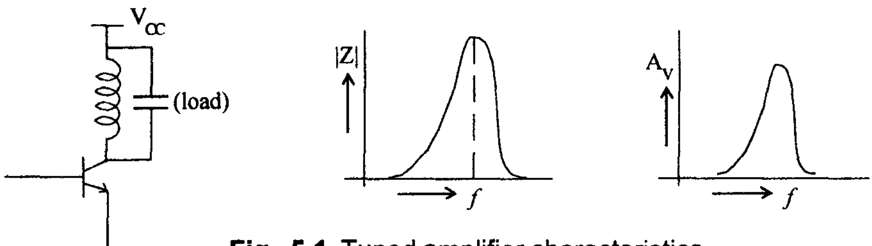


Fig. 5.1 Tuned amplifier characteristics

5.1.1 Applications

Tuned amplifiers are used to amplify a single radio frequency or narrow band of frequencies.

So basically they are used in 1. RF amplifiers 2. Communication receivers

Tuned amplifiers use variable Inductance (L) or variable Capacitance (C) to vary the resonant frequency.

In tuned amplifiers, *harmonic distortion is very small,* because the gain of the amplifiers is negligibly small for frequencies other than f_0 (the resonant frequency). So *Harmonics which are of higher frequencies will have very low gain* and hence harmonic distortion *will be less for tuned amplifiers.*

5.1.2 Classification

Tuned Amplifiers

Small Signal

* To amplify low RF signals
* Power output is low
* Operated in class A

Single tuned | Double tuned | Staggered tuned

Large Signal

* To amplify large RF signals
* Power output is more
* Operated in class B, class C or class AB modes.
* Pushpull configuration used to further reduce harmonic distortion.

This classification is similar to the classification of power amplifiers.

Small Signal Tuned Amplifiers

Single Tuned Amplifiers | Double Tuned Amplifiers | Staggered Tuned Amplifiers

5.1.3 Single Tuned Amplifier

Uses one parallel tuned circuit as the load |Z| in each stage and all these tuned circuits in different stages are tuned to the same frequency. To get large A_V or A_P, multistage amplifiers are used. But each stage is tuned to the same frequency, one tuned circuit in one stage.

5.1.4 Double Tuned Amplifier

It uses two inductively coupled tuned circuits, for each stage of the amplifier. Both the tuned circuits are tuned to the same frequency, two tuned circuits in one stage, to get sharp response.

5.1.5 Stagger Tuned Amplifier

This circuit uses number of single tuned stages in cascade. The successive tuned circuits are tuned to slightly different frequencies.

Single tuned amplifiers are further classified as :

Capacitive coupled | Transformer coupled or inductive coupled

5.2 Single Tuned Capacitive Coupled Amplifier

L, C tuned circuit is not connected between collector and ground because, the transistor will be short circuited at some frequency other than resonant frequency.

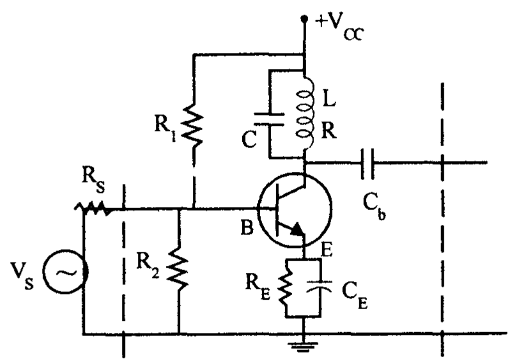


Fig. 5.2 Single tuned capacitive coupled amplifier

The output of the tuned circuit is coupled to the next stage or output device, through capacitor C_b. So this circuit is called single tuned capacitive coupled amplifier.

R_1, R_2, R_E, C_E are biasing resistors and capacitors. The tuned circuit formed by Inductance (L) and capacitor (C) resonates at the frequency of operation.

Transistor hybrid π equivalent circuit must be used since the transistor is operated at high frequencies. Tuned circuits are high frequency circuits.

R_i = input resistance of the next stage.

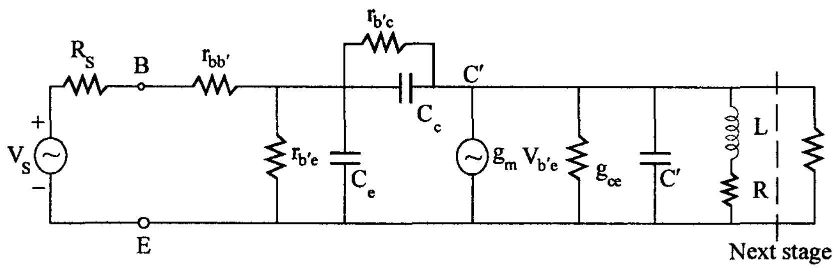


Fig. 5.3 Equivalent circuit

Modified equivalent circuit using Miller's Theorem.

According to Miller's theorem, the feedback capacitance C_C is C_C (1 - A) on the input side and $C_C\left(\frac{A-1}{A}\right)$ on the output side. But where as resistance is $\frac{r_{b'c}}{(1-A)}$ on the input side $\frac{r_{b'c}}{\left(\frac{A-1}{A}\right)}$ on the output side.

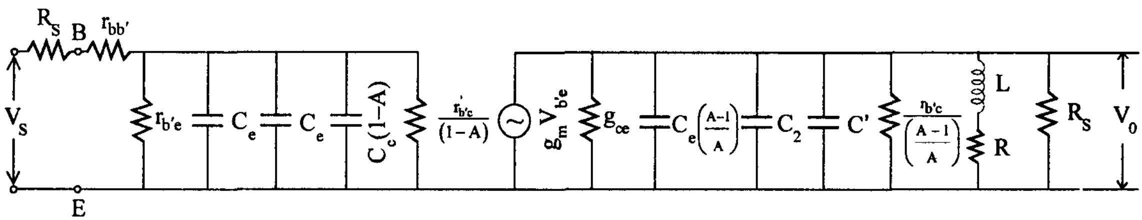


Fig. 5.4 Equivalent circuit (applying Miller's Theorem)

The equivalent circuit after simplification, neglecting $\frac{r_{b'c}}{\left(\frac{A-1}{A}\right)}$ is shown in Fig. 5.5.

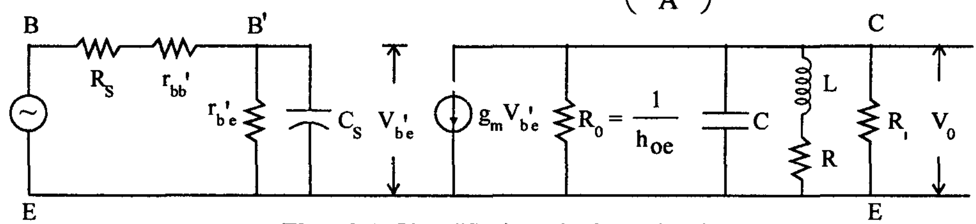


Fig. 5.5 Simplified equivalent circuit

$$Y_i = \frac{1}{R + j\omega L} = \frac{R - j\omega L}{R^2 + \omega^2 L^2} = \frac{R}{R^2 + \omega^2 L^2} - j\frac{\omega L}{R^2 + \omega^2 L^2}$$

Input admittance as seen by II stage.

Instead of L and R being in series, they are being represented as equivalent shunt element: R_P and L_P for parallel

$$= \frac{1}{R_P} + \frac{1}{j\omega L_P}$$

where $$R_P = \frac{R^2 + \omega^2 L^2}{R}$$

$$L_P = \frac{R^2 + \omega^2 L^2}{\omega^2 L}$$

Inductor is represented by R_P in series with inductance L_P.

Q at resonance, $$Q_0 = \frac{\omega_0 L}{R}$$

$\omega L >> R$ $\quad\because$ Resistance of the inductor R is small,

$\therefore$ $$R_P = \frac{\omega^2 L^2}{R} \quad \text{neglecting } R^2 \text{ compared to } \omega^2 L^2$$

$$L_P = L \quad \text{neglecting } R^2 \text{ compared to } \omega^2 L^2.$$

Therefore output circuit is simplified to,

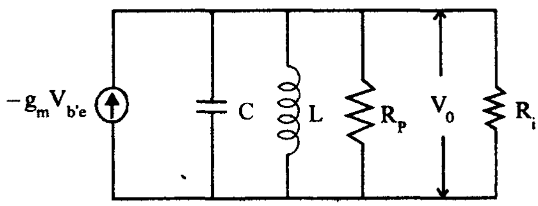


Fig. 5.6 Simplified circuit

$$\frac{1}{R_t} = \frac{1}{R} + \frac{1}{R_P} + \frac{1}{R_i}$$

$$\omega_0 = \frac{1}{\sqrt{LC}}$$

R_i is the input resistance of the next stage

Q_e is defined as, $$Q_e = \frac{\text{Suspectance of L or capacitance of C}}{\text{Conductance of shunt resistance } R_t}$$

R_t = resistance of tuned circuit

$$Q_e = \omega_0 CR_t$$

$$= \frac{R_t}{\omega_0 L} \frac{(1/\omega_0 L)}{1/R_t} = \left(\frac{\omega_0 C}{1/R_t}\right)$$

Let ω_0 be the resonant angular frequency in rad/sec.

$$\omega_0 = \frac{1}{\sqrt{LC}}$$

Output voltage $V_0 = -g_m V_{b'e}.Z$ ($-g_m V_{b'e}$ is the current source).
where Z is the impedance of C, L and R_t in parallel.

Admittance $$Y = \frac{1}{Z} = \frac{1}{R_t} + \frac{1}{j\omega L} + j\omega C$$

Multiplying by R_t throughout and dividing,

or $$Y = \frac{1}{R_t}\left[1 + \frac{R_t}{j\omega L} + j\omega C R_t\right]$$

$$= \frac{1}{R_t}\left[1 + j\frac{\omega_0 \omega C R_t}{\omega_0} + \frac{R_t \omega_0}{j\omega_0 \omega L}\right] \text{ (Multiplying and dividing by } \omega_0)$$

$$Y = \frac{1 + jQ_e\left[\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}\right]}{R_t} \qquad \left(\because \quad Q_e = \frac{R_t}{w_0 L} = \omega_0 C R_t\right)$$

where $Q_e = \omega_0 C R_t$

$$= \frac{R_t}{\omega_0 L} \qquad \because \quad \omega_0 L = \frac{1}{\omega_0 C}$$

$$\therefore \qquad Z = \frac{R_t}{1 + jQ_e\left[\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}\right]}$$

$$Q_e \text{ is defined as } = \frac{\text{Susceptance of L or C}}{\text{Conductance of shunt resistance } R_t}$$

Let δ = Fractional frequency variation
i.e., variation in frequency expressed as a fraction of the resonant frequency

$$\therefore \qquad \delta = \frac{\omega - \omega_0}{\omega_0} = \frac{\omega}{\omega_0} - 1$$

$$\therefore \qquad \frac{\omega}{\omega_0} = 1 + \delta$$

$\therefore$ Rewriting the expression for Z, as

$$Z = \frac{R_t}{1 + jQ_e\left[(1+\delta) - \frac{1}{(1+\delta)}\right]}$$

$$= \frac{X + \delta^2 + 2\delta - X}{1+\delta} = \frac{2\delta\left(1 + \frac{\delta}{2}\right)}{1+\delta}$$

$$Z = \frac{R_t}{1 + j2Q_e\,\delta\left[\frac{1+\delta/2}{1+\delta}\right]}$$

If the frequency ω is close to resonant frequency ω_0, $\delta << 1$.
Therefore Simplified expression for Z is

$$\boxed{Z = \frac{R_t}{1 + j2Q_e\,\delta}}$$

At resonance, $\omega = \omega_0, \quad \delta = 0$

At resonance, R_p may also be put as,

$$R_p = Q_0^2\,R = Q_0 = \sqrt{\frac{L}{C}} = \omega_0\,L\,Q_0$$

Expression for $V_{b'e} = V_i \cdot \frac{r_{b'e}}{r_{bb'} + r_{b'e}}$ potential divider network

Expression for $V_0 = -g_m V_{be} \cdot Z$

Expression for $V_0 = -g_m V_i \cdot \frac{r_{b'e}}{r_{b'e} + r_{b'e}}\ Z$

$\therefore$ Voltage gain $A = \frac{V_0}{V_i} = -g_m \cdot \frac{r_{b'e}}{r_{b'e} + r_{bb'}} \cdot Z$

$$A = -g_m \cdot \frac{r_{b'e}}{r_{b'e} + r_{bb'}} \cdot \frac{R_t}{1 + j2\delta Q_e}$$

voltage gain at resonance. Since at resonance $\delta = 0$

$$A_{reso} = \frac{-g_m \cdot r_{b'e}}{r_{b'e} + r_{bb'}} \cdot R_t$$

$$\therefore \quad \frac{A}{A_{reso}} = \frac{1}{1 + j2\delta Q_e}$$

Magnitude $$\left|\frac{A}{A_{reso}}\right| = \frac{1}{\sqrt{1+(2\delta Q_e)^2}}$$

Phase angle $$\left|\frac{A}{A_{reso}}\right| = -\tan^{-1}(2\,\delta\,Q_e)$$

At a frequency ω_1, below the resonant frequency δ has the value,

$$= -\frac{1}{2Q_e};$$

$$\frac{A}{A_{reso}} = \frac{1}{\sqrt{2}} = 0.707$$

ω_1 is the lower 3db frequency.

Similarly ω_2, the upper 3db frequency is

$$\delta = +\frac{1}{2Q_e};\ \frac{A}{A_{reso}} = \frac{1}{\sqrt{2}} = 0.707$$

The 3 db band width $\Delta\omega = (\omega_2 - \omega_1)$

$$= \frac{[(\omega_2-\omega_0)+(\omega_0-\omega_1)].\,\omega_0}{\omega_0}$$

$$= [\delta + \delta]\,\omega_0 \qquad = 2\,\delta\,\omega_0$$

But $$\delta = \frac{1}{2Q_e}$$

$$\therefore \qquad \Delta\,\omega = \frac{\omega_0}{Q_e} = \frac{\omega_0}{R_t\,\omega_0\,C} = \frac{1}{R_t\,C} \quad \text{rad/sec.}$$

5.3 Tapped Single Tuned Capacitance Coupled Amplifier

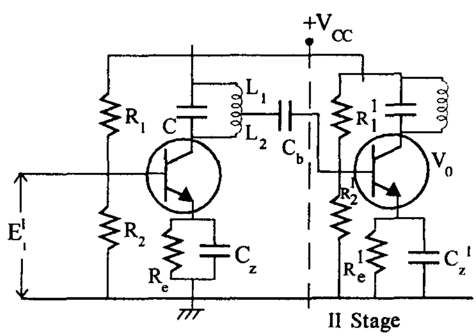


Fig. 5.7 Tapped single tuned capacitive coupled amplifier circuit

5.3.1 Equivalent Circuit on the Output Side of the I Stage

R_i is the input resistance of the II stage.

R_0 is the output resistance of the I stage amplifier.

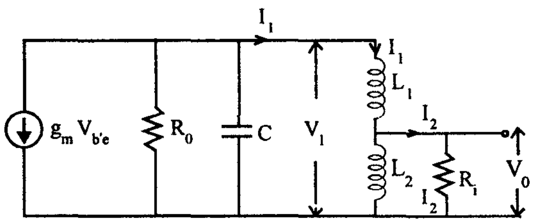


Fig. 5.8 Equivalent circuit

The input |Z| of the common emitter amplifier circuits will be less. So the output impedance of the circuit being coupled to one common emitter amplifier, should also have low |Z| for impedance matching and to get maximum power transfer. So in order to reduce the impedance of the LC resonant circuit, to match the low |Z| of the common emitter circuit, tapping is made in the LC tuned circuit. Tapped single tuned circuits are used in such applications.

5.3.2 Expression for 'Inductance' for Maximum Power Transfer

Let the tapping point divide the impedance into two parts L_1 and L_2.

Let $L_1 = nL$ so that $L_2 = (1 - n)$

Writing Kirchoff's Voltage Law (KVL)

$$V_1 = j\omega L \,.\, I_1 - j\omega\,(L_2 + M)\,I_2 \qquad .....(1)$$

$$0 = -j\omega\,(L_1 + M)\,I_1 + (R_i + j\omega L_2)\,I_2 \qquad .....(2)$$

Where M is the mutual inductance between L_1 and L_2. Solving equations 1 and 2,

$$I_1 = \frac{V_1\left(R_i + j\omega L_2\right)}{j\omega L\left(R_i + j\omega L_2\right) + \omega^2\left(L_2 + M\right)^2} \qquad .....(3)$$

Hence the |Z| offered by the coil along with input resistance R_i of the next stage is

$$Z_1 = \frac{V_1}{I_1} = \frac{j\omega L\left(R_i + j\omega L_2\right) + \omega^2\left(L_2 + M\right)^2}{\left(R_i + j\omega L_2\right)} \qquad .....(4)$$

$$= j\omega L + \frac{\omega^2\left(L_2 + M\right)^2}{R_i + j\omega L_2} \qquad .....(5)$$

But ωL_2 much less than R_i.

As R_i, the input resistance of transistor circuit II stage is $K\Omega$ and much greater than ωL_2

$$Z_1 = j\omega L + \frac{\omega^2\left(L_2 + M\right)^2}{R_i} \qquad .....(6)$$

$$M = K\sqrt{L_1 L_2} \qquad M = \text{Mutual Inductance}$$

Where K is the coefficient of coupling. Since $L_1 = nL$, $L_2 = (1-n)L$

$$= K\sqrt{nL(1-n)L} = KL\sqrt{(n-n^2)} \qquad .....(7)$$

Putting K = 1, we get

$$M \simeq L\sqrt{n-n^2} \qquad .....(8)$$

Substituting thus value of M in (6),

$$Z_1 \simeq j\omega L \pm \frac{\omega^2\left[(1-n)L + L\sqrt{n-n^2}\right]^2}{R_i} \qquad .....(9)$$

$$\simeq j\omega L + \frac{\omega^2 L^2\left[(1-n)+\sqrt{n-n^2}\right]^2}{R_i} \qquad .....(10)$$

$(j\omega L + R)$

The resistance effectively reflected in series with the coil due to the resistance R_i is given by,

$$R_{is} \simeq \frac{\omega^2 L^2\left[(1-n)+\sqrt{n-n^2}\right]^2}{R_i}$$

This is the resistance component; S : series, i : input

This resistance R_{is} in series with the coil L may be equated to a resistance R_{ip} in shunt with the coil where R_{ip} is given by,

$$R_{ip} = (\omega L)^2 / R_{is}$$

So the equivalent circuit is

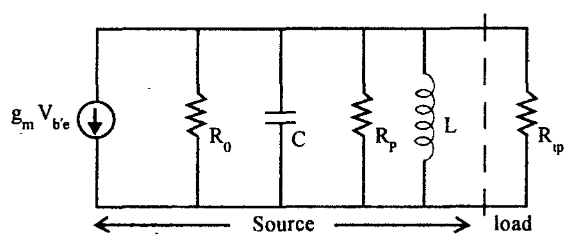


Fig. 5.9 Equivalent circuit

Simplifying,

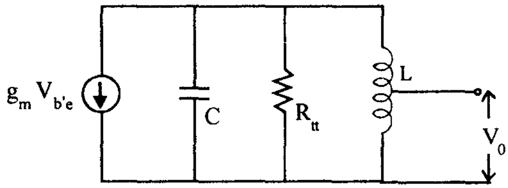


Fig. 5.10 Equivalent circuit after simplification

$$\frac{1}{R_{tt}} = \frac{1}{R_0} + \frac{1}{R_p} + \frac{1}{R_{ip}}$$

$$Q_e = \frac{R_{tt}}{\omega_0 L}$$

tt : tuned tapped circuit.

$$\omega_0 = \frac{1}{\sqrt{LC}}$$

Under the conditions of maximum power transfer theorem, the total resistance appearing in shunt with the coil is = R_{op}

Since it is a resonant circuit, at resonance, the |Z| in purely resistive. For maximum power transfer |Z| = R/2.

$$\therefore \qquad Q_e = \frac{R_{op}/2}{\omega_0 L}; \quad R_{tt} = R_{op}/2$$

$$R_{op} = 2\, Q_e .\, \omega_0\, L$$

But $$R_{op} = \frac{R_0 R_p}{R_0 + R_p}$$

$$\therefore \qquad 2\, Q_e\, \omega_0\, L = \frac{R_0\, \omega_0\, Q_0\, L}{R_0 + \omega_0\, Q_0\, L}$$

Solving for L, we get

$$L = \frac{R_0 (Q_0 - 2Q_e)}{2\omega_0 Q_0 Q_e}$$

Expression for L for maximum power transfer.

$$\boxed{L = \frac{R_0}{\omega_0}\left[\frac{1}{2Q_e} - \frac{1}{Q_0}\right]}$$

This is the value of L for maximum power transfer.

Expression for voltage gain and Bandwidth are determined in the same way as done for a single tuned circuit. In this circuit we have,

1. R_{tt} instead of R_t (as in single tuned) tapped tuned circuit.
2. Output voltage equals (1 – n) times the voltage developed across the complete coil.

$|Z|$ at any frequency close to w_0 is given by,

$$Z = \frac{R_{tt}}{1 + j\,2\delta\,Q_e} \qquad R_{tt} = \text{resistance of Tapped Tuned Circuit}$$

output voltage $$V_0 = \frac{-g_m V_i\, r_{b'e}}{r_{b'e} + r_{bb'}} \,.\, Z\,(1-n)$$

$\therefore$ voltage gain $$A = \frac{V_0}{V_i} = -g_m\,(1-n)\,\frac{r_{b'e}}{r_{b'e} + r_{bb'}} \,.\, Z$$

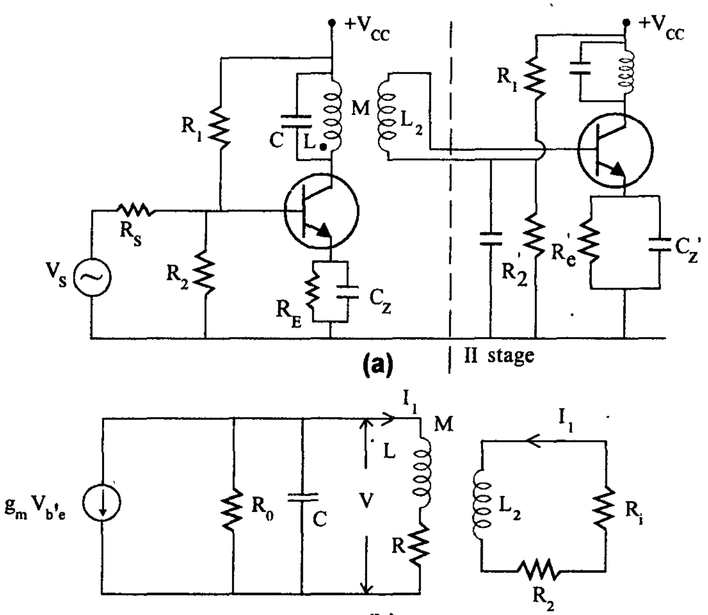
$$= -g_m\,(1-n).\frac{r_{b'e}}{r_{b'e} + r_{bb'}} \,.\, \frac{R_{tt}}{1 + j\,2\delta Q_e}$$

At resonance, voltage gain is

$$A_{reso} = -\,g_m\,(1-n)\,.\,\frac{r_{b'e}}{r_{b'e} + r_{bb'}} \,.\, R_{tt}$$

$$\therefore \quad \boxed{\frac{A}{A_{reso}} = \frac{1}{1 - j\,2\delta Q_e}}$$

5.4 Single Tuned Transformer Coupled or Inductively Coupled Amplifier



(b) Equivalent output circuit

Fig. 5.11 Inductive coupled amplifier circuit (a) and its equivalent (b)

In this circuit, the voltage developed across the tuned circuit is inductively coupled to the next stage. Coil L, of the tuned circuit, and the inductor coupling the voltage to the II stage, L_2 form a transformer with mutual coupling M. This type of circuit is also used, where the input |Z| of the II stage is smaller or different from the tuned circuit. So |Z| matching is done by the transformer depending on its turn ratio. In such requirements, this type of circuit is used.

The resistors R_1, R_2 and R_1' and R_2' are the biasing resistors. The parallel tuned circuit, L and C resonates at the frequency of operation. Fig. (b) shows output equivalent circuit. Input equivalent circuit will be the same as that of the capacitive coupled circuit.

In the output equivalent circuit, C is the total capacitance, including the stray capacitance, Miller equivalent capacitance $C\left(\frac{A-1}{A}\right)$. L_2 and R_2 are the inductance and resistance of the secondary winding.

5.4.1 Expression for L_2 for Maximum Power Transformer

Writing KVL to the primary and secondary windings,

$$V = I_1 Z_{11} + I_2 Z_{12} \qquad .....(1)$$

$$0 = I_1 Z_{21} + I_2 Z_{22} \qquad .....(2)$$

where

$$Z_{11} = R + j\omega L \qquad .....(3)$$

$$Z_{12} = Z_{21} = j\omega M \qquad .....(4)$$

$$Z_{22} = R_2 + R_i + j\omega L_2 \qquad .....(5)$$

Solving eqs. (1) and (2) for I_1,

$$I_1 = \frac{V.Z_{22}}{Z_{11} Z_{22} - Z_{12}^2} \qquad .....(6)$$

The impedance seen looking into the primary is,

$$Z_{in} = \frac{V}{I_1} \; \frac{Z_{11} Z_{22} - Z_{12}^2}{Z_{22}}$$

$$= Z_{11} - \frac{Z_{12}^2}{Z_{22}} \qquad .....(7)$$

Substituting the values of Z_{11}, Z_{22} and Z_{12} in equation (7) we get,

$$Z_{in} = (R + j\omega L) + \frac{\omega^2 M^2}{R_2 + R_i + j\omega L_2} \qquad .....(8)$$

R_i generally much greater than R_2 and ωL_2.

$$\therefore \qquad Z_{in} \simeq (R + j\omega L) + \frac{\omega^2 M^2}{R_i} \qquad .....(9)$$

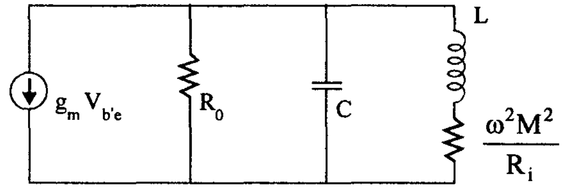


Fig. 5.12 Equivalent circuit

$\frac{\omega^2 M^2}{R_i}$ is the impedance of the secondary side reflected to the primary.

If M is reasonably large, then $R << \frac{\omega^2 M^2}{R_i}$

$$\therefore \qquad Z_{in} \simeq j\omega L + \frac{\omega^2 M^2}{R_i} \qquad \text{......(10)}$$

$\therefore$ The equivalent circuit may be written as,

Inductance L with series resistance $\frac{\omega^2 M^2}{R_i}$ may be represented as L in shunt with R_{in} as shown below, where

$$R_{ip} = \frac{(\omega L)^2}{\left(\frac{\omega^2 M^2}{R_i}\right)} = \left(\frac{L}{M}\right)^2 . R_i \qquad \text{.....(11)}$$

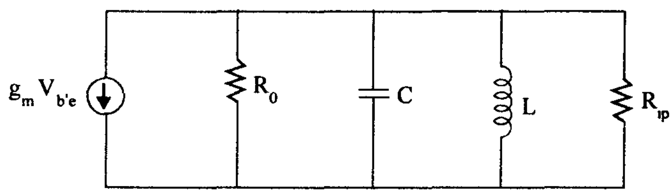


Fig. 5.13 Simplified circuit

For maximum transfer of power at resonance,

$$R_{ip} = R_0$$

$$\therefore \qquad R_0 = \left(\frac{L}{M}\right)^2 . R_i \qquad \text{.....(12)}$$

Equation 12. gives the value of M for maximum power transfer.

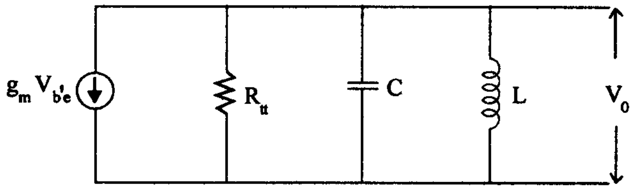


Fig. 5.14 Equivalent circuit

L and L_2 are the primary and secondary windings of inductances.

$\therefore$ $$M = K\sqrt{LL_2} \qquad .....(13)$$

Combining eqs. (12) and (13) we get

$$R_0 = \left(\frac{L}{K^2 L_2}\right) R_i \qquad .....(14)$$

Therefore from equation 14, for a given value of R_0 and coefficient of coupling K and R_i, we can determine L_2 for maximum transformer of power.

Shunt resistance R_0 and R_{ip} may be combined to yield the total shunt resistance R_{tt}.

$$\frac{1}{R_{tt}} = \frac{1}{R_0} + \frac{1}{R_{ip}}$$

R_{tt} = Resistance of tapped tuned circuit .....(15)

Effective Q of the entire circuit is,

$$Q_e = \frac{R_{tt}}{\omega_0 L} \qquad .....(16)$$

where w_0 is the resonant frequency of L and C.

$$\omega_0 = \frac{1}{\sqrt{LC}} \qquad .....(17)$$

Under conditions of maximum transfer of power, total resistance appearing in shunt with the coil equals $R_0/2$. Since it is resonant circuit, at resonance, |Z| = resistance only. For maximum power, R = R/2.

$\therefore$ equation 16 becomes

$$Q_e = \frac{R_0/2}{\omega_0 L} \qquad .....(18)$$

or $$R_0 = 2\, Q_e\, \omega_0\, L \qquad .....(19)$$

Solving equations 1 and 2

$$I_2 = \frac{V.Z_{21}}{Z_{21}.Z_{12} - Z_{11}\,Z_{22}} \qquad .....(20)$$

$$\therefore \quad V_0 = -I_2 \,.\, R_i \qquad .....(21)$$

$$= V \,.\, \frac{R_i.Z_{21}}{Z_{11}.Z_{22} - Z_{12}^2} \qquad .....(22)$$

$|Z|$ of the output circuit at any frequency 'ω' close to ω_0, is given by,

$$\text{Impedance of output circuit } Z = \frac{R_{tt}}{1 + j2\delta Q_e} \qquad .....(23)$$

$$\therefore \quad V_0 = -g_m \,.\, \frac{V_0\, r_{b'e}}{r_{b'e} + r_{bb'}} \,.\, Z \,.\, \frac{R_i\, Z_{21}}{Z_{11}\, Z_{22} - Z_{12}^2} \qquad .....(24)$$

$$= -g_m\, V_i \,.\, \frac{r_{b'e}}{r_{b'e} + r_{bb'}} \,.\, \frac{R_i.Z_{21}}{Z_{11} Z_{22} - Z_{12}^2} \,.\, \frac{R_{tt}}{1 + j2\delta Q_e} \qquad .....(25)$$

$\therefore$ Voltage gain A at any frequency ω is,

$$A = \frac{V_0}{V_i} = -g_m \frac{r_{b'e}}{r_{b'e} + r_{bb'}} \,.\, \frac{R_i\, Z_{21}}{Z_{11}\, Z_{22} - Z_{12}^2} \,.\, \frac{R_{tt}}{1 + j2\delta Q_e} \qquad .....(26)$$

Voltage at resonance,

$$A_{reso} = -g_m \,.\, \frac{r_{b'e}}{r_{b'e} + r_{bb'}} \,.\, \frac{R_i\, Z_{22}}{Z_{11}\, Z_{22} - Z_{12}^2}$$

$$\therefore \quad \boxed{\frac{A}{A_{reso}} = \frac{1}{1 + j2\delta Q_e}} \qquad .....(27)$$

5.5 CE Double Tuned Amplifier

In this circuit, voltage developed across the tuned circuit in the collector circuit is inductively coupled to another tuned circuit. Both circuits are tuned to the same frequency, the desired frequency of the input signal.

5.5.1 Advantages

1. It provides larger 3-db band width than the single tuned amplifier. Therefore Gain × Bandwidth product is more. (eventhough gain is same, Bandwidth is more. So gain × Bandwidth product is more).
2. It provides gain - frequency curve having steeper sides and flatter top.

In double tuned amplifier, as Bandwidth is increased the overshoot of gain also increases. So a compromise must be made. The value of the coefficient 'b' ranges from 1.0 to 1.7.

5.5.2 Circuit

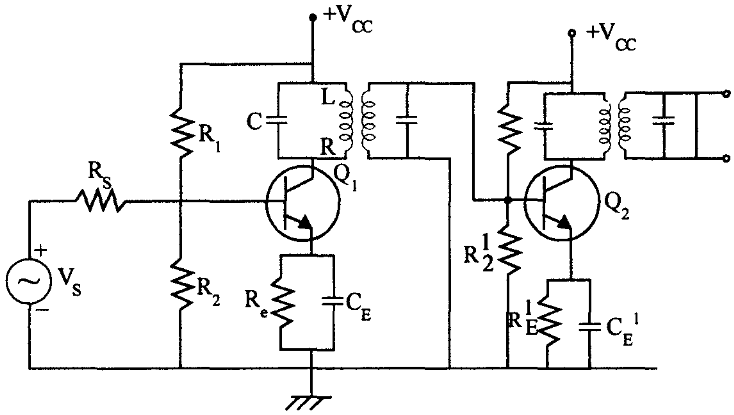


Fig. 5.15 Double tuned amplifier circuit

5.5.3 Equivalent Circuit

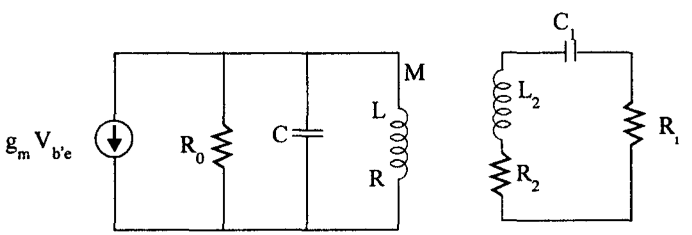


Fig. 5.16 Equivalent circuit

Voltage developed across the tuned circuit in the LCR combination is inductively coupled to another tuned circuit of the same resonant frequency.

R is the resistance associated with L. R_i is the output |Z| of the second circuit. The equivalent circuit can be further simplified as, R_i and R_2 are combined to form R_i'. R_0 in parallel with L-R may be brought in series with inductance and combined with R to from R_i.

The current source $g_m V_{b'e}$ in shunt with 'C' is modified to a voltage source V_1 in series with 'C'.

∴ The modified circuit is as shown in Fig. 5.17.

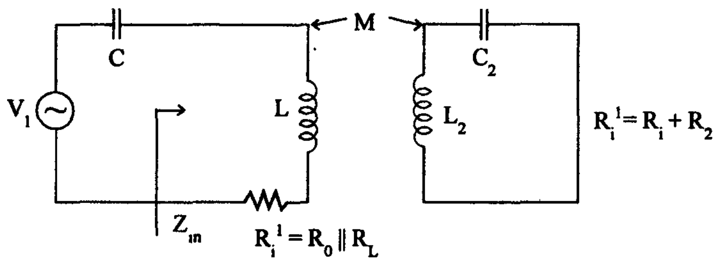


Fig. 5.17 Modified circuit

$$Z_{in} = \frac{\omega^2 M^2}{R_{ik} + \left(\omega L_2 - \frac{1}{\omega L_2}\right)} \quad .....(1)$$

At resonance, $$\omega_0 L = \frac{1}{\omega_0 C} \quad .....(2)$$

and $$\omega_0 L_2 = \frac{1}{\omega_0 C_2} \quad .....(3)$$

$\therefore$ At resonance, Z_i is reduced to

$$Z_{in} = \frac{\omega_0^2 M^2}{R_i^1} \quad .....(4)$$

Hence at resonance for maximum transfer of power R_0 must equal Z_{in}. i.e., M is adjusted to critical value M_C, such that

$$R_0 = \frac{\omega_0^2 M_C^2}{R_i} \quad ......(5)$$

or $$\sqrt{R_0' R_i'} = \omega_0 M_0 \quad .....(6)$$

$$= \omega_0 K_C \sqrt{L L_2} \quad .....(7)$$

where K_C *is the critical value of the coefficient of coupling corresponding to the critical value* M_C *of mutual inductance.*

From 7, $$K_C = \frac{\sqrt{R_0' R_i'}}{\omega_0 \sqrt{L L_2}} \quad .....(8)$$

$$= \left(\frac{R_0'}{\omega_0 L}\right)^{1/2} \cdot \left(\frac{R_i'}{\omega_0 L_2}\right)^{1/2} = \frac{1}{\sqrt{Q_1 Q_2}} \quad ......(9)$$

In a general case, $K \neq K_C$

So let $K = b.\, K_C$

Now, $V_1 = Z_{11}\, I_1 + Z_{12}.I_2$ .....(10)

$$0 = Z_{21}\, I_1 + Z_{22}\, I_2 \quad .....(11)$$

Solving equation 10 and 11, for I_2, we get

$$I_2 = \frac{V_1 Z_{21}}{Z_{11} Z_{22} - Z_{12}^2} \quad .....(12)$$

where $Z_{11} = R_0' + j\,(\omega L - \frac{1}{\omega C})$ ......(13)

$$Z_{22} = R_i' + j\left(\omega L_2 - \frac{1}{\omega C_2}\right) \quad .....(14)$$

and $Z_{12} = Z_{21} = j\omega_0\, M$ .....(15)

At resonance, $Z_{11} = R_0'$ and $Z_{22} = R_i'$

For maximum transfer of power at resonance,

$$Z_{11} = R_0', \; Z_{22} = R_i',$$

$$Z_{12} = j\omega_0\, M_C \quad .....(16)$$

Substituting these values of Z_{11}, Z_{22}, and Z_{12} in equation 12, we get the following conditions for maximum transfer of power at resonance.

$$I_{2\,Max} = \frac{-j\, V_1\, \omega_0 M_C}{R_0^1\, R_i^1 + \omega_r^2\, M_C^2} \quad .....(17)$$

M_c is the critical value of Mutual Inductance.

Substituting the value of M_C in equation 17, we get

$$I_{2\,Max} = \frac{-j\, V_1 \sqrt{R_0'\; R_i'}}{R_0^1\, R_i^1 + R_0' R_i'}$$

$$= \frac{-jV_1}{2\sqrt{R_0'\, R_i}} \quad .....(18)$$

Magnitude $$|I_{2\,Max}| = \frac{V_1}{2\sqrt{R_0' R_i'}}$$

$$\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega} \pm \sqrt{\left(b^2 - 1 \pm 2b\right)/Q}$$

where
b = (K/K_C)
K = Coefficient of coupling
K_C = Critical value of coefficient of coupling corresponding to the critical value of Mutual Inductance Mc.

Tuned amplifiers are used where it is desired to amplify a relatively narrow band of frequencies, centered about some designated mean carrier frequency.

5.6 Applications of Tuned Amplifiers

1. Radar
2. Television
3. Communication receivers
4. I.F amplifiers

There are mainly three types tuned voltage amplifiers.

1. Single tuned amplifier
2. Double tuned amplifier
3. Stagger tuned amplifier

Objective Type Questions

1. Radio Frequency Range is ____________________.
2. VHF Frequency Range is ____________________.
3. Parallel Tuned Circuit is also known as ____________________.
4. Generally Tuned Amplifiers are used in ____________________.
5. In Tuned Amplifiers, Harmonic Distortion is ____________________.
6. Small signal Tuned Amplifiers are operated in ____________________ mode.
7. Large signal Tuned Amplifiers are operated in ____________________ modes.
8. Small signal Tuned Amplifiers are classified as

   (a) ____________________ (b) ____________________ (c) ____________________
9. Single Tuned Amplifiers are classified as ____________________.
10. In Tuned Amplifiers equivalent circuits, the model used for Transistors (BJT) is ____________________.
11. Expression for $\frac{A}{A_{reso}}$ for tapped single tuned capacitance coupled amplifier with usual notation is ____________________.
12. Double Tuned Amplifier provides ____________________ Bandwidth than single tuned amplifier.
13. Common Emitter (C.E) Double Tuned amplifier provides Gain - Frequency curve with ____________________ sides ____________________ top.
14. In Radars and Television ____________________ type of amplifiers are used.

Essay Type Questions

1. (a) What are the different types of Tuned Amplifiers ?
   (b) How are Tuned amplifiers classified ?
   (c) What are the applications of Tuned amplifiers ?
2. Draw the circuit for single tuned capacitive coupled amplifier and explain its working. Draw its equivalent circuit and derive the expression for (A/A_{reso})
3. Draw the circuit for tapped single tuned capacitance coupled amplifier and explain its working. Draw the frequency response. Derive the expression for L for maximum power transfer.
4. Draw the circuit for single tuned inductively coupled amplifier. Draw its equivalent circuit and derive the expression for $\left(\dfrac{A}{A_{reso}}\right)$.
5. Draw the circuit for Double Tuned Amplifier. Explain its working. What are the advantages of this amplifier ? Derive the expression for I_2 Max.

Answers to Objective Type Questions

1. > 20 KHzs
2. 30 MHzs - 300 MHzs
3. Anti Resonant Circuit
4. R. F amplifiers, communication Receivers
5. Less
6. Class A
7. Class B, class C or class AB
8. (a) Single Tunded (b) Double Tuned (c) Staggered Tuned
9. (a) Capacitive coupled (b) Transformer coupled or Inductive coupled
10. Hybrid - π equivalent circuit
11. $\dfrac{A}{A_{reso}} = \dfrac{1}{1 + j2\delta Q_e}$ where $\delta = \left(\dfrac{\omega - \omega_0}{\omega_0}\right)$ $Q_e = \omega_o C R_t = \dfrac{R_t}{\omega_0 L}$.
12. Larger
13. Steaper sides and flatter top
14. Tuned amplifiers

UNIT - 6

Tuned Amplifiers - II

In this Unit,

- Single stage amplifiers in the three configurations of C.E, C.B, C.C, with design aspects are given.
- Using the design formulae for A_V, A_I, R_i, R_o etc, the design of single stage amplifier circuits is to be studied.
- Single stage JFET amplifiers in C.D, C.S and C.G configurations are also given.
- The Hybrid - π equivalent circuit of BJT, expressions for Transistor conductances and capacitances are derived.
- Miller's theorem, definitions for f_β and f_T are also given.
- Numerical examples, with design emphasis are given.

6.1 Stagger Tuning

Tuned amplifiers have large gain, since at resonance, Z is maximum. So A_V is maximum. To get this large A_V over a wide range of frequencies, stagger tuned amplifiers are employed. This is done by taking two single tuned circuits of a certain Bandwidth, and displacing or staggering their resonance peaks by an amount equal to their Bandwidth. The resultant staggered pair will have a Bandwidth, $\sqrt{2}$ times as great as that of each of individual pairs.

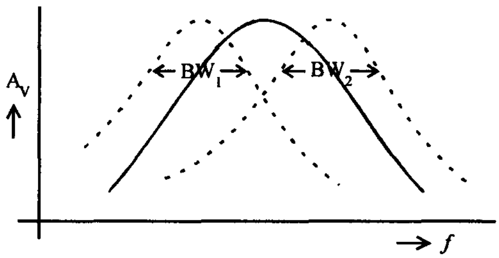


Fig. 6.1 Variation of A_V with f

6.2 Single Tuned Transistor Amplifier

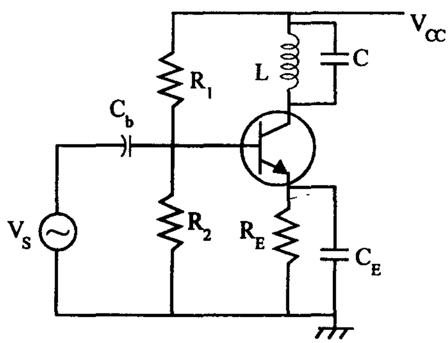


Fig. 6.2 Single tuned amplifier

6.3 Stability Considerations

An electronic amplifier circuit or oscillator circuit becomes unstable, i.e., will not perform the desired function, due to various reasons associated with circuit design aspects like Thermal stability, Bias considerations, output circuit, feedback, circuit etc. Let us consider these aspects.

Thermal Effects : Any electronic circuit, when used continously, various components will get heated, due to power dissipation in each of the components. When the active device in the circuit (BJT) also gets heated, due to the dependance of its characteristics on temperature, the operating point changes. So the device will not function as desired and the output from the electronic circuit will not be obtained as per specifications. Heat sinks are to be used, to dissipate the excess thermal energy and to keep the operating temperature of the active device within the limits. Heat sinks are good themal conductors designed suitably, to keep the temperature of the device within limits.

Let

P_J = Power dissipated in watts at the junction of the device

T_A = Ambient Temperature

T_J = Temperature of the junction

θ_T = Themel resistance in °C/W

$T_J = T_A + \theta_T \cdot P_J$

Range of value of θ_J is 0.2 to 2.0 °C/W.

A thin mica spacer is often used to electrically insulate the BJT or semiconductor device from the heat sink. The thermal path for heat dissipation is from semiconductor p-n junction to casing of the device, from the case to heat sink and from heat sink to the ambient.

θ_C = Thermal resistance in °C/W associated with the Casing of the device

θ_H = Thermal resistance in °C/W associated with the Heat sink.

θ_R = Radiation Thermal Resistance

So,

$$T_H = T_J - P_J(\theta_J + \theta_C)$$

$$\text{Total Heat sink resistance} = \theta_H + \frac{\theta_C\,\theta_R}{\theta_C + \theta_R}$$

If P_J, the power dissipated at the junction is independent of T_J then,

$$\frac{dP_J}{dT_J} = \frac{1}{\theta_T}$$

At the operating temperature, $\dfrac{dP_J}{dT_J} > \dfrac{1}{\theta_T}$

Bias Considerations : Distortion in Audio amplifiers and other types of circuits depends on :

(i) Input signal level (in mv)

(ii) Source Resistance

(iii) Bias Conditions

(iv) Type of output load and its impedance

(v) Loading effect.

For audio frequency amplifiers, distortion of 1 or 2% is considered maximum for higher fiedility equipment.

A maximum of 5% distorion is set sometimes for radio receivers and public address systems.

Consider the circuit shown in Fig. 6.3.

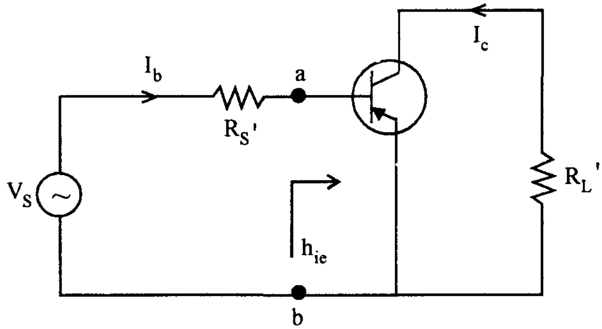


Fig. 6.3

Expression for input power P_S is,

$$P_S = Ib^2 \left(R_S' + h_{ie}\right)$$

Expression for output power P_o is,

$$P_O = I_C^2.R_L'$$

$\therefore$ Power Gain
$$A_P = \frac{P_o}{P_s} = \frac{I_C^2 R_L'}{I_b^2\left(R_S' + h_{ie}\right)}$$

$$= \frac{h_{fe}^2 R_L'}{R_S' + h_{ie}}$$

Considering only the BJT, expression for power gain

$$A_{p(BJT)} = \frac{h_{fe}^2 R_L}{h_{ie}} = h_{fe}.\, g_m\, R_L'$$

Maximum power is transferred to the base-emitter circuit of BJT, when impedance matching is done as,

$$R_S' = h_{ie}$$

$\therefore$ Matched input Power Gain

$$A_P \text{ (Matched input)} = \frac{h_{fe}^2 R_L'}{2h_{ie}}$$

$$A_p = h_{fe} \,.\, \frac{g_m.R_L'}{2}$$

To maintain output voltage and power levels stable, the circuit must be designed accordingly.

6.4 Tuned Class B and Class C Amplifiers

The efficiency of the output circuit of an amplifier increases as the operation is shifted from class A to B and then to C.

In class C amplifiers, efficiency approaches 100%.

But the difficulty with class 'C' operations is harmonic distortion is more. So the conventional untuned amplifiers use class B pushpull configuration. But, if it is a tuned amplifier, and only one frequency f_0, is to be amplified and power to be handled P_0 is large, then class C operation is preferable, since efficiency is high and harmonic distortion will not be a problem since, only one frequency is to be amplified and the tuned circuit will reject the other frequencies.

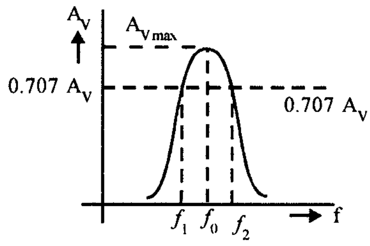


Fig. 6.4 Frequency response

In radio transmitters, the output power often exceeds 50 KW and efficiency is the important criteria. Hence usually class C operation is done. The operation of such amplifier circuits is non linear, since the variation of output current i_L with the input current i_b is non linear, as the signal magnitudes are large. So these amplifiers are also called as *Large signal amplifiers*.

Since they have a tuned circuit and usually operate in the R.F range, they are also called as *R.F power amplifiers*.

Usually these circuits use common emitter configuration, but sometimes common base configuration is also used. A simplified circuit (without emitter stabilization) uses transformer and FET as shown below. Since the circuit is class B and class C configurations, the input signal itself drives the transistor or FET into conduction. So there are no separate biasing resistors.

The circuit may be class B or class C, depending upon the actual conduction angle (180^0 or less).

6.4.1 Bipolar Junction Transistor (BJT) Tuned Class B/C amplifier

The capacitors C_S, C_b and C_C are considered to be short circuits at the operating signal frequencies.

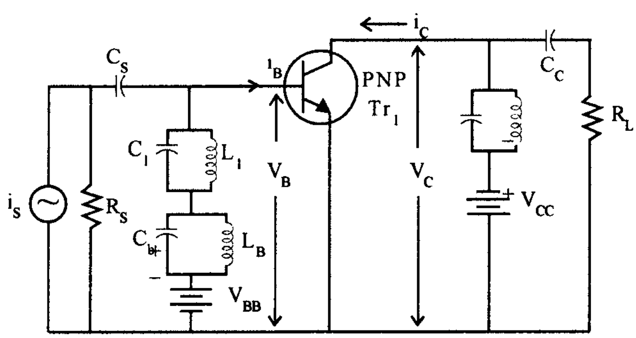


Fig. 6.5 Tuned class B/C amplifier

The transformer circuit L_1, C_1 and R_b, C_b provide high input impedance |Z| to the input signal and so i_b passes to the base of the transformer only and will not get divided across L_1 C_1 or R_b C_b. So the power output will be more.

6.4.2 FET Tuned R.F Amplifier

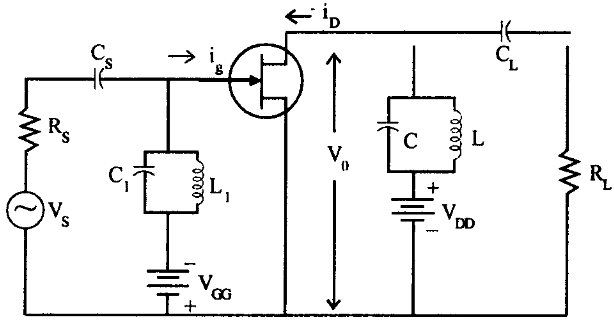


Fig. 6.6 FET tuned RF amplifier

6.4.3 Waveforms

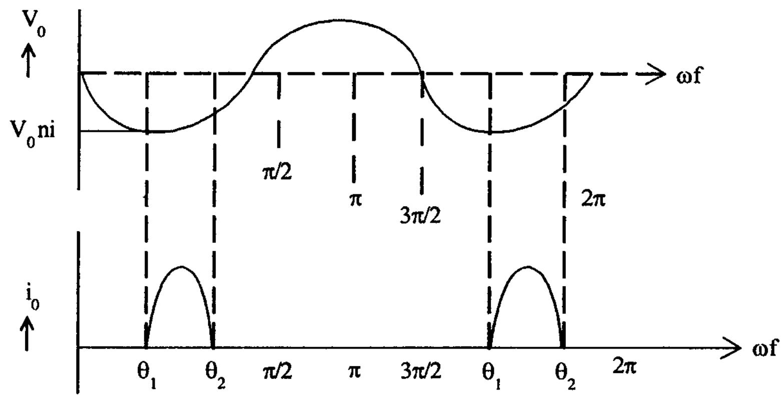


Fig. 6.7 Frequency response

6.4.4 Resonant circuit

In a tuned amplifier, the functions of the resonant circuit are :

1. To provide correct load impedance to the amplifier.
2. To reject unwanted harmonics
3. To couple the power to the load

The resonant circuits in tuned power amplifiers are sometimes called tank circuits, because the L and C elements store energy like water stored in a tank. Such a circuit is as shown in Fig. 6.8.

Its equivalent is (R + jωL) in parallel with R_L.

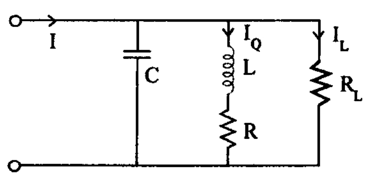


Fig. 6.8 Resonant circuit

$$= \frac{R_L(R + jX_L)}{R_L + R + jX_L} = \frac{R_L R}{R_L + R + jX_L} + j\frac{(X_L R_L)}{R + R + jX_L}$$

Neglecting the losses in the capacitor C, the η of the above circuit is,

Efficiency $= \eta =$ output power across R_L/Input power

$$\eta = \frac{I_L^2 . R_L}{I_L^2 R_L + I_a^2 R}$$

I_L = current through load resistance R_L

I_a = current through inductor inductance with its internal resistance R in series.

At resonance, the $|Z|$ is only, resistive.

R = Series resistance of 'L'. $R_L{}^1$ is internal resistance

Let $Q_0 = \dfrac{\omega_0 L}{R}$

= Q of the coil at resonance

Let $Q_{eff} = \dfrac{\omega_0 L}{R + R_L}$

= Q of the coil shunted by R_L'. (Taking R_L into consideration)

$\therefore$ $$\eta = \frac{R_L}{R + R_L}$$

This equation can be written as,

$$\text{Efficiency} \quad = \eta = \frac{\dfrac{1}{Q_{eff}} - \dfrac{1}{Q_0}}{1/Q_{eff}} = 1 - \frac{Q_{eff}}{Q_0}$$

Q_0 = Q factor at resonance frequency f_0.

Q_{eff} = Effective value of Q

$Q_0 >> Q_{eff}$, $\eta \simeq 1$ or 100% (or it is very high). If R_L can be varied, Q_{eff} can be made as small as desired. The value of Q_0 is usually large.

The purpose of resonant circuits in tuned circuits is,

1. To provide correct load |Z|
2. To reject unwanted harmonics
3. To couple power to load

These tuned circuits are sometimes called Tank circuits because, like water tank, energy can be stored in inductance and capacitance energy storage elements, if they are ideal.

6.4.5 Tank Circuits

Fig. 6.9 Tank circuits

R_L = equivalent circuits R_L in series with inductance, resistance

Neglecting losses in capacitors,

$$\eta = \frac{I_L^2 R_L}{I_L^2 R_L + I_a^2 R}$$

For the equivalent circuit,

$$R_L{}^1 = \frac{\omega_0^2 L^2}{R_L} \quad (R_L >> \omega_0 L)$$

For the equivalent circuit

$$\eta = \frac{I_b^2 R_L^2}{I_b^2 \left(R + R_L\right)} = \frac{R_L}{R + R_L}$$

Let $Q_0 = \dfrac{\omega_0 L}{R}$ = Q of the coil at resonance.

$$Q_{eff} = \frac{\omega_0 L}{R + R_L^1} = \text{Q of the coil shunted by } R_L.$$

$$\therefore \qquad \eta = \frac{(1/Q_{eff}) - (1/Q_0)}{(1/Q_{eff})}$$

$$= 1 - \frac{Q_{eff}}{Q_0}$$

6.4.6 Mutual Inductance Coupled Output Resonant Circuit

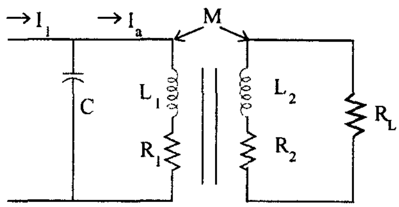


Fig. 6.10 Mutual Inductance coupled resonant circuit

6.4.7 Equivalent Circuit

Power dissipated in R_2 and R_L

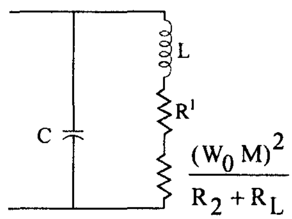


Fig. 6.11 Equivalent circuit

$$P = I_a^2 \frac{\omega_0^2 M^2}{R_2 + R_L}$$

Power dissipated in R_L can be obtained by multiplying the above equation by $\frac{R_L}{R_2 + R_L}$.

6.5 Wideband Amplifiers

The frequency response of a given amplifier can be extended by adding few passive circuit elements to the basic amplifier.

6.5.1 Shunt Compensation

One simple method of shortening the rise time in the response of an amplifier circuit and thus enhancing the high frequency response of the amplifier. (pulse having, sudden change in the input is considered as high frequency variation) is to add an inductor in series with V_{CC} and collector.

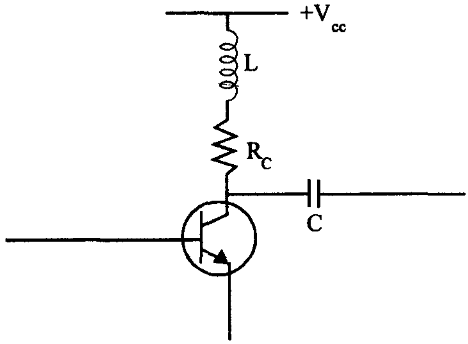


Fig. 6.12 Shunt compensation circuit

In the a.c equivalent circuit, this 'Inductance' will be in parallel with capacitor. Thus 'Inductance Capacitor' combinations changes the output response. Since in shunt in the output stage, this is called *shunt compensated amplifier*. The collector circuit $Z = R_C + jwL$.

This increases with frequency. So V_0 increases and gain increases. So if 'Inductance' is not present, the gain will be less. When '*capacitor*' is present in the output circuit, X_C decreases as f increases. Thus L will compensate for capacitor.

So for compensated amplifier, when L is introduced, the damping factor K is defined as,

$$K = R_C \cdot \sqrt{\frac{C}{L}}$$

$$f_2 = \frac{1}{2\pi R_c C}$$

Where f_2 is the upper 3 db point of the uncompensated amplifier.

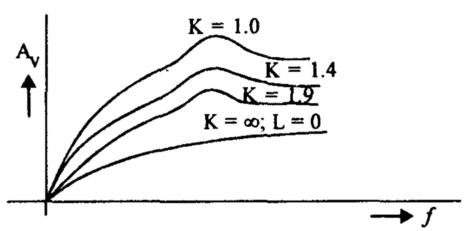


Fig. 6.13 Frequency response

So the frequency response changes, when 'L' is added :

The bandwidth of an amplifier circuit can be increased by decreasing f_1 and increasing f_2.

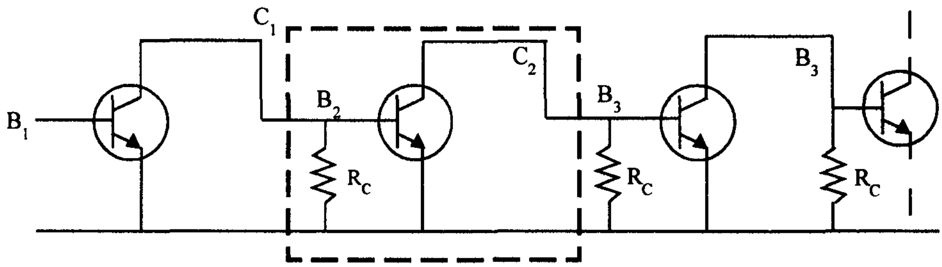
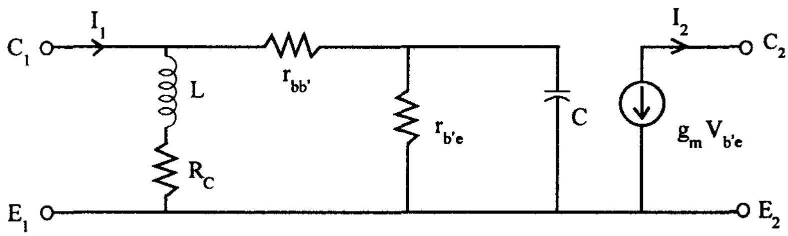


Fig. 6.14 Simplified circuit



$C = C_e + C_C(1 - A)$ Where A is the gain of the angle (I stage)

Fig. 6.15 Equivalent circuit

6.5.2 Extension of Low Frequency Range

Low frequency range can be extended by decreasing f_1 (Since the region as seen from the mid frequency range becomes more if f_1 is decreased). For resistance capacitance coupled amplifier,

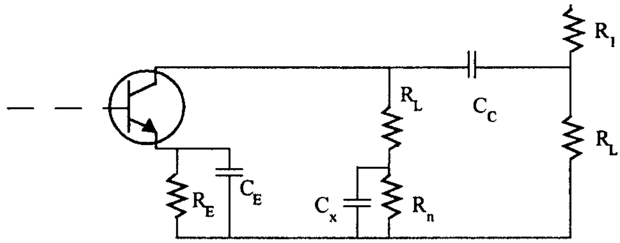
$$f_1 = \frac{1}{2\pi C_c (R_C + R_L)}$$

Where C_C is the coupling capacitor, f_1 can be decreased by increasing C_C. If the value of C_c were to be large, its cost and size will be more. So there is a limit to which C_c can be increased. Hence, to get lesser value of f_1, R should be increased. This is known as *Compensation.* Instead of changing the value of C, to get decrease in f_1 we are changing the value of R. Thus R is compensating for the effect of C.

Now if R were to be fixed and load Z were to change with frequency, another capacitor C_c is connected in parallel with load resistance R_L so that the net load Z, is Z_L so that Z_L increases as f decrease. So f_1 can be increased. This is known as *Compensation.*

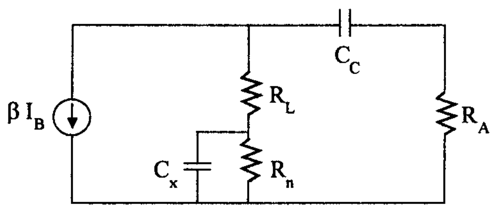
But the value of f_1 is very small (few hundreds MHz) compared to f_2. Therefore $j\omega$ is increased effectively by increasing f_2.

6.5.3 Circuit for Extending Low Frequency Range (Fig. 6.16)



(a) Kinks in frequency response

6.5.4 Low Frequency Equivalent Circuit with Transistor Replaced by a Current Source



(b) Equivalent circuit with current source

Fig. 6.16

6.5.5 Extension of High Frequency Range

Bandwidth of a given amplifiers can be effectively increased by increasing f_2. (since $f_2 >> f_1$) f_2 can be increased by decreasing C_S. But there is a limit to which C_S value can be reduced f_2 can also be increased by decreasing $R_L{}^1$. But if $R_L{}^1$ is reduced the mid band gain will reduce. Therefore without changing the value of C_S and $R_L{}^1$ and without decreasing the mid band gain, f_2 can be increased by compensating techniques.

There are two different methods :

(i) Series compensation

(ii) Shunt compensation

This classification is depending upon character '*Inductance*' is in series or in shunt with the oad resistance in the a.c equivalent circuit.

$$\left|\frac{A_H}{A_M}\right|^2 = \frac{1+m^2\left(\dfrac{\omega}{\omega_2}\right)^2}{1+m^2\left(\dfrac{\omega}{\omega_2}\right)^2+m^2\left(\dfrac{\omega}{\omega_2}\right)^4}$$

where $m = \omega_2 L/R_1$ (R_1 is the resistance in series or the resistance of the coil itself)

ω_2 is the upper cutoff frequency of the uncompensated amplifier.

For a shunt peaked amplifier, for different values of m, the response will be as shown.

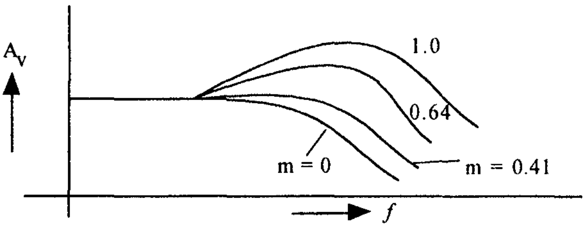


Fig. 6.17 Kinks in frequency response

If m = 0.414, $\omega_2^1 = 1.72\ \omega_2$ where $\omega_2{}^1$ is the upper cutoff frequency with compensation. For this value of 'm', there will not be peaking of the mid band gain. For higher value of m, there will be peaking. So m = 0.414 value is often used. Because of resonance, the voltage across C_S or the output voltage will be maximum. So overshoot occurs.

6.5.6 Series Peaked Circuit

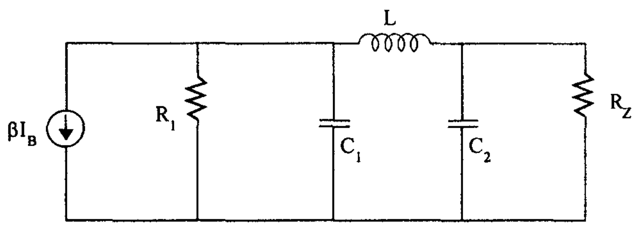


Fig. 6.18 Series peaked circuit

Series peaked circuit is used if $\dfrac{C_1}{C_1 + C_2} = a = 0.25.$

If any other type of capacitances and shunt capacitances are present, this is not used. Shunt compensated circuit is preferred over series peaked since, for shunt compensated value circuits, the gain falls smoothly beyond f_2. For series compensated circuits, there will be sudden drop in gain beyond f_2.

Because of the presence of both Inductance and Capacitance, in the circuit the f_2 point will be near about the resonant frequency of the circuit. Overshoot or peaking in gain will occur near about the resonant frequency. This will depend upon the Q factor of the circuit. As Q increase peak gain increases.

6.6 Tuned Amplifiers

6.6.1 Impedance Transformation

When a signal generator is to supply power to a load or amplifier is to supply output power to a load (driving a load), for maximum power transfer the output impedance of the signal generator or amplifier Z_0 must be complex conjugate of load impedance Z_L according to maximum power transfer theorem. In other words, their magnitudes must be the same.

i.e., $\quad |Z_L| = |Z_0|$

This is konwn as *Impedance Matching.*

In the case of audio amplifiers, the load is usually a loudspeaker. Its impedance is of the order of 4Ω, 8Ω or 16Ω. But the audio amplifier circuit may not have output impedance equal to these values. So impedance matching condition is not satisfied.

Similarly a radio transmitter will have typically output impedance of 4000Ω. It is required to supply power to an antenna. Antenna will hae usually impedance of 70Ω. So impedance matching condition is not satisfied for maximum power transfer, impedance transformation must be used in such coupled circuits.

Some of the methods by which impedance transformation is done in coupoled circuits are :

1. Transformation of impedances with tapped resonant circuits
   (a) by tapping inductors
   (b) by tapping capacitors
2. Reactance section for impedance transformation
3. Image impedances - Reactance matching
4. Reactance T Networks for impedance transformation

6.6.2 Transformation of impedances with tapped resonant circuits

Consider a parallel LC tuned circuit connected to a generator. At antiresonant frequency, the net impedance of the tuned circuit is only resistive and say it is R_{ar} (resistance at anti resonance). The generator sees a load of R_{ar} at anti resonance. R_{ar} is independent of L and C values of the tuned circuit. This value of R_{ar} may be greater than or less than the generator output resistance for maximum power transfer. The resistive impedance into which the generator supplied power can be reduced by tapping the external generator connections across only a portion of the impedance is shown in Fig. 6.19.

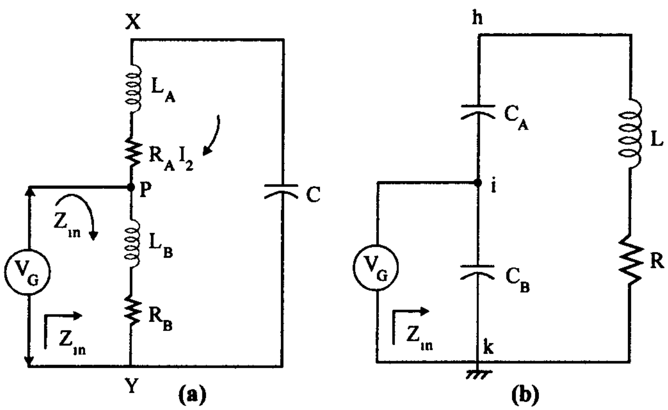


Fig. 6.19 (a) Equivalent circuit with current source

Let the mutual inductance between L_A and L_B is such that the total iinductance is,

$$L = L_A + L_B + 2M \quad .....(19)$$

Anti resonance will occur between points P and Y if,

$$\omega\,(L_A + L_B + 2M) = \frac{1}{\omega_C} \qquad .....(20)$$

Consider the terminals P and Y of Fig. 4.35(a) :
Anti resonance will occur if

$$\omega\,(L_B + M) = \frac{1}{\omega_C} - \omega\,(L_A + M) \qquad .....(21)$$

Because tapping is done in the inductor, part of the inductor is in series with capacitor C. But still, the net reactance must be capacitive for this branch.

The circuit equations in matrix force for the Fig. 6.18 (a) are :

$$\begin{bmatrix} V_G \\ O \end{bmatrix} = \begin{bmatrix} R_B + jX_{LB} & -\left(R_B + jX_{LB} + jX_M\right) \\ -\left(R_B + jX_{LB} + jX_M\right) & \left(R_A + R_B + jX_{LA} + jX_{L_B} + j2X_M - jX_C\right) \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} \qquad .....(22)$$

Since $\qquad Z_{in} = Z_{P,\,Y} = \Delta/\Delta_{11}$,

$$Z_{P,\,Y} = \frac{\left(R_B + jX_{LB}\right)\left(R_A + R_B + jX_{LA} + jX_{LB} + j2X_M - jX_C\right) - \left(R_B + jX_{LB} + jX_M\right)^2}{R_A + R_B + jX_{LA} + jX_{LB} + j2X_M - jX_C} \qquad .....(23)$$

If $\qquad R_A + R_B, = R$

$$Z_{P,\,Y} = R_B + jX_{LB} - \frac{\left(R_B + jX_{LB} + jX_M\right)}{R + j\left(X_L - X_C\right)} \qquad .....(24)$$

If the Q factor of the circuit is high, and the circuit is in anti resonance, then $X_L = X_C$.

$X_{LB} >> R_B$. So R_B can be neglected.

$$\therefore \qquad Z_{P,Y} = jX_{LB} + \frac{\left(X_{LB} + X_M\right)^2}{R} \qquad .....(25)$$

If Q value is reasonable, X_{LB} is small compared to $(X_{LB} + X_M)^2 / R$. So the term X_{LB} can be neglected. Comparing the value of impedance $Z_{2,\,3}$ with resonant impedance across the terminals X and Y, where

$$Z_{X,\,Y} = \frac{R^2 + \omega^2 L^2}{R} = \frac{R^2 + X_L^2}{R} \qquad .....(26)$$

Then $$\frac{Z_{P,Y}}{Z_{X,Y}} = \frac{(X_{LB} + X_M)^2}{R^2 + X_L^2} \qquad .....(27)$$

Again if Q is high $\left(Q = \frac{\omega L}{R}\right)$, R must be small, or $R << X_L$. Then simplifying,

$$\frac{Z_{P,Y}}{Z_{X,Y}} = \frac{(X_{LB} + X_M)^2}{X_L^2} = \frac{(L_B + M)^2}{L^2} \qquad .....(28)$$

Considering Fig. 6.19 (b), if the circuit capacitance is split into two capacitors in series, equivalent in capacitance to the single capacitor C, and if the external generator is tapped between the two capacitors,

since $$\omega L = \frac{1}{\omega C},$$

$$Z_{i,k} = \frac{(X_{C2})^2}{R} \qquad .....(29)$$

and $$Z_{n,k} = \frac{(X_{C1} + X_{C2})^2}{R} \qquad .....(30)$$

The effect of tapping down in the capacitive side of the circuit is :

$$\frac{Z_{i,k}}{Z_{n,k}} = \frac{(X_{C2})^2}{(X_{C1} + X_{C2})^2} = \frac{C_1^2}{(C_1 + C_2)^2} \qquad .....(31)$$

This shows that impedance is reduced.

These methods become very convinient at high frequencies.

6.6.3 Reactance L Section for impedance transformation :

R is the load resistance R_{in}'is the net input resistance for the generator. $R < R_{in}$. R is to be matched with R_{in} through impedance transformation. So two reactances of opposite sign i.e., X_L and X_C are to be connected as shown in Fig. 6.20. L and C elements are connected in the shape of L. So it is called as L-section circuit. At a particular frequency, the oppposite reactances X_L and X_C and R can be transformed to match R_{in}.

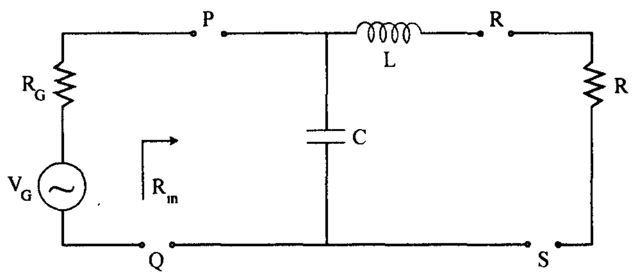


Fig. 6.20 Reactive L section for impedance transformation ($R < R_a$)

The RLC section of the circuit is a parallel resonant circuit. At anti resonance, it appears as a resistance load for the generator. The value of the resistance load depends upon L/C ratio such that R_{in} is matching with R_a for the parallel RLC resonant circuit,

$$\omega = \sqrt{\frac{1}{LC} - \frac{R^2}{L^2}} \qquad .....(32)$$

Resistance at anti resonance, $R_{ar} = R_{in} = \dfrac{L}{CR}$

$\therefore \qquad L = R_{in} RC$

Substituing this value of L in eqn. (ii),

$$\omega^2 = \frac{1}{R_{in} RC^2} - \frac{1}{R_{in}^2 C^2} \qquad .....(33)$$

$$\omega C = \sqrt{\frac{R_{in} - R}{R_{in}^2 R}}$$

Value of capacitance C needed for the L-section is,

$$C = \frac{1}{\omega R_{in}} \sqrt{\frac{R_{in}}{R} - 1}$$

Similarly from eqn. (ii),

$$C = \frac{L}{R_{in} R}$$

Substituting this value in eqn. (32) for ω^2,

$$\omega^2 = \frac{R_{in} R}{L^2} - \frac{R^2}{L^2}$$

$$\omega L = \sqrt{R_{in} R - R^2}$$

$$\therefore \qquad L = \frac{R}{\omega}\sqrt{\frac{R_{in}}{R} - 1} \qquad .....(34)$$

So L is the value of inductance needed for the L section to ensure the desired value of load R_{in} where $R < R_{in}$.

6.6.4 Image Impedances : Reactance Matching :

The impedances Z_1, Z_2 and Z_3 are arranged in the form of T-Network V_a is the generator having internal impedance Z_{1i}. The load impedance is Z_{2i}. The circuit is shown in Fig. 6.21.

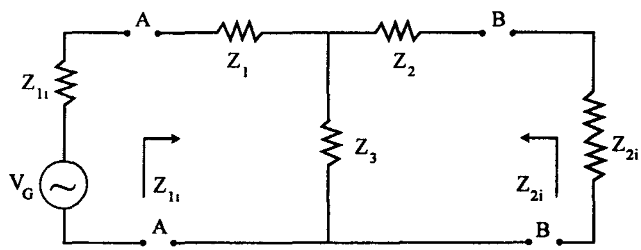


Fig. 6.21 T-Network - Image Impedances

The generator supplies power into the terminals AA. So the impedance betweeen terminals AA must be equal to the generator impedance. The impedance looking into terminals BB must be equal to load Z_{2i}. The impedance at AA looking into one direction is the image impedance of the impedance looking in the other direction. Z_{1i} is called the impedance of the network.

Similarly at B, B terminals the impedance looking is one direction is the same as that looking in the other so that Z_{2i} is also an image impedance at B, B terminals. The network is then said to be matched on an image basis.

The value of image impedance of the T-section is computed as shown below.

The impedance $Z_{1\,in}$ between A, A terminals is,

$$Z_{1\,in} = Z_{1i} = Z_1 + \frac{Z_3 (Z_2 + Z_{2i})}{Z_2 + Z_3 + Z_{2i}} \qquad .....(35)$$

The impedance looking into B, B terminals is required to be Z_{2i}.

$$Z_{2i} = Z_2 + \frac{Z_3 (Z_1 + Z_i)}{Z_1 + Z_3 + Z_{1i}} \qquad .....(36)$$

Solving for Z_{1i} and Z_{2i}

$$Z_{1i} = \sqrt{\frac{(Z_1 + Z_3)(Z_1 Z_2 + Z_2 Z_3 + Z_3 Z_1)}{Z_2 + Z_3}} \quad .....(37)$$

$$Z_{2i} = \sqrt{\frac{(Z_2 + Z_3)(Z_1 Z_2 + Z_2 Z_3 + Z_3 Z_1)}{Z_1 + Z_3}} \quad .....(38)$$

If impedance is measured between terminals AA of the T-section, and terminals B, B are open circuited,

$$Z_{1OC} = Z_1 + Z_3 \quad .....(39)$$

Similarly if impedance is measured at A, A terminals with B, B terminals short circuited,

$$Z_{1\,SC} = Z_1 + \frac{Z_2 Z_3}{Z_2 + Z_3}$$

$$= \frac{Z_1 + Z_2 + Z_2 Z_3 + Z_3 Z_1}{Z_2 + Z_3} \quad .....(40)$$

So the image impedance $Z_{1\,i} = \sqrt{Z_{1OC} Z_{1SC}}$

Similarly for the measurements made at B, B terminals gives

$$Z_{ZC} = \sqrt{Z_{2OC} Z_{2SC}}$$

So a porperly designed T network will have the property of transformation of an impedance to produce matching of a load and a source.

6.6.5 Reactance T Networks for impedance transformation :

In the T-network shown in Fig. 6.22 the T Network elements are reactances only, either capacitive or inductive. V_a is a generator with internal resistance R_1. It is connected to a lod R_2 through T-Network.

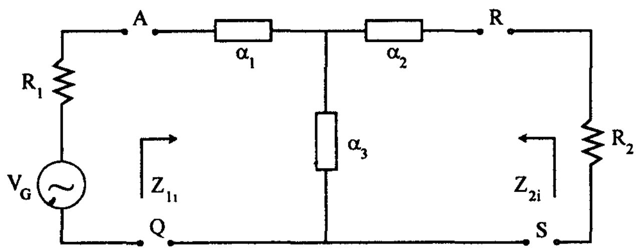


Fig. 6.22 Reactance T-Network

If the generator is to transfer maximum power to the laod, it is necessary only that the image impedance Z_{1i} at terminals P,Q must be equal to R_1. In other words, the load impedance R_2 is transformed by the T-network to a value at the P,Q terminals equal to R_1.

When R_2 is connected, the image impedance Z_{1i} must be

$$Z_{1i} = R_1 = jX_1 + \frac{jX_3(R_2 + jX_2)}{R_2 + jX_2 + jX_3} \quad .....(41)$$

X may have either positive sign or negative sign, i.e., it may be either inductive or capacitive in nature. Then, $R_1 R_2 + j R_1 (X_2 + X_3)$

$$= -(X_1 X_2 + X_2 X_3 + X_3 X_1) + jR_2 (X_1 + X_3)$$

By equating real terms,

$$R_1 R_2 = -(X_1 X_2 + X_2 X_3 X_3 + X_1) \quad .....(42)$$

In the above equation, $R_1 R_2$ term on the LHS is positive. So the term on RHS must also be positive. Since it is negative sign, one or more of the three terms on RHS must be positive. X can be $+jWL$ or $\frac{-j}{WC}$. In order that the product term $X_1 X_2$ is positive, X_1 can be $+jX_a$ and X_2 can be $-jX_a$ $(-jX_b) = +X_a X_b$. This requires that one reactive arm of the T-Network be opposite in sign to the sign of the other two arms. So the T-Network must consist of one capacitance and two inductances or Vice-versa.

By equating imaginary terms,

$$R_1 (X_2 + X_3) = R_2 (X_1 + X_3)$$

$$X_2 + X_3 = \frac{R_2}{R1} (X_1 + X_3) \quad .....(43)$$

The above equation may be written as,

$$R_1 R_2 = -[(X_1 + X_3)(X_2 + X_3) - X_3^2] \quad .....(44)$$

$$\therefore \quad R_1 R_2 = -\left[(X_1 + X_3)^2 \frac{R_2}{R_1} - X_3^2\right]$$

$$X_1 + X_3 = \pm\sqrt{\frac{R_1}{R_2}\left(X_3^2 - R_1 R_2\right)} \quad .....(45)$$

So the value of one of the reactance arms is,

$$X_1 = -X_3 \pm \sqrt{\frac{R_1}{R_2}\left(X_3^2 - R_1 R_2\right)} \qquad .....(46)$$

Substituting eqn. (46) in (44),

$$X_2 + X_3 = \pm \frac{R_2}{R_1}\sqrt{\frac{R_1}{R_2}\left(X_3^2 - R_1 R_2\right)}$$

or

$$X_2 + X_3 = \pm \sqrt{\frac{R_1}{R_2}\left(X_3^2 - R_1 R_2\right)} \qquad .....(47)$$

The above equations are the design equations for the T-Network, in terms of the values of X_3.

Objective Type Questions

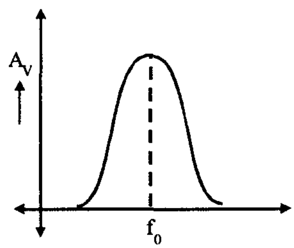
1. The purpose of resonant circuits in tuned circuits is ______________.
2. Give the classification of tuned amplifiers.
3. What are the applications of tuned amplifiers ?
4. Give the frequency response of a tuned amplifier.
5. What is the expression for Rp in terms of ω, L, R ? What is Rp ?
6. What is δ called ? What is the expression in terms of ω, ω_0 ?
7. What is A/Ao ?
8. Why do we go for tapped single tuned amplifier ?
9. What is maxium power transfer theorem ?
10. What is a double tuned amplifier ?
11. What is staggered tuning ?
12. At what frequencies are the tuned amplifiers operate ?
13. What is a tank circuit ?
14. What is the expression for harmonic distortion in tuned amplifiers ?
15. How do you build a class B tuned amplifier ?

Essay Type Questions

1. Draw the circuit for BJT tuned class B/C amplifier. Explain its working.
2. Draw the circuit for JFET tuned R.F. amplifier and explain its working.
3. Explain the principle and working of wide band amplifiers.

Answers to Objective Type Questions

1. (a) To provide properly matching load impedance
 (b) To reset unwanted harmonics
 (c) To couple power to load.
2. Single tuned, double tuned, stagger tuned amplifiers.
3. RF amplifiers, communication receivers.
4.



5. $R_p = \dfrac{\omega^2 L^2}{R}$, R_p is the series internal resistance of inductor represented as a shunt element.
6. δ - fractional frequency variation. $\delta = \dfrac{\omega - \omega_o}{\omega_o}$
7. $\dfrac{A}{A_o} = \dfrac{1}{1 + j2\delta Q_e}$
8. For impedance matching.
9. For a linear circuit, for the maximum power to he delivered to the load the output or load impedance should be the complex conjugate of the effective or equivalent input impedance of the circuit.
10. It has two resonant circuits both tuned to the same frequency.
11. Two resonant circuits tuned to different frequencies.
12. High or radio frequencies.
13. Parallel LC circuit is called a tank circuit.
14. There is very negligible harmonic distortion in tuned amplifiers as they are narrow band amplifiers.
15. By removing the bias resistors from class A amplifier, we can build a class B amplifier.

UNIT - 7

Voltage Regulators

In this Unit,

- Different types of Voltage Regulator Circuits are explained.
- Terminology associated with Voltage Regulator Circuits is given.
- I.C. Voltage Regulator Circuits, 3 terminal Voltage Regulator Circuits are explained.
- Voltage Multiplier Circuits, Voltage Doubler Circuits are also given.
- Voltage Tripler, quadrupler circuits are explained. Numerical examples are also given.

7.1 Introduction

Voltage Regulator Circuits are electronic circuits which give constant DC output voltage, irrespective of variations in *Input Voltage* V_i, *current drawn by the load* I_L from output terminals, and *Temperature T*. Voltage Regulator circuits are available in discrete form using BJTs, Diodes etc and in IC (Integrated Circuit) form. The term voltage regulator is used when the output delivered is DC voltage. The input can be DC which is not constant and fluctuating. If the input is AC, it is converted to DC by Rectifier and Filter Circuits and given to I.C. Voltage Regulator circuit, to get constant DC output voltage. If the input is A.C 230 V from mains, and the output desired is constant DC, a stepdown transformer is used and then Rectifier and filter circuits are used, before the electronic regulator circuit. The block diagrams are shown in Fig. 7.1 and 7.2.

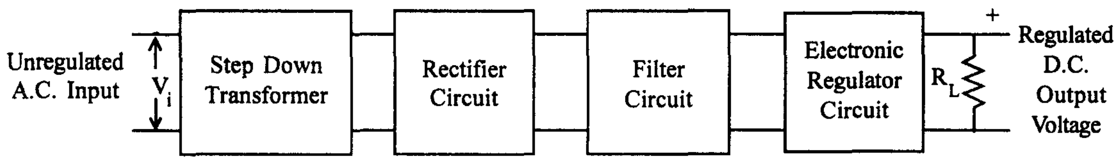


Fig. 7.1 Block Diagram of Voltage Regulator with A.C Input

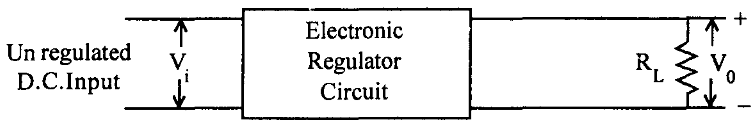


Fig. 7.2 Block Diagram of Voltage Regulator with D.C Input

The term *Voltage Stabilizer* is used, if the output voltage is AC and not DC. The circuits used for voltage stabilizers are different. The voltage regulator circuits are available in IC form also. Some of the commonly used ICs are, μA 723, LM 309, LM 105, CA 3085 A.

7805, 7806, 7808, 7812, 7815 : Three terminal positive Voltage Regulators.

7905, 7906, 7908, 7912, 7915 : Three terminal negative Voltage Regulators.

The Voltage Regulator Circuits are used for electronic systems, electronic circuits, IC circuits, etc.

The specifications and Ideal Values of Voltage Regulators are :

Specifications		Ideal Values
1. Regulation (S_V)	:	0 %
2. Input Resistance (R_i)	:	∞ ohms
3. Output Resistance (R_0)	:	0 ohms
4. Temperature Coefficient (S_T)	:	0 mv/oc.
5. Output Voltage V_0	:	-
6. Output current range (I_L)	:	-
7. Ripple Rejection	:	0 %

7.1.1 Different types of Voltage Regulators are

1. Zener regulator
2. Shunt regulator
3. Series regulator
4. Negative voltage regulator
5. Voltage regulator with foldback current limiting
6. Switching regulators
7. High Current regulator

7.1.2 Zener Voltage Regulator Circuit

A simple circuit without using any transistor is with a zener diode Voltage Regulator Circuit. In the reverse characteristic voltage remains constant irrespective of the current that is flowing through Zener diode. The voltage in the break down region remains constant. (Fig. 7.3)

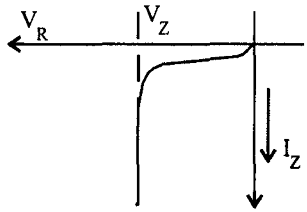


Fig. 7.3 Zener diode reverse characteristic

Therefore in this region the zener diode can be used as a voltage regulator. If the output voltage is taken across the zener, even if the input voltage increases, the output voltage remains constant. The circuit as shown in Fig. 7.4.

The input V_i is DC. Zener diode is reverse biased.

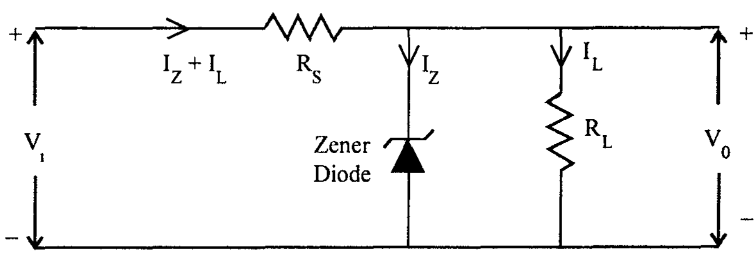


Fig. 7.4 Zener regulator circuit

If the input voltage V_i increases, the current through R_s increases. This extra current flows, through the zener diode and not through R_L. Therefore zener diode resistance is much smaller than R_L when it is conducting. Therefore I_L remains constant and so V_0 remains constant.

The limitations of this circuits are

1. The output voltage remains constant only when the input voltâge is sufficiently large so that the voltage across the zener is V_Z.
2. There is limit to the maximum current that we can pass through the zener. If V_i is increased enormously, I_Z increases and hence breakdown will occur.
3. Voltage regulation is maintained only between these limits, the minimum current and the maximum permissible current through the zener diode. Typical values are from 10m A to 1 ampere.

7.1.3 Shunt Regulator

The shunt regulator uses a transistor to amplify the zener diode current and thus extending the Zener's current range by a factor equal to transistor h_{FE}. (Fig. 7.5)

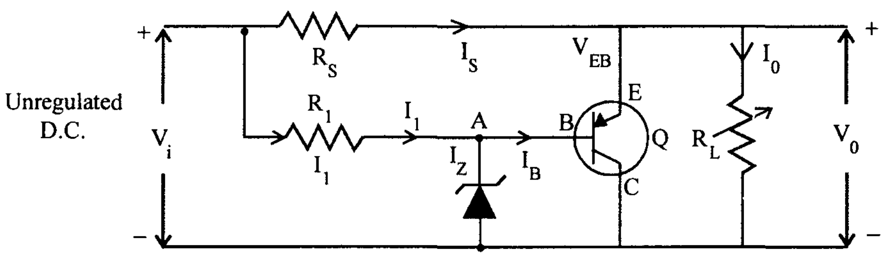


Fig. 7.5 Shunt Regulator Circuit

Zener current, passes through R_1

Nominal output voltage

$$= V_Z + V_{EB}$$

The current that gets branched as I_B is amplified by the transistor. Therefore the total current $I_0 = (\beta + 1)\ I_B$, flows through the load resistance R_L. Therefore for a small current through the zener, large current flows through R_L and voltage remains constant. In otherwords, for large current through R_L, V_0 remains constant. Voltage V_0 does not change with current.

Example : 7.1

For the shunt regulator shown, determine

1. The nominal voltage
2. Value of R_1,
3. Load current range
4. Maximum transistor power dissipation.
5. The value of R_S and its power dissipation.

V_i = Constant. Zener diode 6.3V, 200mW, requires 5mA minimum current.

Transistor Specifications :

$$V_{EB} = 0.2V,\ h_{FE} = 49,\ I_{CBO} = 0.$$

1. The nominal output voltage is the sum of the transistor V_{EB} and zener voltage.

$$V_0 = 0.2 + 6.3 = 6.5V = V_{Eb} + V_Z$$

2. R_1 must supply 5mA to the zener diode :

$$\therefore \qquad R_1 = \frac{8V - 6.3}{5 \times 10^{-3}} = \frac{1.7}{5 \times 10^{-3}} = 340\ \Omega$$

3. The maximum allowable zener current is

$$\frac{\text{Power rating}}{\text{Voltage rating}} = \frac{0.2}{6.3} = 31.8 \text{ mA}$$

The load current range is the difference between minimum and maximum current through the shunt path provided by the transistor. At junction A, we can write,

$$I_B = I_Z - I_1$$

I_1 is constant at 5 mA

$$\therefore \qquad I_B = I_Z - I_1$$

I_1 is constant at 5 mA

$$\therefore \qquad I_B = 5 \times 10^{-3} - 5 \times 10^{-3} = 0$$

$$I_B = I_{Z\ Max} - I_2$$

$$= 31.8 \times 10^{-3} - 5 \times 10^{-3} = 26.8 \text{ mA}$$

The transistor emitter current $I_E = I_B + I_C$

$$I_C = \beta\, I_B = h_{FE}\, I_B$$

$$\therefore \qquad I_E = (\beta + 1)\, I_B = (h_{FE} + 1)\, I_B$$

I_B ranges from a minimum of 0 to maximum of 26.8 mA

$\therefore$ Total load current range is $(h_{FE} + 1)\, I_B$

$$= 50\,(26.8 \times 10^{-3}) = \mathbf{1.34\ A}$$

4. The maximum transistor power dissipation occurs when the current is maximum $I_E \simeq I_e$

$$P_D = V_o\, I_E = 6.5\,(1.34) = \mathbf{8.7\ W}$$

5. R_S must pass 1.4 A to supply current to the transistor and R_L.

$$R_S = \frac{V_i - V_0}{1.34} = \frac{8 - 6.5}{1.34} = 1.12\ \Omega$$

The power dissipated by R_S,

$$= I_S^2\, R_S$$

$$= (1.34)^2 \,.\, (1.12) = 24 \text{ W}$$

Regulated Power Supply

An unregulated power supply consists of a transformer, a rectifier, and a filter. For such a circuit regulation will be very poor i.e. as the load varies (*load means load current*) [*No load means no load* *current or 0 current. Full load means full load current or short circuit*], we want the output voltage to remain constant. But this will not be so for unregulated power supply. The short comings of the circuits are :

1. Poor regulation
2. DC output voltage varies directly as the a.c. input voltage varies
3. In simple rectifiers and filter circuits, the d.c. output voltage varies with temperature also, if semiconductors devices are used.

An electronic feedback control circuit is used in conjuction with an unregulated power supply to overcome the above three short comings. Such a system is called a "*regulated power supply*".

Stabilization

The output voltage depends upon the following factors in a power supply.

1. Input voltage V_i
2. Load current I_L
3. Temperature

∴ Change in the output voltage ΔV_0 can be expressed as

$$\Delta V_0 = \frac{\partial V_0}{\partial V_i}.\Delta V_i + \frac{\partial V_0}{\partial I_L}.\Delta I_L + \frac{\partial V_0}{\partial T}.\Delta T$$

$$\Delta V_0 = S_1\,\Delta V_i + R_0\,\Delta I_L + S_T\,\Delta T$$

Where the three coefficients are defined as,

(i) Stability factors.

$$S_V = \left.\frac{\Delta V_0}{\Delta V_i}\right|_{\Delta I_L = 0,\ \Delta_T = 0}$$

This should be as small as possible. Ideally 0 since V_0 should not change even if V_i changes.

(ii) *Output Resistance*

$$R_0 = \left.\frac{\Delta V_0}{\Delta I_L}\right|_{\Delta V_i = 0,\ \Delta_T = 0}$$

(iii) *Temperature Coefficient*

$$S_T = \left.\frac{\Delta V_0}{\Delta_T}\right|_{\Delta V_i = 0,\ \Delta I_L = 0}$$

The smaller the values of the three coefficients, the better the circuit.

7.1.4 Series Voltage Regulator

The voltage regulation (i.e., change in the output voltage as load voltage varies (or input voltage varies) can be improved, if a large part of the increase in input voltage appears across the control transistor, so that output voltage tries to remain constant, i.e., increase in V_i results in increased V_{CE} so that output almost remains constant. But when the input increases, there may be some increase in the output but to a very smaller extent. This increase in output acts to bias the control transistor. This additional bias causes an increase in collector to emitter voltage which will compensate for the increased input.

If the change in output were amplified before being applied to the control transistor, better stabilization would result.

Series Voltage Regulator Circuit is as shown in Fig. 7.6.

Series Voltage Regulator Circuit

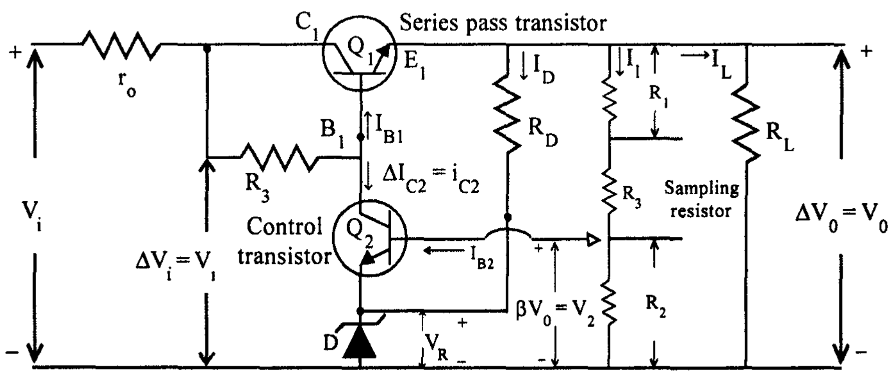


Fig. 7.6 Series Regulator Circuit

Q_1 is the series pass element of the series regulator. Q_2 acts as the difference amplifier. D is the reference zener diode. A fraction of the output voltage bV_0 (b is a fraction, which is taken across R_2 and the potentiometer) is compared with the reference voltage V_R. The difference $(bV_0 - V_R)$ is amplified by the transistor Q_2. Because the emitter of Q_2 is not at ground potential, there is constant voltage V_R. Therefore the net voltage to the Base - Emitter of the transistor Q_2 is $(bV_0 - V_R)$. As V_0 increases, $(bV_0 - V_R)$ increases. When input voltage increases by ΔV_i, the base-emitter voltage of Q_2 increases. So Collector current of Q_2 increases and hence there will be large current change in R_3. Thus all the change in V_i will appear across R_3 itself. V_{BE} of the transistor Q_1 is small. Therefore the drop across $R_3 = V_{CB}$ of $Q_1 \simeq V_{CE}$ of Q_1 since V_{BE} is small. Hence the increase in the voltage appears essentially across Q_1 only. This type of circuit takes care of the increase in input voltages only. If the input decreases, output will also decrease. (If the output were to remain constant at a specified value, even when V_i decreases, buck and boost should be there. The tapping of a transformer should be changed by a relay when V_i changes). r_0 is the output resistance of the unregulated power supply which proceeds the regulator circuit. r_0 is the output resistance of the rectifier, filter circuit or it can be taken as the resistance of the DC supply in the lab experiment.

The expression for S_V (Stability factor) = $\frac{\Delta V_0}{\Delta V_i}$

$$= \left[\frac{R_1 + R_2}{R_2}\right] \cdot \frac{(R_1 \text{in parallel with } R_2) + h_{ie2} + (1 + h_{fe2}) R_z}{h_{fe2} R_3}$$

R_z = Zener diode resistance (typical value)

$$R_0 = \frac{r_0 + \frac{R_3 + h_{ie1}}{1 + h_{fe1}}}{1 + G_m (R_3 + r_0)}; \qquad G_m = \frac{\Delta I_{C2}}{\Delta V_0}$$

The preset pot or trim pot R_3 in the circuit is called as *sampling resistor* since it controls or samples the amount of feedback.

Preregulator

It provides constant current to the collector of the DC amplifier and the base of control element.

If R_3 is increased, the quantity $\frac{R_3 + h_{ie1}}{1 + h_{fe}}$ also increases, but then T is very small, since it is being divided by h_{fe}.

7.1.5 Negative Voltage regulator

Sometimes it is required to have negative voltage viz., –6V, –18V, –21V etc with positive terminal grounded. This type of circuit supplies regulated negative voltages. The input should also be negative DC voltage.

7.1.6 Voltage regulator with foldback current limiting

In high current voltage regulator circuits, constant load current limiting is employed. i.e. The load current will not increase beyond the set value. But this will not ensure good protection. So foldback current limiting is employed. When the output is shared, the current will be varying. The series pass transistors will not be able to dissipate this much power, with the result that it may be damaged. So when the output is shorted or when the load current exceeds the set value, the current through the series transistors decrease or folds back.

7.1.7 Switching regulators

In the voltage regulator circuit, suppose the output voltage should remain constants at +6V, the input can be upto +12V or +15V maximum. If the input voltage is much higher, the power dissipation across the transistor will be large and so it may be damaged. So to prevent this, the input is limited to around twice that of the input. But if, higher input fluctuations were to be tolerated, the voltage regulators IC is used as a switch between the input and the output. The input voltage is not connected permanently to the regulator circuit but ON/OFF will occur at a high frequency (50 KHz) so that output is constantly present.

A simple voltage regulator circuit using *CA3085A* is as shown in Fig. 7.7. It gives 6 V constant output upto 100 mA.

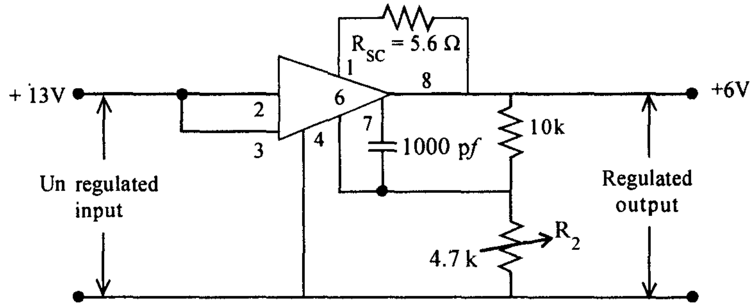


Fig. 7.7 CA 3085A IC Voltage Regulator

$$V_0 = \frac{\beta A_V}{(1+\beta A_V)}$$

$$\beta = \frac{R_2}{R_1+R_2}$$

RCA (Radio Corporation of America) uses for the ICs, alphabets CA. CA3085A is voltage regulator. LM309 K – is another Voltage Regulator IC.

µA716C is head phone amplifier, delivers 50 mW to, 500-600Ω load

CA3007 is low power class AB amplifier, and delivers 30 mW of output power.

MC1554 is 20W class B power amplifier.

Preregulator

The value of the stability factor S_V of a voltage regulator should be very small. S_V can be improved if R_3 is increased (from the general expression) since $R_3 \simeq \frac{(V_i - V_0)}{I}$. We can increase R_3 by decreasing I, through R_3. The current I through R_3 can be decreased by using a Darlington pair for Q_1. To get even better values of S_V, R_3 is replaced by a constant current source circuit, so that R_3 tends to infinity ($R_3 \to \infty$). This constant current source circuit is often called *a transistor preregulator*. V_i is the maximum value of input that can be given.

Short Circuit Overload Protection

Overload means overload current (or short circuit). A power supply must be protected further from damage through overload. In a simple circuit, protection is provided by using a fuse, so that when current excess of the rated values flows, the fuse wire will blow off, thus protecting the components. This fuse wire is provided before r_0. Another method of protecting the circuit is by using diodes.

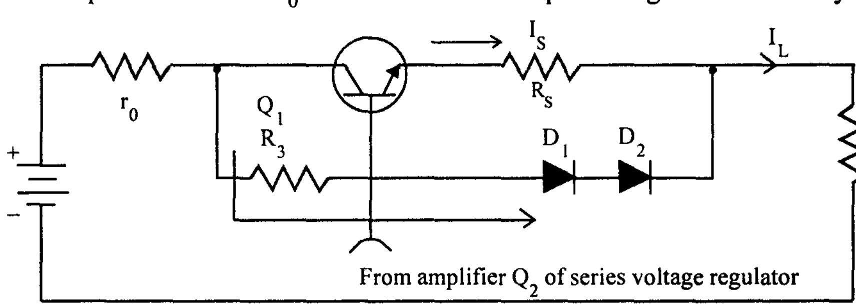


Fig. 7.8 Circuit for short circuit protection

Zener diodes can also be employed, but such a circuit is relatively costly.

The diodes D_1 and D_2 will start conducting only when the voltage drop across R_S exceeds the current in voltage of both the diodes D_1 and D_2. In the case of a short circuit the current I_S will increase upto a limiting point determined by

$$I_S = \frac{V_{\gamma_1} + V_{\gamma_2} - V_{BE1}}{R_S}$$

When the output is short circuited, the collector current of Q_2 will be very high I_S . R_S will also be large.

$\therefore$ The two diodes D_1 and D_2 start conducting.

$\therefore$ The large collector current of Q_2 passes through the diodes D_1 and D_2 and not through the transistor Q_1.

$\therefore$ Transistor Q_1 will be safe, D_1 and D_2 will be generally si diodes, since cut in voltage is 0.6V. So I_S R_S drop can be large.

Example 7.2

Design a series regulated power supply to provide a nominal output voltage of 25V and supply load current $I_L \leq 1A$. The unregulated power supply has the following specifications $V_i = 50 \pm 5V$, and $r_0 = 10\ \Omega$.

Given : $R_Z = 12\ \Omega$ at $I_Z = 10$ mA. At $I_{C2} = 10$ mA, $\beta = 220$, $h_{ie2} = 800\ \Omega$, $h_{fe2} = 200$, $I_1 = 10$ mA.

The reference diodes are chosen such that $V_R \simeq \frac{V_0}{2}$.

$$\frac{V_0}{2} = 12.5\ V$$

$\therefore$ Two Zener diodes with breakdown voltages of 7.5 V in series may be connected.

$$R_Z = 12\ \Omega \text{ at } I_Z = 20 \text{ mA}$$

Choose $\quad I_{C2} \simeq I_{E2} = 10$ mA

At $I_{C_2} = 10$ mA, the h-parameters for the transistor are measured as,

$$\beta = 220, \quad h_{ie2} = 800\ \Omega, \quad h_{fe2} = 200$$

Choose $\quad I_D = 10$ mA, so that $I_Z = I_{D1} + I_{D2} = 20$ mA

$$R_D = \frac{V_0 - V_R}{I_D} = \frac{25-15}{10} = 1K\Omega$$

$$I_{B2} = \frac{I_{C_2}}{\beta} = \frac{10\,mA}{220} = 45\mu A$$

Choose I_1 as 10 mA for si transistors, $V_{BE} = 0.6$ V

$$V_2 = V_{BE2} + V_R = 15.6\ V$$

$$R_1 = \frac{V_0 - V_2}{I_1} = \frac{25-15.6}{10 \times 10^{-3}} = 940\ \Omega$$

$$R_2 \simeq \frac{V_2}{I_1} = \frac{15.6}{10 \times 10^{-3}} = 1{,}560\ \Omega$$

For the transistor Q_1, choose I_2 as 1A and $h_{FE1} = 125$ (d.c. current gain β)

$$I_{B1} = \frac{I_L + I_1 + I_D}{h_{fe1}(\beta)} \qquad \therefore \quad I_{C_1} \simeq I_{E_1} = I_L + I_1 + I_D$$

(DC Current gain)

$$= \frac{1000 + 10 + 10}{125} \simeq 8 \text{ mA}$$

The current through resistor R_3 is $I = I_{B1} + I_{C2} = 8 + 10 = 18$ mA

The value of R_3 corresponding to $V_i = 45$ V and $I_L = 1$A is (since these are given in the problem $V_i = 50 + 5, \acute{4}5$ V)

$$R_3 = \frac{V_i - \left(V_{BE_1} + V_0\right)}{I} = \frac{50 - 25.6}{18 \times 10^{-3}} = 1{,}360\ \Omega.$$

Voltage regulator is a circuit which maintains constant output voltage, irrespective of the changes of the input voltage or the current.

Stabilizer - If the input is a.c, and output is also a.c, it is a stabilizer circuit.

7.2 Terminology

Load Regulation : It is defined as the % change in regulated output voltage for a change in load current from minimum to the maximum value.

E_1 = Output voltage when I_L is minimum (rated value)

E_2 = Output voltage when I_L is maximum (rated value)

$$\% \text{ load regulation} = \frac{E_1 - E_2}{E_1} \times 100\ \%\ ;\ E_1 > E_2. \text{ This value should be small.}$$

Line Regulation : It is the % change in V_0 for a change in V_i.

$$= \frac{\Delta V_0}{\Delta V_i} \times 100\ \%$$

In the Ideal case $\Delta V_0 = 0$ when V_0 remains constant.

This value should be minimum.

Load regulation is with respect to change in I_L

Line regulation is with respect to change in V_i.

Ripple Rejection : It is the ratio of peak to peak output ripple voltage to the peak to peak input ripple voltage.

$$\frac{V_0'(p-p)}{V_i'(p-p)} \quad \begin{array}{l} V_0' = \text{output ripple voltage} \\ V_i' = \text{input ripple voltage} \end{array}$$

Stand by Current Drain **:**

It is the current drawn by the regulator circuit, when $I_L = 0$

(current drawn by the circuit components only and not by the load)

Short Circuit Current Limit **:**

The output current of the regulator (I_L) when the output terminals are shorted.

Sense Voltage **:**

It is the voltage between current sense and current limit terminals.

Temperature Stability or Average Temperature Coefficient **:**

Change in V_0 per unit change in temperature mV/o_C.

7.3 Basic Regulator Circuit

A monolothic voltage regulator circuit mainly consists of 3 parts.

1. Reference voltage circuit
2. Error Amplifier
3. Series pass element

$$V_0 = \frac{\beta A_V}{1+\beta A_V}$$

$$\beta = \frac{R_2}{R_2+R_2}$$

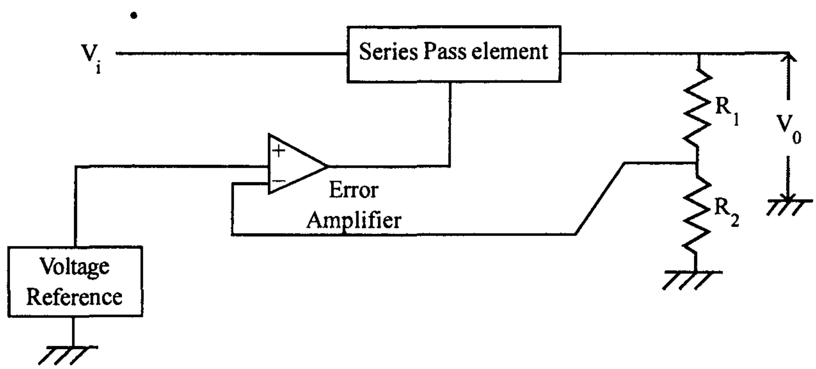


Fig. 7.9 Basic I.C. voltage regulator circuit

Voltage reference circuit generates a constant voltage level. A fraction of the output voltage is derived by the potential divider network R_1, R_2 and this voltage is compared with the reference voltage. The difference in these two voltages is converted into an error signal, which will control the voltage drop across the series pass element, to keep V_0 constant..

If V_0 is less, the drop across series pass element is reduced, so that V_0 increases. If V_0 is more, the drop across series pass element increases so that V_0 decreases and comes to the normal value.

The error amplifiers controls the base current to the series pass element, which is a transistor and the drop across it, V_{CE} varies, as its I_C changes, in proportion to I_B. The characteristics of a good regulator circuit are :

1. It should have low line regulation
2. It should have low load regulation
3. It must have a high degree of ripple rejection

Voltage regulator ICs are provided with 3 kinds of protection

1. Short circuit protection
   (a) *Active current limiting :*
   (b) *Passive current limiting :* This is *foldback* current limiting
2. Over voltage protection
3. Thermal overload protection

7.4 Short Circuit Protection

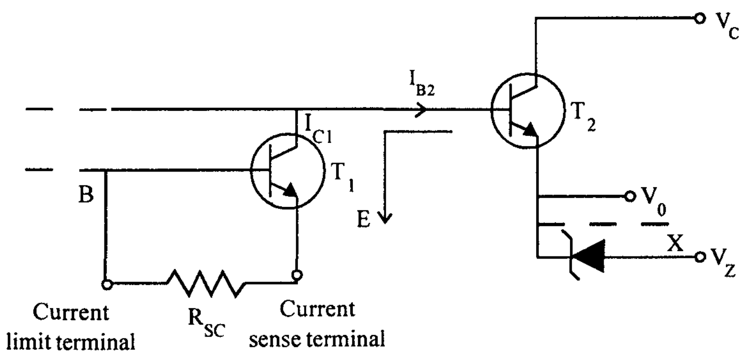


Fig. 7.10 Short circuit protection circuit

7.4.1 Active Current Limiting

Normally *T_1 is off.* A resistor R_{SC} is connected between current limit and current sense terminals. When V_0 is shorted, the drop across R_{SC} is such that T_1 turns ON. When T_1 turns ON, it draws current (I_C flows) and reduces the base drive I_B to the power device T_2.

$\therefore$ I_0 is reduced to zero.

If the short circuit current limit is 65 mA, and cut in voltage V_{BE} for T_1 is 0.65 V, R_{SC} must be such that when 65 mA is reached T_1 should turn ON.

$$\therefore \qquad R_{SC} = \frac{0.65\,\text{V}}{65\,\text{mA}} = 10\Omega$$

Current sense will detect the short circuit. Short circuit current will flow through this terminal.

7.4.2 Foldback Limiting

If the short circuit is not detected, and short circuit condition exists for a long time, due to large current flow, excessive heating will take place, damaging the I-C. In such cases, foldback limiting is employed. When short circuit occurs, I_L decreases and becomes a minimum value.

The circuit is as shown :

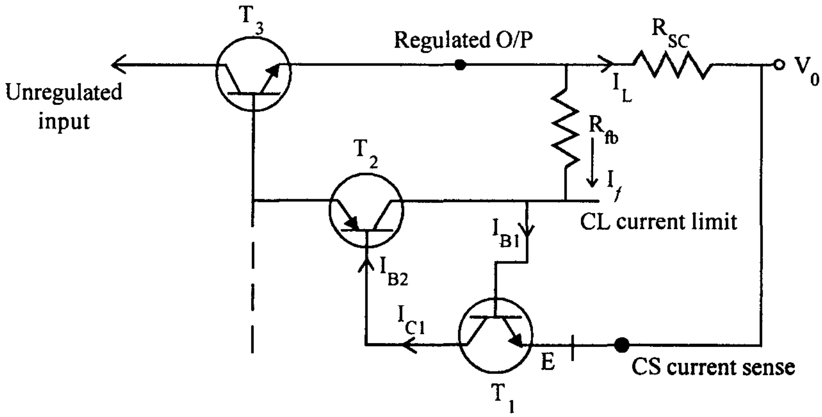


Fig. 7.11 Foldback limiting circuit

T_1 and T_2 are normally off. When I_L increases to a high value, the voltage drop across R_{SC} increases and turns on T_1. T_1 inturn, turns on T_2. Since I_C of T_1 = I_B of T_2, when T_2 turns ON, the base drive for T_3 is reduced. Therefore I_C of T_3 i.e., I_L reduces.

7.4.3 Over Voltage Protection

Here Zener diode is connected between output and ground terminals. When V_0 decreases, the diode starts conducting, maintaining V_0 constant at the breakdown voltage of the zener.

Objective Type Questions

1. The stability factor S_V in Voltage Regulator Circuits is defined as ________________.
2. Output Resistance Ro of Voltage Regulator Circuit is defined as ________________.
3. Temperature coefficient of Voltage Regulator Circuits is defined as ________________.
4. The present pot or trimpot element in the series Voltage Regulator Circuit is called as ________________.
5. The purpose of Pre regulator circuit is the series Voltage Regulator Circuit is ________________.
6. Fold back limiting circuit is also known as ________________.
7. In a voltage stabilizer circuit, the input and outputs are ________________.
8. Load Regulation is defined as ________________.
9. Line Regulation is defined as ________________.
10. Ripple Rejection is defined as ________________.
11. The three important sections of Voltage Regulator I.C.s are ________________.
12. The elements used in Active Current limiting circuit of Voltage Regulators are ________________.

Essay Type Questions

1. Draw the circuit for shunt type Voltage Regulator and explain its working.
2. Explain the terms
   (i) Stabilization
   (ii) Stability factor S_V
   (iii) Output Resistance R_o
   (iv) Temperature Coefficient, pertaining to Voltage Regulators.
3. Draw the circuit for series type voltage regulator and explain its working.
4. What is the function of pre regulator circuit ? Explain.
5. Draw the circuit and explain how short circuit over load protection is provided in Voltage Regulator circuits.
6. Define the terms
   (i) Load Regulation
   (ii) Line Regulation
   (iii) Ripple Rejection
   (iv) Sense Voltage
   (v) Temperature stability pertaining to Voltage Regulator ICs.

Answers of Objective Type Questions

1. $S_V = \left.\dfrac{\Delta V_o}{\Delta V_i}\right| \Delta I_L = 0, \Delta T = 0$

2. $R_o = \left.\dfrac{\Delta V_o}{\Delta I_L}\right| \Delta V_i = 0, \Delta T = 0$

3. $S_T = \left.\dfrac{\Delta V_o}{\Delta T_0}\right| \Delta V_i = 0, \Delta I_L = 0$

4. Sampling Resistor
5. It provides constant current to the collector of the d.c. amplifier and base of control element.
6. Crow - bar limiting circuit
7. a.c.
8. $(V_1 - V_2/V_1) \times 100\ \%$
9. $\left(\dfrac{\Delta V_o}{\Delta V_i}\right) \times 100\ \%$
10. $\dfrac{V_0^1(p-p)}{V_i^1(p-p)}$
11. (a) Reference Voltage Circuit
    (b) Error Amplifier
    (c) Series Pass Element
12. Transistors, Resistors, Zener Diodes.

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UNIT - 8

Switching and IC Voltage Regulators

In this Unit,

- IC 723 Voltage Regulators and 3 terminal IC Regulators
- Current Limiting
- Specifications of Voltage Regulator Circuits
- DC to DC Converters
- Switching Regulators
- Voltage Multipliers
- UPS and SMPS

8.1 IC 723 Voltage Regulators and 3 Terminal IC Regulators

1. Current sense — 2. Inverse input
3. Non Inverse input — 4. V_{ref}
5. $-V_{CC}$ — 6. V_{out}
7. V_C — 8. $+V_{CC}$
9. Frequency compensation — 10. Current limit

V^- (pin 5) can be grounded 8 and 7 are shorted and DC V_i is given.

$$V_R = V_{23} = 5\text{ V}$$
$$R = 10\ \Omega\ \text{(Ohms)} \qquad I_L \simeq 0.5\text{ A}$$

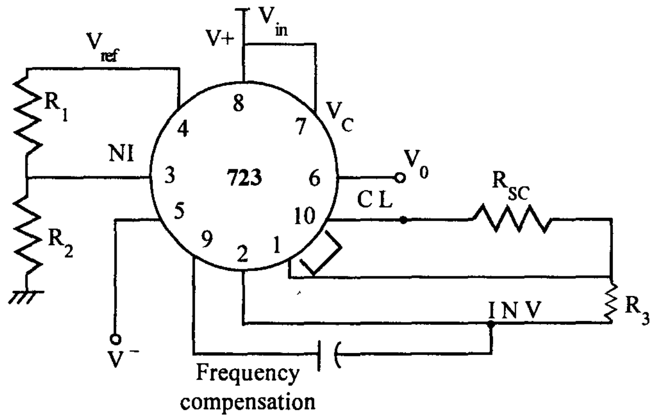


Fig. 8.1 IC 723 Voltage Regulator

8.1.1 IC 723 Pin Configuration

The pin configuration of the 723 I.C. voltage regulator is shown in Fig. 8.3

Pin 1: Current sense. The drop across R_{SC} connected between this pin and pin 10 acts as V_{BE} of the current limit transistor.

Pin 2 : Inv. input. It is the inverting input terminal of the error amplifier of the I.C., in the schematric circuit.

Pin 3 : Non-Inv. input : It is the non-inverting terminal of the error amplifier.

Pin 4 : V_{ref} : It is the reference voltage terminal of the reference source provided in the I.C.

Pin 5 : –V : Negative Voltage is applied at this terminal.

Pin 6 : Regulated output voltage V_O is obtained at this terminal.

Pin 7 : Control Voltage Terminal.

Pin 8 : Positive Voltage is applied to this terminal.

Pin 9 : Frequency Compensating Capacitor is Connected at this pin.

Pin 10 : Short circuit current limiting resistor R_{SC} is connected between pin nos 10 and 1.

723 I.C. Voltage Regulator can give a load current of 150 mA on its own. By using external pass transistor the I_L can be enhanced to several amperes.

The internal reference voltage is approximately 7.15v. Resistors R_1 and R_2 are used to set the gain of the internal amplifier.

Resistors R_3 acts as DC bias compensation provider for R_1 and R_2.

If the output voltage desired is less than the reference voltage V_{ref}, $(R_1 - R_2)$ network acts as potential divider, and the desired V_0 ($<V_{ref}$) can be obtained.

The current limit is set by,

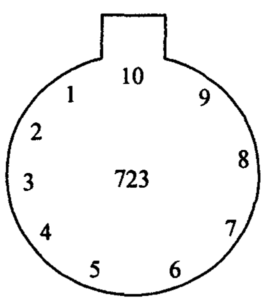
$$\text{I limit} = \frac{V_{sense}}{R_{sc}}$$

V_{sense} is approximately 0.65V at room temperature. R_{SC} resistor is placed in series with load and so the current through it is the load current.

The current limit transistor is used such that the drop across R_{SC} is applied as V_{BE} for the transistor.

The collector of the current limit transistor is conected to the base of the output pass transistor. If the output current rises to the point where the voltage across R_{SC} exceeds 0.65V, the current limit transistor wil turn ON, so the output current is shunted away from the output pass transistor.

723 I.C. is available in (1) Metal can package and (2) Duel-in-line packages (DIP). The pin configurations are shown in Fig. 8.2 and 8.3.



Top view

1. Current sense
2. Inverting input
3. Non-Investing input
4. V_{Ref}
5. V^-
6. V_0
7. V_c = Control Voltage
8. V^+
9. Frequency Compensation
10. Current limit.

Fig. 8.2 723 IC Metal can Package

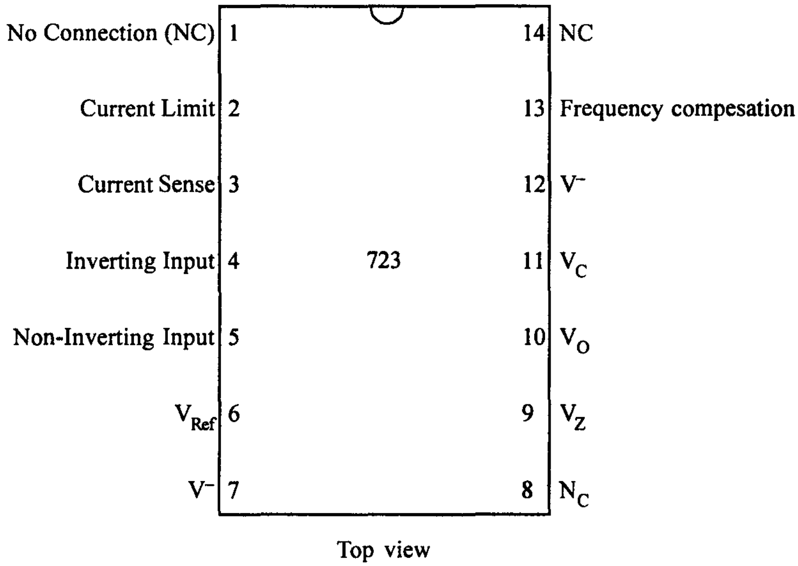


Fig. 8.3 723 IC DIP Package

The internal schemetric of the 723 IC is shown in Fig. 8.4

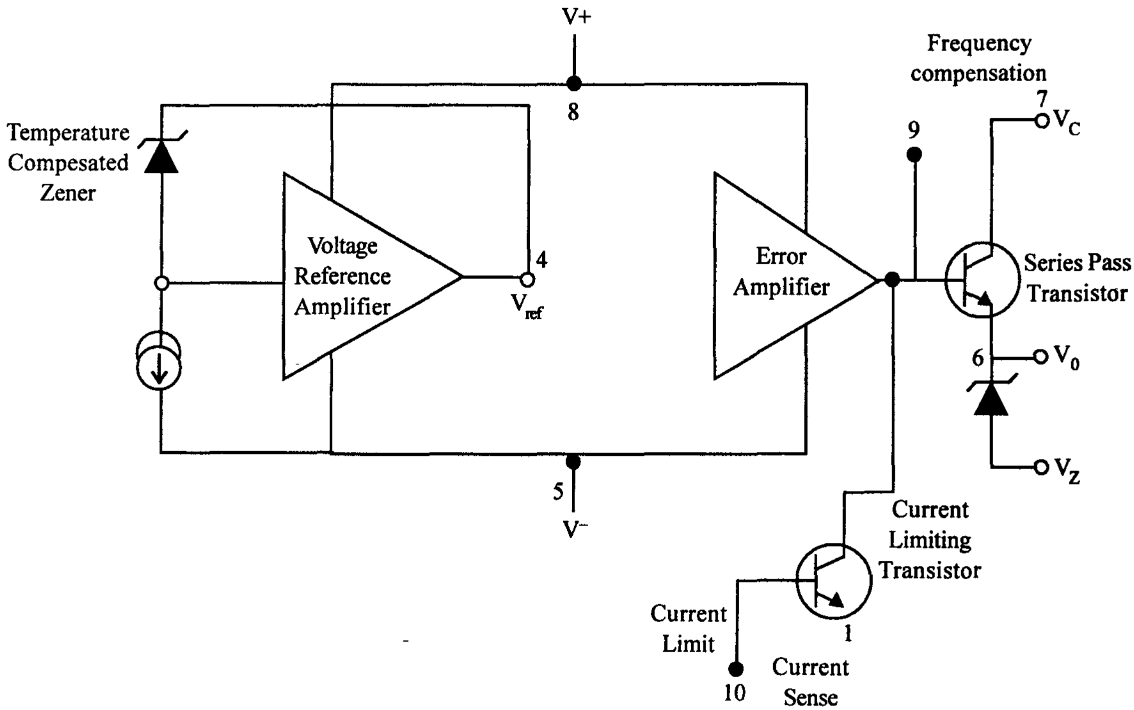


Fig. 8.4 Internal schematic of 723 voltage regulator I.C.

Problem 8.1 : Design a + 12 V voltage regulator circuit using 723 IC to give current limit of 50 mA.

$$V_0 = V_{ref} \cdot \left(\frac{R_1 + R_2}{R_2} \right)$$

Let $R_2 = 12\ K\Omega$. $V_{ref} = 7.15v$. $V_0 = 12v$, $R_1 = ?$

$$\therefore \quad R_1 = \frac{V_0}{V_{ref}} . R_2 - R_2$$

$$= \frac{12}{7.15} .12 - 12$$

$$= 20.14 - 12 = 8.14 \simeq 8K\Omega$$

$$R_3 = R_1 \| R_2 = \frac{12 \times 8}{12 + 8} = \frac{96}{20} = 4.8K\Omega$$

The circuit diagram is shown in Fig. 8.5

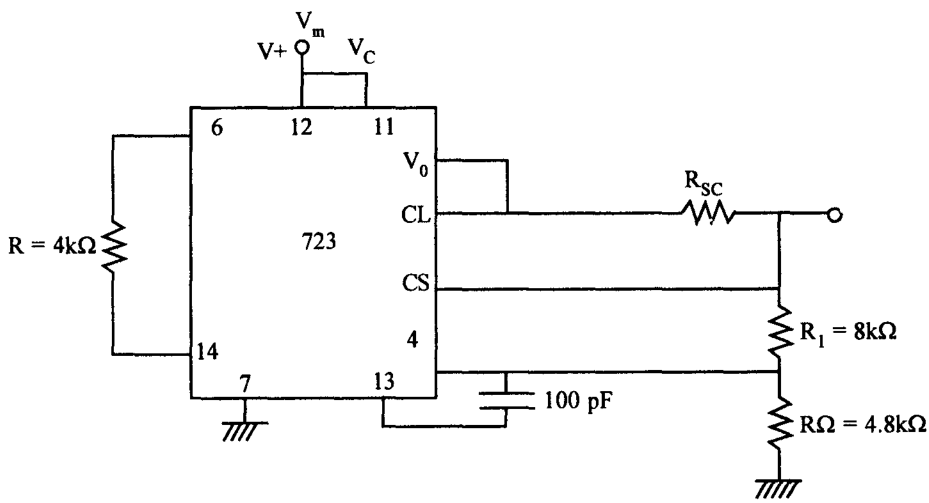


Fig. 8.5 Circuit diagram for a +12V voltage regulator circuit.

8.1.2 3 - Pin Voltage Regulator ICs

7800 I.C series is of 3- pin positive voltage regulator ICs 7900 IC series is of 3 - Pin Negative Voltage regulator ICs.

3 - Terminal Voltage Regulators

7800 Series Voltages Regulators :

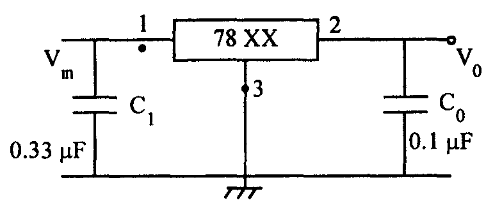


Fig. 8.6 Three terminal I.C. Regulator Circuit

These are 3 terminal, positive voltage regulators. V_0 is positive. General circuit is :

XX : indicates the numbers that will follow like 00, 01, 02 etc.,

These are available in *T0 - 3 type* Metal package.

Pin 1 : Input

2 : Output — Pins 1 and 2 can be

Case : Ground — known from the base diagram

T0 220 type Plastic package

Pin 1 Input

2 Ground

3 Output

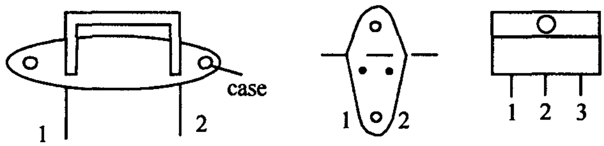


Fig. 8.7 Pin diagram

Device type	Output voltage V_0	Maximum input voltage (V)
7805	5.0	
7806	6.0	
7808	8.0	35V
78012	12.0	
7815	15.0	
7818	18.0	
7824	24.0	40V

7805 can be used as a 0.5 A current source. The current supplied to the load is,

$$I_L = \frac{V_R}{R} + I_Q$$

I_Q = Quiescent current, I_L = Load current = 4.3 mA for 7805

7800 series positive voltage regulator ICs.

IC No.	V_0
7802	+ 2 V
7805	+ 5 V
7808	+ 8 V
7818	+ 18 V
7824	+ 24 V

7900 series is negative voltage regulator ICs.

IC No.	V_0	Max V_i
7902	– 2V	
7905	– 5	
7906	– 6	– 35
7908	– 8	
7918	– 18	
7924	– 24	– 40

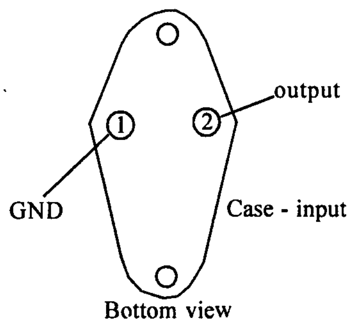


Fig. 8.8 Pin configuration base diagram

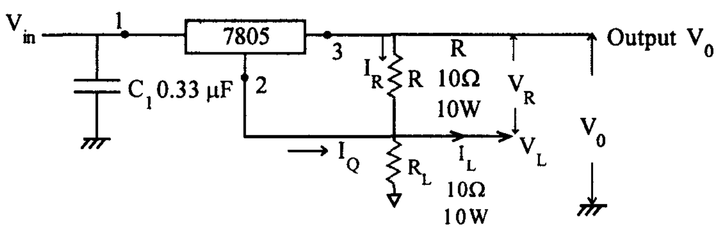


Fig. 8.9 IC 7805 Voltage Regulator

$$V_0 = V_R + V_L$$
$$V_0 = I_L R_L$$
$$R_L = 10\ \Omega \text{ (Ohms)}$$
$$\therefore \quad V_L = 5\text{ V}; \qquad I_L = 0.5\text{ A}$$
$$\therefore \quad V_0 = V_R + V_L$$
$$= 5\text{V} + 5\text{V} \qquad = 10\text{V}$$

The voltage drop across 7805 is 2V

$\therefore$ The minimum input voltage required is $V_{in} = V_0$ + Dropout voltage

$$V_{in} = 12\ V$$

So a current source circuit using a voltage regulator can be designed for a desired value of I_L, by choosing an appropriate value of R.

Example : 8.2

Using 7805C, voltage regulator, design a current source that will deliver 0.25 A current to the 48Ω 10W load.

Neglecting $\quad I_Q,\ I_L = \frac{V_R}{R} + I_Q$

$$R \simeq \frac{V_R}{I_L} \approx \frac{5V}{0.25A} = 20\ \Omega$$

$$V_0 = V_R + V_L$$

$$= 5V + (48\ \Omega)\ (0.25) = 17V$$

$$V_{in} = V_0 + \text{drop across } I_C$$

$$V_{in} = 17 + 2 = \mathbf{19V\ Ans.}$$

8.2 Current Limiting

This means short circuit protection i.e. Even if the output terminals of the voltage regulator are shorted, the current should be limited and should not exceed a particular value. This can be done in two ways.

1. Simple limiting circuit
2. Foldback limiting circuit

8.2.1 Simple Limiting Circuit

As the drop across R_3, $V_{C2\ B2}$ increases, $V_{B2\ E2}$ decreases.

$\therefore$ Q_2 goes off.

R_4 is called current sensing resistor.

If $I_L < 600$ mA, voltage drop across R_4 is < 0.6V $\quad (\because R_4 = 1\ \Omega,\ 1 \times 600\ \text{mA} = 0.6\ \text{V})$. The drop across R_4 is V_{BE} for transistor Q_3.

$\therefore$ Q_3 is cut off. So the regulator circuit works as a normal circuit, without any limiting provision. When I_L is between 600 and 700 mA, the voltage across R_4 is between 0.6 V and 0.7 V. Therefore Q_3 will turn on. So the collector current of Q_3 will flow through R_3. So the base voltage V_{BE} *to* Q_2 *will decrease.* Therefore output voltage V_0 will decrease and hence load current will decrease.

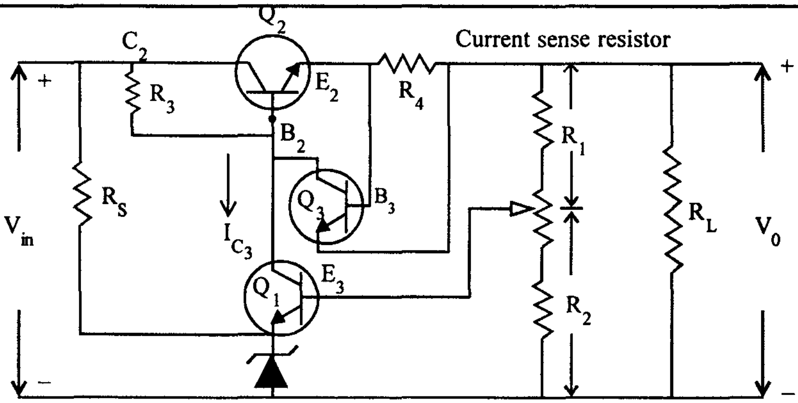


Fig. 8.10 Current limiting circuit.

If, I_S = Short circuit current when output terminals are shorted

Voltage across R_4 is $V_{BE} = I_S \cdot R_4$

$\therefore \qquad I_S = V_{BE} / R_4$

By choosing the value of R_4, we can change the level of current limiting.

The *disadvantage* with this circuit is power dissipation across transistor Q_2 will be very large.

8.2.2 Fold Back Limiting

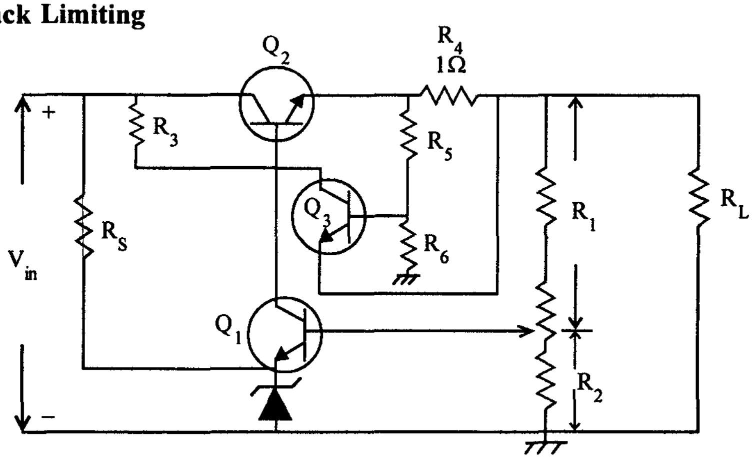


Fig. 8.11 Foldback limiting circuit.

As I_B of a transistor decreases, I_C decreases. Therefore I_0 also decreases, instead of fully being cut off. This is the principle of foldback limiting.

Using this circuit, we can reduce the power dissipation in the pass transistor. The load current flows through R_4 producing a voltage drop $\simeq I_L \cdot R_4$. So the voltage fed to the potential divider circuit R_5 and R_6 is, $I_L \cdot R_4 + V_0$. This voltage controls Q_3. The feedback fraction is,

$$K \simeq \frac{R_6}{R_5 + R_6}$$

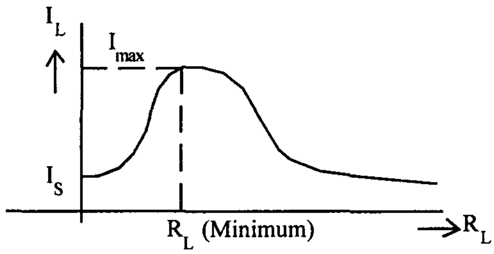


Fig. 8.12 I - R_L Characteristic

The maximum load current will be higher than short circuit current.

8.3 Specifications of Voltage Regulator Circuits

1. Regulation %
2. Input Z
3. Output Z
4. Ripple rejection
5. Current rating
6. Voltage rating

8.4 DC To DC Converter

These are used when large DC voltage is required from small DC voltage i.e. If DC 5V is available, we can make it 15V. The DC 5V is used to drive an oscillator circuit. The AC output is amplified with transformer. Then it is converted to DC, to get large DC output voltage.

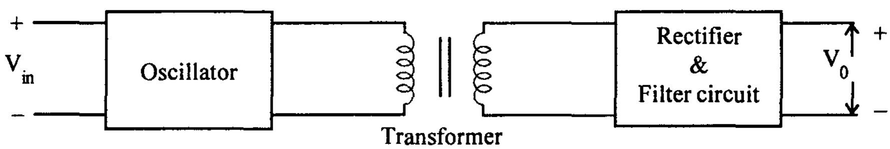


Fig. 8.13 DC to DC Converter

8.5 Switching Regulators

In the series regulators, the excess voltage is dropped across the series pass element. So power dissipation is more. In order to reduce this, switching regulators are used. Here a switch connects the input to the regulator intermittently, so that average current is passed to the load. When the switch is closed, energy is stored in an inductor. This energy is transferred to the load. When the load voltage decreases, this is sensed by the comparator and when the energy in the storage element is dissipated, the switch is closed by the comparator and input is connected to the regulator circuit. So the storage device gets charged again.

Switch is a transistor which is turned ON and OFF by the voltage of the threshold detector.

When switch is open, Diode D conducts. The energy stored in 'L' forward biases the diode. This maintain current flow through. When 'S' is closed, Diode D is Reverse Biased. Capacitor C charges. It supplies energy to the load. When V_0 decreases, detector changes state, and closes the switch.

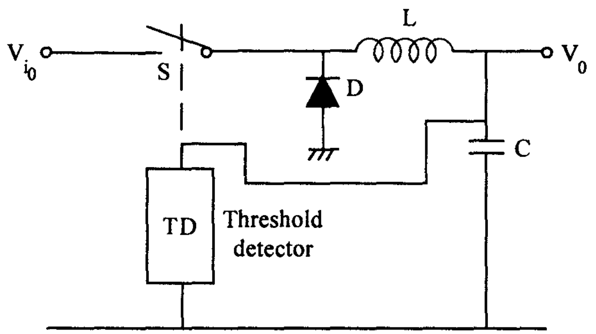


Fig. 8.14 Regulator switch.

Switching Regulators

Voltage Regulators

Dissipative	Non Dissipative
ex : Series - voltage regulator.	*ex :* Switching regulator.
Shunt - voltage regulator.	

Dissipative - Excess voltage when V_i, increases is dissipated across a series pass element. Efficiency (η) is less.

Non-dissipative - Switching type. Input is not permanently connected. (Efficiency) η is more.

Block Schematic of Switching Regulator

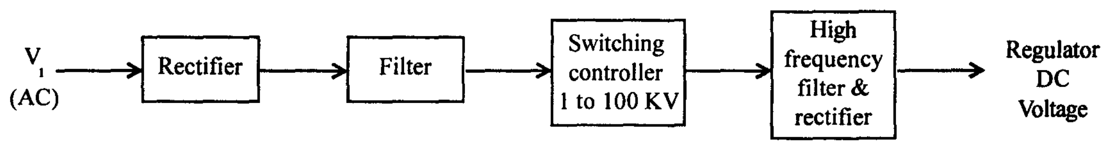


Fig. 8.15 Switching Regulator

The voltage regulating transistor is operated in cut off or saturation. So current flowing through this is small. Hence power dissipation in the circuit is less. Efficiency η is more.

The chopped AC voltage is filtered by high frequency filter and rectified to get DC.

Switching regulator is (advantages) :

1. Lighter
2. Smaller
3. More efficient than a series-pass type.

8.5.1 Step - Down (Buck) Switching Regulator

Control voltage (to turn ON/OFF the transistor Q_1)

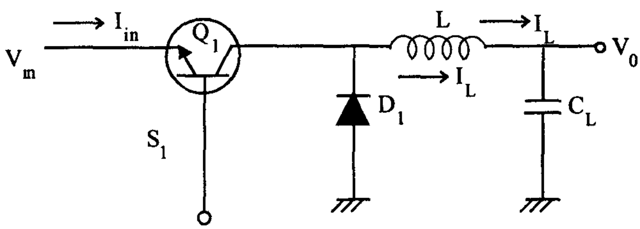


Fig. 8.16 Bucking type regulator

$$V_0 = \frac{t_{ON}}{T} V_{in}$$

t_{ON} = Time period for which Q_1 is ON

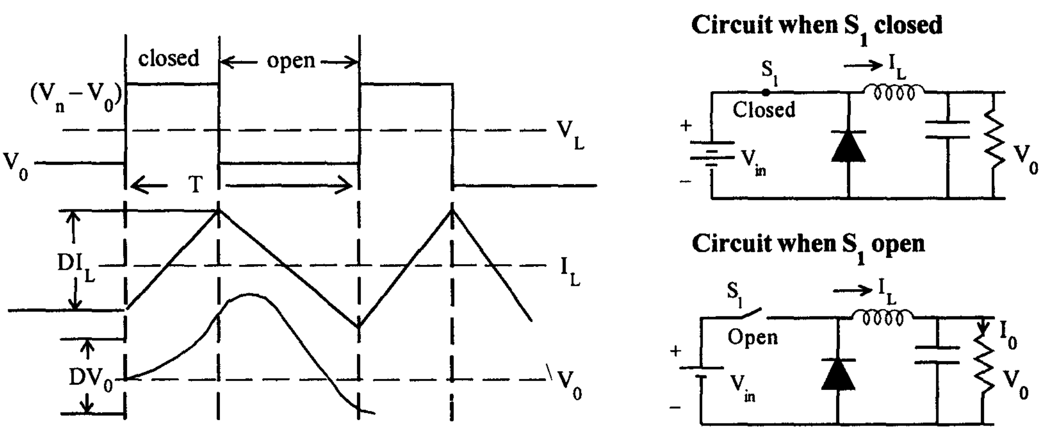


Fig. 8.17 Circuits and waveforms

T = Total time period Q_1 of input square wave.

D = Duty cycle

$$= \frac{t_{ON}}{t_{ON} + t_{off}} = \frac{t_{ON}}{\text{Total time}} = \frac{t_{ON}}{T}$$

D_1 is catch diode in the circuit

It provides continuous path for the inductor current when Q_1 turns off. When S_1 is closed, inductor current I_L passes from the input voltage V_{in} to the load ($V_{in} - V_0$) appears across inductor. So I_L increases.

When S_1 is open, *stored energy* in the inductor forces I_L to continue to pass in the load, and return through diode. The inductor voltage is now reversed and is $\simeq V_0$. So I_L decrease.

8.6 Voltage Multipliers

8.6.1 Half Wave Voltage Doubler Circuit

During the first negative half cycle, D_1 is forward biased. So C_1 will get charged, to the peak of the input voltage V_P, with the polarity as shown in Fig. 8.18. During the positive half cycle, D_2 is forward biased. Therefore, C_2 will get charged to $V_P + V_P = 2V_P$. Capacitor C_1 will charge C_2 to V_P and from the source, through D_2, C_2 will get charged to a further value of V_P. So after several cycles, the voltage across C_2 will be $2V_P$. Here R_L should be large. Other wise, C_2 will be discharging quickly and the voltage may not be maintained constant at $2V_P$. This is half wave doubler circuit, since the output capacitor C_2 is charged only once during the full cycle.

Such circuits are used where large output voltage is required. Large V_0 can be obtained by using a bigger transformer. But its cost will be more.

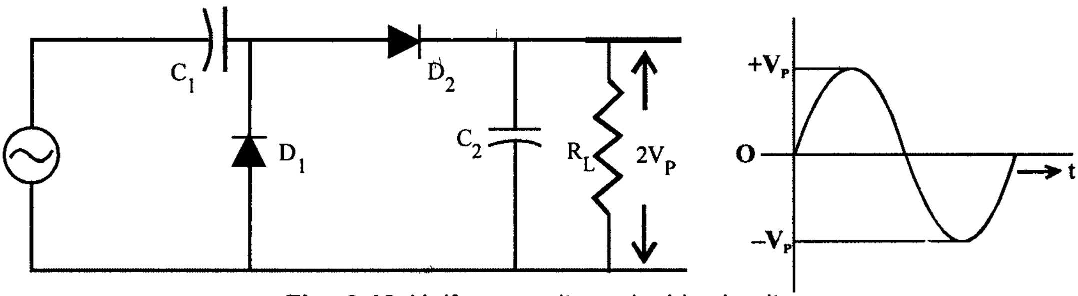


Fig. 8.18 Half wave voltage double circuit

8.6.2 Full Wave Voltage Regulator

During the positive half cycle, D_1 is forward biased C_1 gets charged to V_P. During the negative half cycle, D_2 is forward biased. So C_2 gets charged to V_P. In the steady state, the voltage across R_L in 2 V_P. Here center tapped transformer is not used. It is called full wave, since one of the diodes is conducting in each half cycle (similar to a full wave rectifier circuit). But the problem is, since no centre tapped transformer is used, there is no common ground between the input and the output. If the bottom of R_L is grounded, input is floating. This is not desirable in electronic circuits. So in FWR circuits, centre tapped transformer is used. In this circuit ripple will be less as shown in Fig. 8.19.

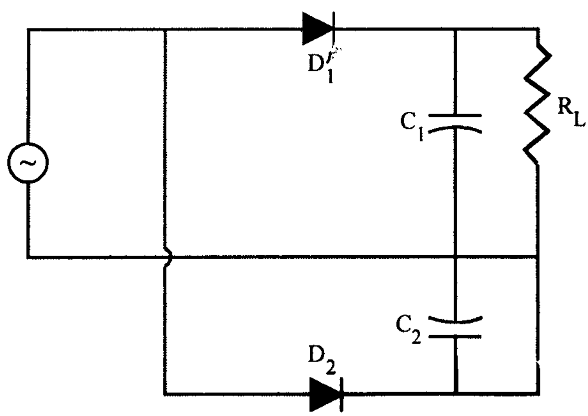


Fig. 8.19 Voltage Doubler Circuit

8.6.3 Voltage Tripler

The circuit is as shown in Fig. 8.20. Working is similar to the previous circuit.

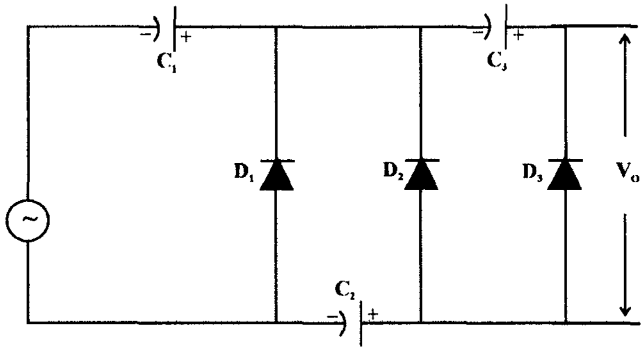


Fig. 8.20 Voltage tripler circuit

8.6.4 Voltage Quadrupler

The circuit is shown in Fig. 8.21. Is there any limit to the number of sections that can be added to get large voltage ? Theoretically it is possible. But the ripple voltage will get worse as additional sections are added. (A diode is being put across or in series. So ripple will increase). So these circuits are used only where very high voltage doubling is to be done. The input voltage itself will be higher.

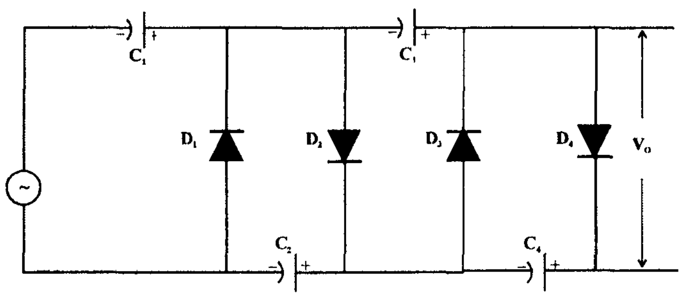


Fig. 8.21 Voltage quadrupler circuit

8.6.5 Peak To Peak Detector

The circuit is as shown in Fig. 8.22.

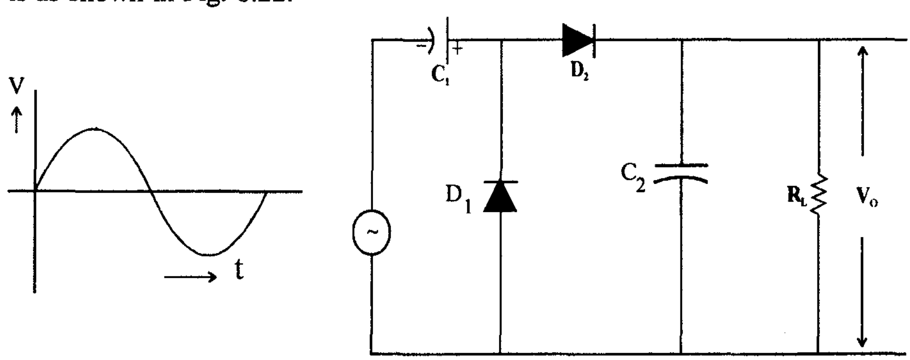


Fig. 8.22 Peak to peak detector

The input sine wave is positively clamped. $C_1 - D_1$ is a positive clamped circuit. $D_2 - C_2$ is a peak detector circuit. When D_1 is forward biased, C_1 gets charged to V_P. When D_2 is forward biased, C_2 gets charged to $2V_P$. So output will measure peak to peak value. R_L should be large. If the input is not symmetrical, positive peak and negative peak are not same, the average value or rms value measured will not be correct. In such cases, first peak to peak detector is connected and then the DC meter or AC meter are connected. In certain measurements, peak to peak value is to be determined. In such cases this type of circuits are used.

Ripple Factors

γ Ripple Factor for 'C' filter $= \dfrac{1}{4\sqrt{3}\,f\,CR_L}$

γ Ripple Factor for 'L' filter $= \dfrac{R_L}{4\sqrt{3}\omega L}$

γ Ripple factor L_C filter $= \dfrac{\sqrt{2}}{3} \times \dfrac{1}{2\omega C} \times \dfrac{1}{2\omega L}$

Critical Inductance $L_C \geq \dfrac{R_L}{3\omega}$

Bleeder Resistor RB $= \dfrac{3X_L}{2}$

γ fro π - filter $\dfrac{\sqrt{2}X_C}{R_L}\left(\dfrac{X_{C1}}{X_{L1}}\right)$

Example : 8.3

Design a power supply using a π - filter to give DC output of 25V at 100 mA with a ripple factor not to exceed 0.01 %. Design of the circuit means, we have to determine L, C, diodes and transformers.

Solution :

Design of the circuit means, we have to determine L, C, diodes and transformer

$$R_L' = \frac{V_{DC}}{I_{DC}} = \frac{25V}{100mA} = 250\ \Omega$$

Ripple factor $\gamma = \sqrt{2}\,.\,\dfrac{X_c}{R_L}\,.\,\dfrac{X_{C_1}}{X_{L_1}}$

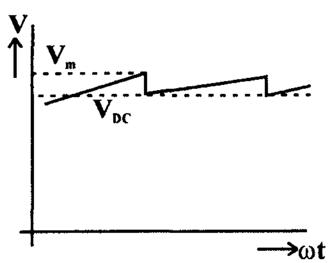


Fig. 8.23 Ripple voltage waveform

X_C can be chosen to be $= X_{c1}$.

$$\therefore \qquad \gamma = \sqrt{2} \cdot \frac{X_C{}^2}{R_L . X_{L_1}}$$

This gives a relation between C and L.

$$C^2 L = y$$

There is no unique solution to this.

Assume a reasonable value of L which is commercially available and determine the corresponding value of capacitor. Suppose L is chosen as 20 H at 100 mA with a DC Resistance of 370 Ω (of Inductor).

$$\therefore \qquad C^2 = \frac{y}{L} \text{ or } C = \sqrt{\frac{y}{L}}$$

$$V_{DC} = V_m - \frac{V_\gamma}{2}$$

$$V\gamma = \frac{I_{DC}}{2fc}$$

Now the transformer voltage ratings are to be chosen.

The voltage drop across the choke = choke resistance × I_{DC}.

$$= 375 \times 100 \times 10^{-3} = 37.5\text{V}.$$

$$V_{DC} = 25 \text{ V}.$$

Therefore, voltage across the first capacitor C in the π - filter is

$$V_c = 25 + 37.5 = 62.5 \text{ V}.$$

The peak transformer voltage, to centre tap is

$$V_m = (V_C) + \frac{V_V}{2} \text{ (for C filter)}$$

$$V\gamma = \frac{I_{DC}}{2fc}$$

$$\therefore \qquad V_m = 62.5\text{v} + \frac{0.1}{2 \times 50 \times c}$$

$$\text{Vrms} = \frac{V_m}{\sqrt{2}} . \cong 60\text{v}$$

Therefore, a transformer with 60 – 0 – 60V is chosen. The ratings of the diode should be, current of 125 mA, and voltage = PIV = $2V_m$ = 2 × 84.6 V = 169.2 V.

Example : 8.4

A full wave rectifier with LC filter is to supply 250 v at 100 m.a. DC. Determine the ratings of the needed diodes and transformer, the value of the bleeder resistor and the ripple, if R_C of the choke = 400Ω. L = 10 H and C = 20 μF.

Solution :

$$R_L = \frac{V_{DC}}{I_{DC}}$$

$$R_L = \frac{250\,V}{0.1} = 2{,}500\Omega.$$

For the choke input resistor,

$$E_{DC} = \frac{2E_m}{\pi\left(1+\frac{R_C}{R}\right)}$$

and $$I_{rms} \cong I_{DC}.$$

$$E_m = \frac{\pi E_{DC}}{2}\left(1+\frac{R_C}{R_L}\right)$$

$$= \frac{\pi \times 250}{2}\left(1+\frac{400}{2500}\right) = 455V$$

$$E_{rms} = \frac{455}{\sqrt{2}} = 322\ V$$

Therefore, the transformer should supply 322V rms on each side of the centre tap. This includes no allowance for transformer impedance, so that the transformer should be rated at about 340 volts 100 mA, DC.

The Bleeder Resistance

$$R_B = \frac{3X_L}{2}$$

$$L = 10H$$

$$I_B = \frac{2E_m}{3\pi\omega L} = \frac{2 \times 455}{3\pi \times 377 \times 10} = 0.256\ A$$

Ripple factor $$\gamma = \frac{0.47}{4\omega^2 LC - 1} = \frac{0.47}{4 \times 377^2 \times 20 \times 10^{-6}}$$

The current ratings of each diode = 0.00413, should be 50 mA.

Example : 8.5

Design a full wave rectifier to supply current in the range 50 mA to 100 mA at 300V with a ripple less than 5V, using,

1. L section filter 2. π - section filter 3. C filter

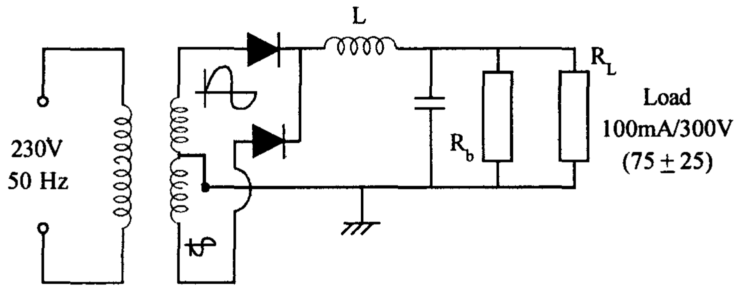


Fig. 8.24 Circuit for Ex. 8.5

$$I_{L(min)} = 50 \text{ mA and}$$

$$I_{L(min)} = 100 \text{ mA}$$

$$r = \frac{5V}{300} = \frac{I_{ac}}{I_{dc}}$$

$$= \frac{V_{ac}}{V_{dc}} = \frac{1.1931}{LC}$$

$\therefore$ LC = 35.8, where L is in henrys and C in μF.

$L_{critical} \geq \frac{R_L}{2\omega_S}$ ($\therefore$ minimum value of I_L = 50 mA, we use R_B for 50 mA only)

$$R_B \cong \frac{V}{I_L} = \frac{300}{50 \times 10^{-3}} = 6K\Omega$$

$$\therefore \qquad L_{critical} = \frac{6K}{3 \times 2\pi \times 50} = 6.4H$$

Taking 25% more, because for formula of $L_{critical}$, we use fundamental frequency value,

$$L_{critical} = 8 \text{ H}$$

$\therefore$ We choose L = 10 H/100 mA

$\therefore$ C = 3.58 μF from the equation,

We choose 4μF/450 V

Now, $V_{dc} = \frac{2V_m}{\pi} - I_{dc} R$, where

$$R_x = R_{diodes} + R_{secondary} + R_{choko}$$
$$= 0 + 250 + 200 = 450\Omega$$

$$V_m = \frac{\pi}{2}[V_{dc} + I_{dc}R]$$

$$= \frac{\pi}{2}[300 + 0.1 \times 450]$$

$$= \frac{345\pi}{2} = 541.92 \text{ V}$$

$$V_{rms} = \frac{542}{\sqrt{2}} = 383 \text{ V}$$

$\therefore$ Transformer used will have 390 – 0 – 390 V/100 mA.

Diode current rating

$= I_L/2 = 100/2 = 50 + 15\%$ due to variation

$= 57.5$ mA.

Nearest current rating of diode = 100 mA

$\therefore$ 100 mA current rating diodes are used.

$PIV = 2V_m$ $\therefore PIV$ rating

$= 1084 + 15\%$

$= 1400$ V

Using π - section filter :

R_B is not required because there is already a path for discharge current, of capacitor, as 50 mA is minimum I_L.

$$r^2 = \frac{1}{30}$$

also $$r^2 = \frac{5700}{C_1C_2LR_L} = \frac{1}{30}$$

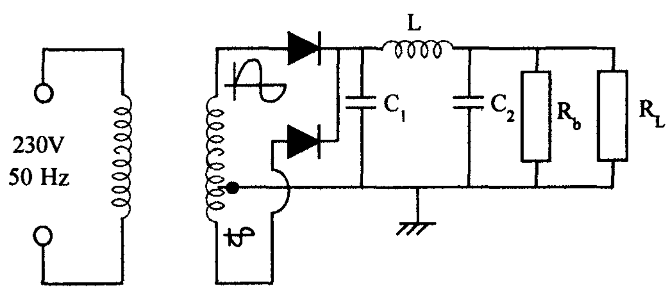


Fig. 8.25 With π - section filter

Let $C_1 = C_2 = C$

$$\therefore \qquad r^2 = \frac{5700}{C^2 L R_L}$$

$$R_{L(min)} = \frac{300V}{100mA} = 3K\Omega,\ R_{L(max)} = \frac{300}{50} = 6\ K\Omega$$

Calculating for worst case of supply, or the lowest value of $R_L = 3\ K\Omega$, we have

$$\frac{5700}{C^2 L \times 3K} = \frac{1}{30} \qquad \therefore\ LC^2 = 57.02$$

Select **L = 1H/100 mA** $\quad \therefore\ C^2 = 57.02$

$$\therefore\ C = 7.55\ \mu F$$

Using **C = 8μF/400 V.**

$$V_m = V_{dc} + I_{dc} \left\{\frac{\pi}{2\omega_S C} + R_L\right\}$$

$$= 300 + 100 \left\{\frac{\pi}{2 \times 2 \times \pi \times 50 \times 8 \times 10^{-6}} + 450\right\} \times 10^{-3}$$

$$= 300 + 107.5$$

$$= 407.5 = 408V$$

$$V_{rms} = \frac{V_m}{\sqrt{2}} = \frac{408}{\sqrt{2}} = 288.5\ V$$

Select transformer as 290 – 0 – 290 V/100 mA

Voltage across C_2 = 300 V. If load goes down to 50 mA the voltage increase, is giv

$$V_{in} = V_{dc} + I_{dc} \left(\frac{\pi}{2\omega_S C} + R\right)$$

$\therefore \qquad V_{dc} + 354,\ I_{dc} = 50$

$\therefore$ voltage across C_2 in worst case is 354 V.

We select 354 + 15% = 408 V

$\therefore$ Using C_2 of 8 μF/450,

Voltage across $\quad C_1 = 408 + I_L\ (200\ \Omega)$, where $I_L = 50$ mA.

$$= 408 + 10 = 418\ V$$

$$V_m = \frac{\pi}{2}\ \{300 + 0.1 \times R_s\}\ \frac{\pi}{2}\ \{300 + 0.1 \times 450\}$$

$$= 541.9 = 542\ V$$

$$V_m = \frac{\pi}{2}\ \{V_{dc} + (0.05 \times 450)\}$$

$$V_{dc} = 336\ V/50\ mA + 15\%\ \text{increase}$$

$$= 386\ V$$

$\therefore \qquad$ 450 V is needed for C

Example : 8.6

Design a FW circuit using bridge rectifier configuration with two sections of L-C filter; to give ripple better than 0.02 %. Inductances available are 100 mH, 100 mA, (r = 100 ohms).

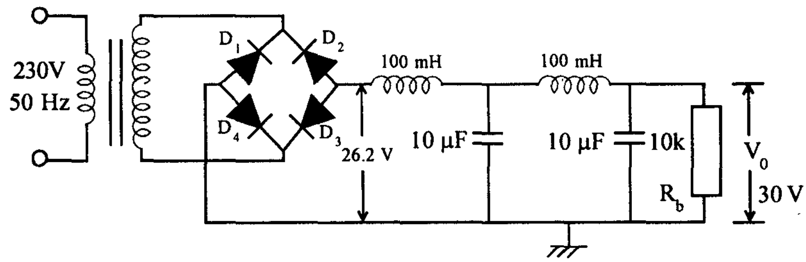


Fig. 8.26 Circuit for Ex. 8.6

For two L - section filter,

ripple factor $$r = \frac{\sqrt{2}}{3} \cdot \frac{1}{(4\omega^2 LC)^2}$$

(i) L critical $\geq \dfrac{R_L}{3\omega}$

Since $\quad$ L = 100 mH, f = 50 Hz.

$R = 3\,\omega\,L$

$\leq\ 9424.78\ \Omega$

(ii) The actual value of R_L will depend on the load itself, and the output voltage required, which is not specified. We assume that R_L = 1 K, and the current required is 30 mA.

(iii) Find the value of C.

Since $$r = \frac{\sqrt{2}}{3} \cdot \frac{1}{(4\omega^2 LC)^2}$$

$$\frac{0.02}{100} = \frac{\sqrt{2}}{3} \cdot \frac{1}{\left(4 \times \omega^2 \times .1 \times C^2\right)}$$

For f = 50 Hz, L = .1H

We get, C = 10 uF with a voltage rating depending upon the peak - voltage of the secondary.

(iv) Transformer :

The dc resistance of the choke given is 100 ohms.

$\therefore$ voltage across the capacitor of the first section

$= 30\text{ V} + I_{dc} \cdot R_{\text{choke}}$

$= 30\text{ V} + 30\text{ mA} \times 100\text{ ohms}$

$= 33\text{ V}$

$\therefore$ The voltage at the input of the first section

$= 33\text{ V} + 40\text{ mA} \times 100\text{ ohms}$

$= 33\text{ V} + 4\text{ V} = 37\text{ V}.$

Note that the current flowing is assumed as 40 mA instead of 30 mA to take care of the capacitor current as well. (Value assumed is slightly on the higher side)

Both capacitors C_1 and C_2 can have voltage ratings of 50 V.

Transformer secondary voltage (RMS)

$$= 37/\sqrt{2} = 26.2 \text{ V}$$

Allowing for two diode voltage drops, we may require the voltage on the secondary

$$= 26.2 + 2 \times .6 = 27.4 \text{ V.}$$

This does not take into account the drop due to transformer secondary, which will depend on the rating of the transformer, but we may assume the same to be about 3 ohms for the transformer (which will create a drop of 3 ohms × 40 mA = 120 mV).

We may select transformer with turns ratio 220 : 27.5, 100 mA.

(v) The diodes should have rating of minimum 100 mA, PIV = 60 V.

(vi) The bleeder resistance should be around 10 times R_L, giving

$$R_B = 10 \text{ K}$$

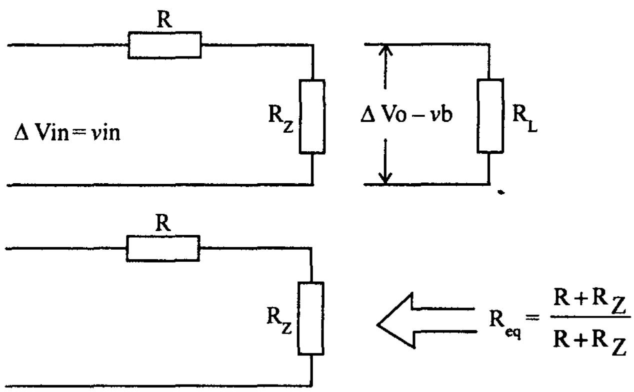


Fig. 8.27 For Ex. 8.6

Example : 8.7

Design a zener voltage regulator to supply a load current which varies between 10mA and 25mA at 10V. Input supply voltage available is 20 V $\pm$ 10 %.

Solution :

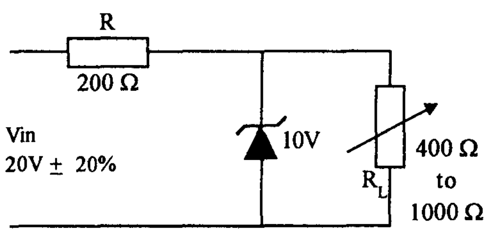


Fig. 8.28 Circuit for Ex. 8.7

1. Since the output voltage = 10V, the load resistance, R_L, varies from

$$V_z/10mA = 1000 \text{ Ohms to}$$
$$V_z/25mA = 400 \text{ Ohms.}$$

2. Given that $V_{in(max)} = 20 + 0.01 \times 20 = 22$ V

$$V_{in(min)} = 20 - 0.01 \times 20 = 18 \text{ V}$$

Hence, $$R = \frac{V_{in(min)} - V_Z}{I_{L(max)} + I_{z(min)}}$$

$$= (22 - 18) \text{ V}/ (25 - 5) \text{ mA}$$
$$= 200 \text{ Ohms,}$$

assuming $I_{z(min)}$ to be slightly greater than I_{zk}.

3. The zener is called upon to absorb maximum current when V_{in} is maximum and at the same time I_L is minimum.

$$I_{z\,(max)} + I_{L(min)} = (V_{in(max)}) / R.$$

Hence, $$I_{z\,(max)} = \{(24 - 10)/200\} - 10mA$$
$$= 60 \text{ mA.}$$

The zener diode rating, therefore, should be

$$P_{z\,(max)} = V_z \times I_{z\,(max)} = 10 \text{ V} \times 60mA$$
$$= 600 \text{ mW.}$$

We will have to select a zener diode of rating of 1 W. This higher rating will also take care of the inadvertent opening of the load resistance circuit, in which case, the zener current will be equal to 70mA and the zener power dissipation will be equal to

$$P_z = 10V \times 70mA = 700 \text{ mW.}$$

In the above analysis, the dynamic resistance of the zener diode is assumed to be equal to zero (and, therefore, S = 0, as per equation). However, even if we assume R_z = 4 Ohms (say), then V_z will change with the change in the zener current. The zener current changes from its minimum value of 5mA to a maximum of 60mA. Therefore, v_0 = the change in the output voltage,

$$= (60 - 5)mA \times 5 \text{ Ohms} = 0.275V.$$

Consequently, the stabilisation factor will be

$$S = R_z/ (R_z + R) = 5/205 = 0.024.$$

Example : 8.8

Design a power supply to give 1A at 12 volts.

Solution :

We shall assume an input voltage supply to be available having twice the output voltage, i.e., say, 25V, with a variation of $\pm$ 20%.

The input voltage available, therefore, will be between 20 and 30 volts.

The circuit, rearranged, will be as shown the Fig. 8.29.

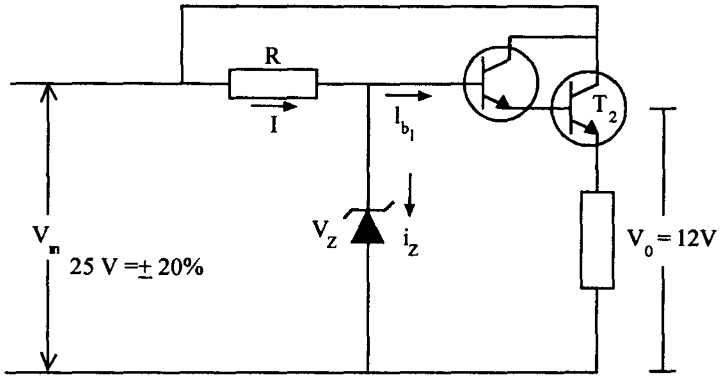


Fig. 8.29 Circuit for Problem 8.8

1. **Let us select, first, the transistor T_2.**

V_{CE} across the transistor

$= V_{in(max)} - V_0$

$= 30 - 12 = 18V.$

Hence, the power dissipation for the transistor $T_2 = 18V \times I_L$

$18 V \times 1A = 18W.$

We will select ECN 149 as our transistor T_2. This transistor has a gain of about 35.

2. **The base current of the transistor T_2 for full variation of the load current, is = 1A/35 = about 30 mA.**

The transistor T_1 will be supplying the base current of transistor T_2. With the voltage across the transistor T_1 being practically the same as that of the transistor T_2, the power dissipation of the transistor T_1 will be, neglecting V_{BE2},

$= (30 - 12)\ V \times 30mA$

$= 18 \times 30mA$

$= 540mW.$

We will, therefore have to select a transistor which has this capacity, and also can withstand 30mA. We select transistor SL 100 for the purpose, which has a current gain of about 50.

This gives $I_{B1} = 30mA/50 = 0.6mA.$

3. **This I_{B1} is the load current for the zener diode, which is operated slightly above I_{zk} of, say, 5mA.**

$$R = \frac{V_{in(min)} - V_Z}{I_{z(min)} + I_{b(max)}} = \frac{20 - 12}{5.6mA}$$

$= 8V/5.6mA = 1.42$ K - Ohms.

We shall select a standard value of the resistance for R.

The values available near about the calculated values are, 1.2 k and 1.5 k. We shall select 1.2 k, the lower of the two normally available values, as the higher value will force reduction in $I_{z\,(min)}$.

We will recalculate the current $I_{z\,(min)}$, using this value of the resistance.

$$I_{z(min)} + I_{B(max)} \doteq 8V/1.2k$$
$$= 6.67\ mA.$$

Hence, $I_{z(min)} = 6.67mA - 0.6mA = 6.07mA.$

The power rating of the resistor

$$= I_z^2 \times R$$
$$= (6.07mA)^2 \times 1.2k$$
$$= 45mW.$$

We shall select a resistance of 1/4 W capacity.

4. To obtain 12 volts at the output, the zener diode will have to be of

$$12V + V_{BE1} + V_{BE2} = 12 + 0.6 + 0.6 = 13.2\ V.$$

We can adopt the strategy shown in Fig. 8.36.

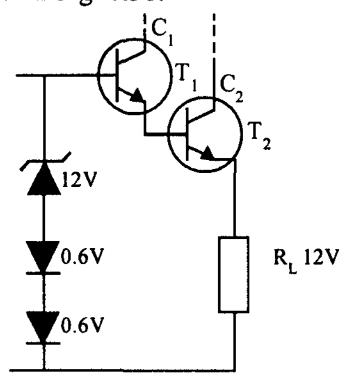


Fig. 8.30 For Ex. 8.8

5. The power rating of the zener diode :

$$V_z = 12\ V$$

and $I_z = 6.07\ mA$

Hence, Pz = 12V × 6.07mA = 80mW. We can select 150m zener. In case there is an open - circuit on the load side, the zener current will increase to 6.07 mA + 0.6 mA = 6.67 mA, needing the zener diode to dissipate power,

$$= 12V \times 6.67\ mA = 80mW.$$

The zener diode selected can take care of the increased dissipation.

We need the following components to build the circuit.

Transistor T_1 = SL 100 or ECN 100.

Transistor T_2 = ECN 149

Example : 8.9

Design 5V, 500ma regulated voltage supply. AC supply is obtained from a 230V : 20V transformer.

Solution :

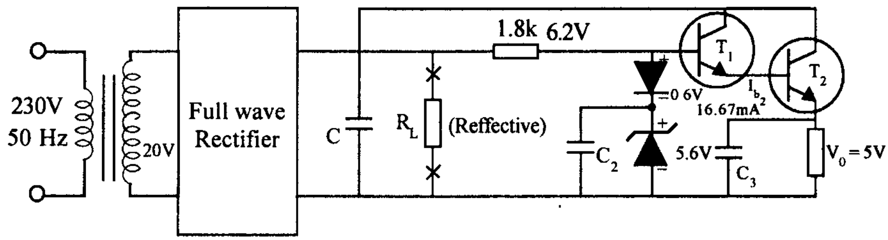


Fig. 8.31 Circuit for Ex. 8.9

1. **The transformer secondary will have a voltage**

$$= 20 \text{ V rms}$$
$$= 20 \times \sqrt{2}$$
$$= 28.28 \text{ V peak.}$$

2. **We will select a capacitor filter even though the load current is large.**

$$V_{av} = V_P = 28.28\text{V}$$

Actually this voltage should be equal to

$$V_{dc} = \frac{(4fR_LC)}{(4fR_LC+1)} \times V_P$$

$$= \frac{(4 \times 50 \times R_L \times C)}{(4 \times 50 \times R_L \times C + 1)} \times 28.28 \qquad \text{.....(i)}$$

Since this supply will have to feed, $I_L + I_r$

= 1A, neglecting I_r,

giving $I_{dc} = 0.5$A, and hence $R_L = V_{dc}/I_{dc}$ =

= 5V/0.5A = 10 – Ohms

Substituting this value in the equation (i) we have,

$$V_{dc} = \frac{(2000 \times 5000 \times 10^{-6})}{(2000 \times 5000 \times 10^{-6} + 1)} \times 28.28\text{V}.$$

$$= \frac{10}{11} \times 28.28 = 25.78\text{V}.$$

3. **Selection of the transistors.**

Let us select the transistor T_2.

Vce for the transistor $T_2 = V_{in} - V_0$

$= 25.78 - 5 = 20.78$V

Since the load current will have to flow through the transistor T_2, the power dissipation capacity of transistor T_2 is

$$V_{ce} \times I_L$$
$$= 20.78V \times 500mA$$
$$= 10.39W.$$

We select a transistor ECN 149 having Ic(max) = 4A., and maximum power dissipation of 30w. This transistor has minimum h_{FE} of 30.

This will mean that a base current of 500mA/30 = 16.67mA will be required to support the required load current through the transistor.

Selection of the transistor T_1 :

The above base current will be supplied by the transistor T_1. This is the collector current of the transistor T_1. Voltage across this transistor is practically the same as that of the transistor T_2. Actually it is

$$= V_{in} \times V_o - V_{BE2}$$
$$= 25.78 - 5.0 - 0.6$$
$$= 19.58 \text{ V}$$

Since the current flowing through the transistor is = 16.67mA, the power dissipation for this transistor

$$= 19.58 \times 16.67mA$$
$$= 326 \text{ mW.}$$

This will necessitate the use of a transistor like SL 100 as transistor T_1. This transistor has $hFE_{(min)} = 50$.

4. Selection of zener diode

Transistor T_2 base is at a voltage

$$= V_o + V_{be}$$
$$= 5 + 0.6 = 5.6V.$$

Likewise, T_1 base should have a voltage of $V_{b_2} + 0.6 = 6.2V$.

We can take a zener of 6.2V, or a zener of 5.6V in series with a diode to provide about 6.2V at the base of T_1.

Resistance $\quad R = (V_{dc} - V_{b1})\ R = \dfrac{(V_{dc} - V_{b1})}{I}$

$$= \frac{25.78 - 6.2}{I} = \frac{19.58}{I}$$

where current $\quad I = I_{b_1} + \cancel{Iz}$

$$I_{b_1} = I_L/(h_{FE1} \times h_{FE2})$$
$$= 500mA/(50 \times 30) = 0.33 \text{ mA.}$$

Hence, R = 19.58V/0.33mA = 1.958 KΩ.

We can select a nominal value of 1.8 KΩ.

Recalculating the value of the current passing through it,

We have $I = I_z$ (approx.) = (25.78 – 6.2)V/1.8k = 10.88mA.

The value of the resistance R is thus 1.8k, and since the current passing through it = 10.88mA, the power rating of R

$$= (10.88)^2 \times 1.8\text{k -Ohms} = 213\text{mW}.$$

We can select R as 1.8k -Ohms/ 1/2W rating.

Example : 8.10

Determine the component values for a voltage regulator circuit for 12V at 100mA. The circuit is to operate from a dc supply of 20 $\pm$ 5V.

Solution :

1. Selection of transistor T_1

Voltage across the transistor

$$= V_{in(max)} - V_o$$
$$= 25 - 12 = 13.$$

The current through the transistor $T_1 = I_{L(max)}$ = 100mA.

Therefore, the power dissipation required of the transistor

$$= 13\text{V} \times 10\text{mA} = 1.3 \text{ Watts}$$

We select a transistor ECN100 for the purpose, which has

$$P_{d(max)} = 5\text{W at } 25\ ^{o}\text{C}.$$
$$I_{c(max)} = 0.7\text{A at } 25\ ^{o}\text{C}.$$
$$h_{FE(min)} = 50.$$
$$h_{fe(typ)} = 90.$$
$$h_{ie} = 1.3\text{k}$$

The base current required

$$I_{B1(max)} = I_{C(max)}/h_{fe(min)}$$
$$= 100\text{mA}/50$$
$$= 2\text{mA}.$$

2. Selection of the zener diode

Since the output voltage V_0 = 12 Volts, we may select a zener diode of a voltage of 6.8V (between about 50 and 80% of the output voltage). The power dissipation capacity of the zener should be around 150mW giving,

$$R_z = \frac{V_0 - V_Z}{I_Z}$$

$$= \frac{12 - 6.8}{5mA} = 1.04\ \text{K}\Omega.$$

We select Rz = the nearest available standard value of 1k -Ohms, which should have power dissipation capability of $(5.2\text{mA})^2 \times 1\text{k} = 27\text{mW}$.

We, therefore select R_z = 1k and of 1/8 watts.

3. Selection of transistor T_2

As a thumb - rule, we select I_{C2} as about, between 10 and 50% of the I_{B1} depending upon the load current. Let I_{C2} = 1ma., in our case. The voltage across the transistor T_2

$$= V_{CE2} = V_o + V_{BE1} - V_z$$
$$= 12 + 0.6 - 6.8$$
$$= 5.8\text{V}.$$

This means that the $P_{d(\max)}$ of the transistor T_2

$$= 5.8\text{V} \times 1\text{mA} = 5.8 \text{ mW}.$$

We select BC147B, which has,

$$P_{d(\max)} = 0.25\text{W}$$
$$I_{c(\max)} = 0.1\text{A}.$$
$$h_{FE(\min)} = 200.$$
$$h_{fe(\min)} = 240.$$
$$h_{ie} = 4.5\text{K}\Omega$$

4. Selection of the resistance R_3

The maximum base current required for the transistor for the maximum collector current of 100mA (which in reality is the load current and hence the emitter current). We neglect the additional current required for zener and the base current, making load current = emitter current = collector current.

$$I_{C1}/h_{FE(\min)} = 100\text{mA}/50 = 2.0\text{mA}.$$

Also the value of I_{C2} = 1mA, giving the value of the current passing through the resistance $R_3 = I$

$$= I_{C2} + I_{B1}$$
$$= 2\text{mA} + 1\text{mA} = 3\text{mA}.$$

Minimum voltage across the resistance R_3

$$= V_{in(\min)} - V_o + V_{BE1}$$
$$= 15 - 12 + 0.6$$
$$= 3.6 \text{ Volts}.$$

Hence, $R_3 = 3.6\text{V} / 3\text{mA}$

$$= 1.2 \text{ K}\Omega$$

Selecting the nearest standard value available, R_3 = 470 Ohms, which will make the total current to 13.6 / 470 = 2.9mA.

Since I_{B1} is dependant upon the load current and hence, will be 2mA, I_{C2} will reduce from 1.0mA to 0.9mA.

The power dissipation will be $(3mA)^2 \times 4.7K = 39mW$.

We select R_3 = 4.7K and of 1/8W.

Likewise, when the input voltage is maximum, i.e., 25V, the current through the resistance R_3 will be equal to

$$(25 - 12 - 0.6)V / 470 \text{ Ohms} = 12.4/470$$

$$= \text{about } 27mA$$

Since this current of 27mA (less 2mA for the I_{B1}) becomes the collector current for the transistor T_2, we have $P_{d(max)}$ for transistor T_2 = 5.8V × 25mA = 145mW.

This is well within the capacity of the transistor selected, which otherwise would have to be changed to a higher power transistor.

5. Selection of R_a and R_b

Voltage $\quad V_{B2} = V_z + V_{BE2}$

$$= 6.8 + 0.6$$

$$= 7.4 \text{ Volts.}$$

Therefore, $\quad \dfrac{R_b}{R_a} = \dfrac{V_{B2}}{V_0} = \dfrac{7.4}{12} = 0.62,$

provided that the value of Rb finally selected be sufficiently small as compared to $\{h_{IE2} + R_z(1 + h_{FE2})\}$, so that the shunting effect of the transistor T_2 is negligible, i.e., it is assumed that the current drawn by the R_a and R_b combination is very large as compared to the base current of transistor T_2, which is

$$= I_{b2} = 0.9 / 200 = 4.5\ \mu A.$$

If we select, I_r as about 1mA, (alternatively, I_r should be chosen, as a thumb - rule, to be about 10% of the load current), we get,

$$R_a + R_b = V_0 / I_r$$

$$= 12/1mA$$

$$= 12k \text{ - Ohms.}$$

and $\quad \dfrac{R_b}{R_a} = 0.62$

Hence, $\quad R_a + 0.62\,R_a = 12K$ - Ohms.

$$R_a = 7.4k \text{ -Ohms}$$

and $R_b = 4.6k$

We can select $R_a = 6.8k$, $R_b = 3.9k$ and connect a potentiometer of 1k in-between giving total resistance $= 6.8 + 3.9k + 1K$

$= 11.7 K$

Adjusting the potentiometer, we will be able to adjust the output voltage finely to the required value.

The power dissipation for

$$R_a = (I_r)^2 \times 6.8 K$$

$$= 6.8mW.$$

Similarly, for R_b, Power dissipation = 4.7 mW.

and for the potentiometer

$$= 1mW$$

We may select all these components of 1/8 W capacity.

Let us calculate S_v and R_o for the above example.

We have,

$$S_v = \frac{R_P + h_{ie2} + R_i(1 + h_{fe2})}{R_3 \times h_{fe2} \times k}$$

where $R_P = 7.4$ K in parallel with 4.6 K

$= 2.8$ K.

R_2 may be assumed as about 10 ohms, at the point of operation, and

$$K = (R_b) / (R_a + R_b)$$

$$= 0.383$$

Hence,

$$S_v = \frac{2.8K + 4.5K + 10(1 + 240)/1000}{0.47 \times 240 \times 0.383}$$

$$= 0.225$$

We have,

$$R_0 = 5.1 \text{ ohms}.$$

These are fairly large values.

We can improve upon these, if so desired, by using a darlington pair of transistors in place of a single transistor T_1. This will help in increasing the value of the resistance R_3 since the base current requirements will be reduced, resulting in smaller value of the voltage - stabilisation ratio. Since the total gain increases the product of the individual current - gains of the transistors used in the pair, the value of the R_0 will reduce to a considerable extent.

8.7 Uninterrupted Power Supply (UPS)

When the egular AC main line supply fails, the uninterrupted power supply (UPS) unit delivers the poweRto the load. The load may be computer or any electronic system etc. The desirable characteristics of UPS are :

1. Voltage and frequency of the UPS output must be stable with close tolerances.
2. The output must be of high quality with minimum distortion
3. Must deliver output power without interruption

UPS units are used in :

1. Computer centres/computer systems
2. Instrumentation systems
3. Process-control units
4. Communication systems etc.

The block schematic of UPS system is shown in Fig. 8.32.

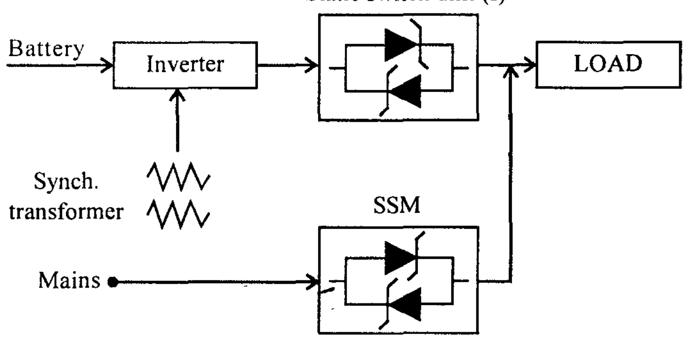


Fig. 8.32 Block schematic of UPS.

UPS consists of a bank of batteries, depending on the output voltage required, static switch unit for the invertor (SSI), and static switch unit for the mains (SSM), and synchronizing transformer.

8.7.1 Operation

When the mains are functioning, the battery unit is charged. The inverter suppliers power to the load, through SSI. After the battery unit is fully charged, it floats. When the mains fail, the Invertor supplies the load current without interruption, by converting the DC voltage it obtains from the battery into a pulse width modulated AC voltage. It is filtered converted to Sinusoidal wave form and supplied to load. The inverter output is always synchronized with the mains. If the inverter fails, power is supplied to load by the mains, by automatically switching on the SSM and switching off the SSI.

8.7.2 Inverter Circuit

The circuit diagram is shown in Fig. 8.33. It is a pulse width modulated Inverter circuit. The circuit functions on complementary communication method. Whenever SCR T_4 is turned ON T_1 gets turned OFF automatically. Similarly when T_2 is tuned ON, T_3 immediately gets turned OFF and Vice-versa. Output is taken between the terminal C and D. The output waveform is shown in Fig. 8.34.

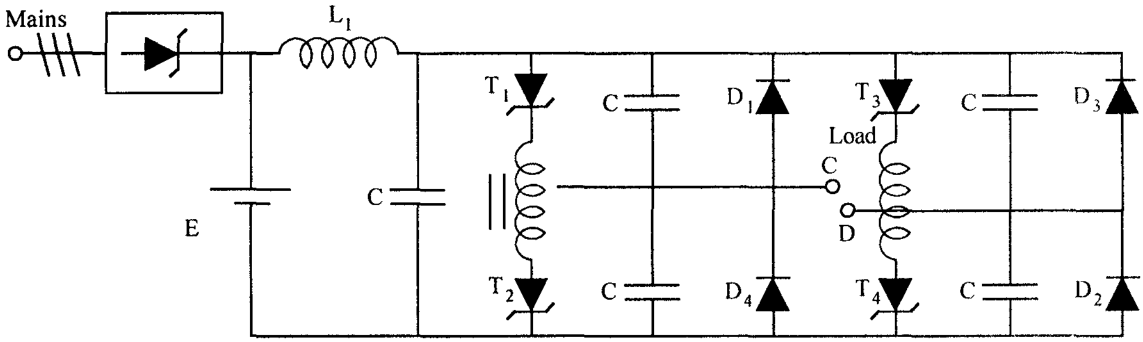


Fig. 8.33 Pulse width modulated inverter circuit.

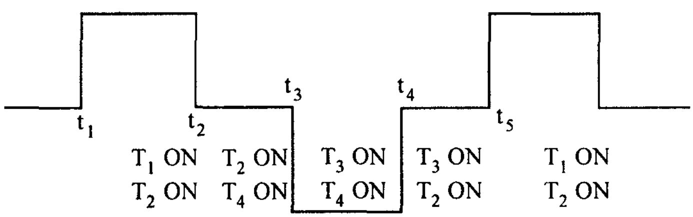


Fig. 8.34 Waveforms.

During the period $t_1 - t_2$: SCRs T_1 and T_2 are conducting. Output voltage follows input DC voltage.

At t_2 : SCR T_4 gets triggered, turning OFF T_1. Load current passes through T_2 and T_4 and Diodes D_2 and D_4 depending on the direction of load current.

At t_3 : SCR T_3 gets triggered and turns OFF T_2. So point D becomes +ve with respect to C.

At t_4 : SCR T_1 gets triggered. The output voltage becomes zero and remains at this level til t_5. This cycle repeats.

Control Circuit : The block schematic of control circuit is shown in Fig. 8.35 The function of the circuit is to obtain proper firing signals.

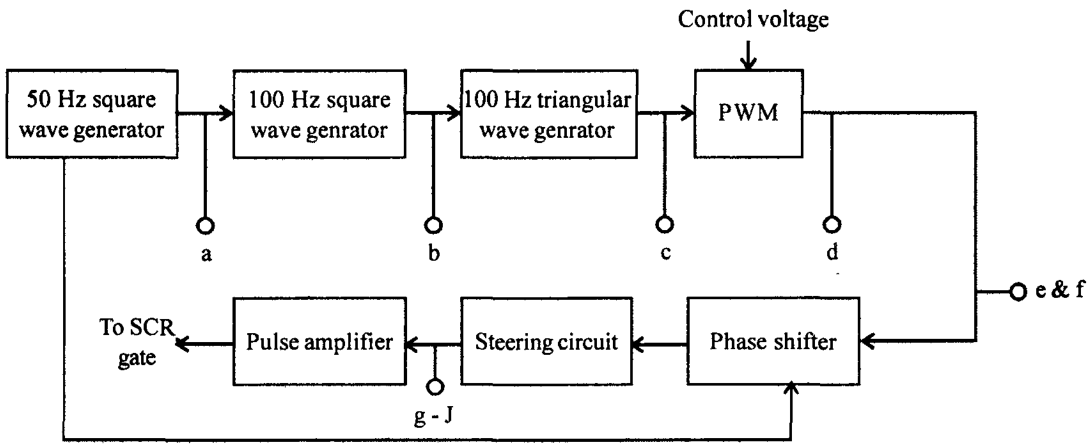


Fig. 8.35 Block diagram of control circuit.

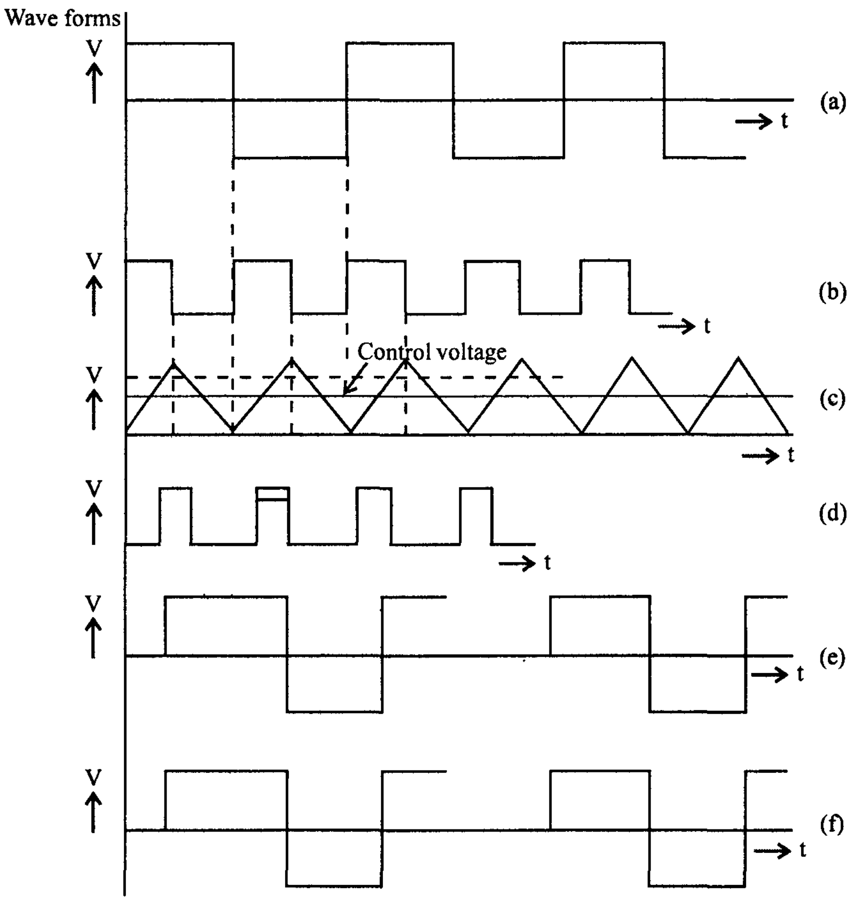


Fig. 8.36 Output waveform of Dual d Flip Flop (e) & (f).

The 50 Hzs square wave output is converted into a 100 Hzs signal, which in turn is converted into a 100 Hzs triangular waveform. This waveform output is compared with the control voltage, by the comparator to produce a 100 Hzs output pulse. The width of this pulse is proportional to the input control voltage. This pulse and the basic 50 Hz square wave are fed as clock input and D input to the Dual D Flop-Flop. The phase shift between the two output wave forms of the Dual D Flop Flop can be varied by the control voltage. These outputs are amplified and applied through the steering circuit, as gating signals to the SCR.

8.7.3 Filter Circuit

The output of the inverter circuit is not a pure sinusoidal wave.

The former equation governing the output is,

$$e_n = \frac{4V}{n\pi} \text{ Sin } \left(\frac{n\beta}{2}\right) . \text{ Cos } n(\omega t)$$

where n = 1, 3, 5...

β = Pulse width in radians

V = Amplitude

ω = Mains radian frequency

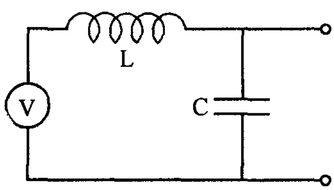
The filter circuits are chosen such that the distortion of the sine wave is within the permissable limits. The desirable characteristics of filter circuits are :

(i) High output impedance (ii) Low output impedance

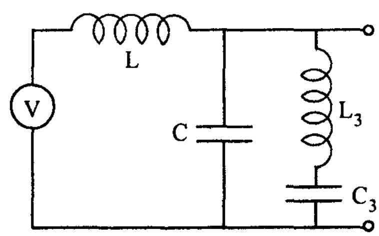
(iii) High efficiency (iv) Low cast

The different types of filter circuits used are :

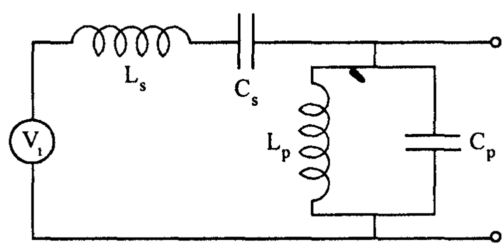
1. Low pass filter 2. Low- Pass-with third harmonic filter 3. Series-parallel filter.



(a) Low - Pass filter



(b) Low - Pass with third harmonic filter



(c) Series-parallel filter

Fig. 8.37 Different types of filter circuits

8.7.4 Static Switch

The block diagrams used for static switch for inverter (SSI) and static switch for mains (SSM) are shown in Fig. 8.38.

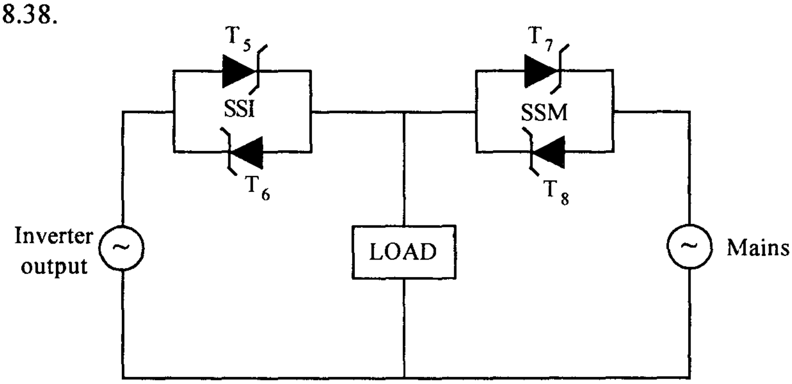


Fig. 8.38 Static switch-circuit diagram.

When the inverter circuit is functioning it supplies the load current through T_5 and T_6. During positive half cycle, T_5 conducts and during negative half cycle T_6 conducts. The gating is done by direct current controlled through an opto coupler. If the inverter circuit stops functioning, it is sensed and SCRs T_7 and T_8 are fired immediately. Then the transmission of gate signals to T_5 and T_6 stops. When the Inverter becomes active, the load is again, transferred to it by switching ON T_5 and T_6, and switching OFF T_7 and T_8.

8.8 Switched Mode Power Supplies (SMPS)

For applications in computer systems, Instrumentation panels, electronic control circuits, a DC source of about 50W and above is usually required. The required features of such a DC power supply are

1. Less ripple
2. Controlled output voltage.

For such requirements, Switching Mode Power Suppliers (SMPS) are used. The schematic of such a SMPS in shown in Fig. 8.39.

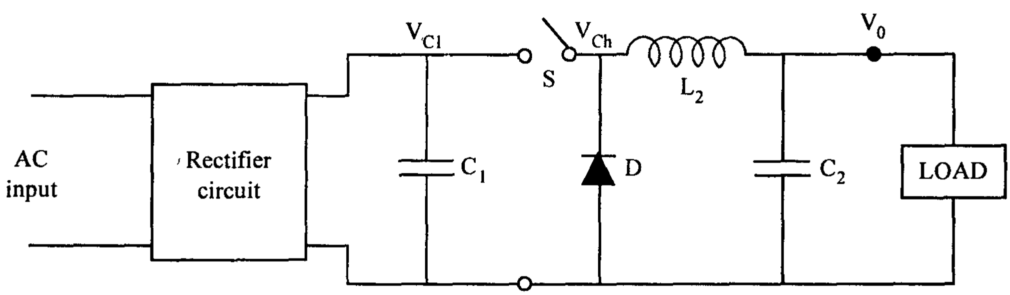


Fig. 8.39 Schematic of Switched Mode Power Supply (SMPS).

The A.C mains input is converted to DC by a rectifier circuit. The output is not controlled at this stage. The capacitor C_1 smoothens the output of rectifier circuit, and reduces ripple voltage. The output voltage of capacitor C_1 V_{C1} is as shown in Fig. 8.40.

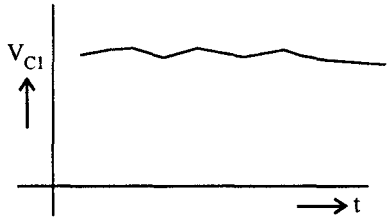


Fig. 8.40 Output wave form of C_1.

An electronic switch like a power transistor or MOSFET changes this output to high frequency A.C V_{ch} as shown in Fig. 8.41. This voltage is chopped between zero and maximum levels, and can be controlled by the rate of switching.

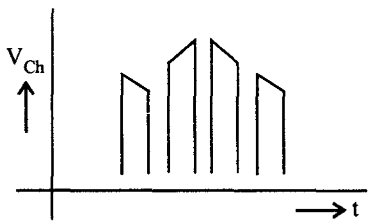


Fig. 8.41 Output waveform V_{ch} after switching.

This chopped controlled AC voltage is given as input to the LC filter network L_2 C_2. This LC filter smoothens the AC voltage to give DC output voltage with very negligible ripple, as shown in Fig. 8.42.

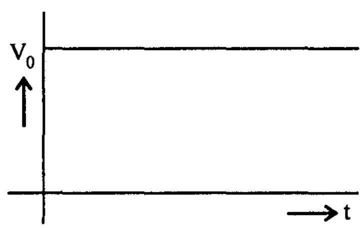


Fig. 8.42 Output voltage from the LC filter circuit.

This DC voltage is applied to the load. This is the principle of SMPS circuits.

But why to chop the output of capacitor C_1 and then again convert this chopped voltage to DC using LC filter ? The reasons are :

1. If the capacitor C_1 it self were to give DC voltage, the value of C_1 has to be very very large to reduce the value of ripple, which is not practicable. The ripple % is inversely proportional to the value of capacitor.

2. If the switching circuit is not used to chop the voltage V_{c1}, the output DC voltage V_0 cannot be controlled. The output voltage magnitude depends on the (ON/OFF) ratio of the switch.

3. The ripple frequency of the voltage after chopping is high. So the values of L_2 and C_2 can be small within the practicable limits. If the ripple frequency is high, filtering is more effective and low values of L and C can be used as indicated by the equation given below.

   The expression for the ratio of output voltage of the filter V_{OF} to its input voltage (V_{iF})

$$\frac{V_{0F}}{V_{iF}} = \frac{1}{w^2LC-1}$$

   Where 'ω' is the radial frequency of the harmonics. So higher order harmonics are attenuated more than the lower order harmonics.

   If $\omega_2 L_2 C_2 >>1$,

$$\frac{V_{0F}}{V_{iF}} = \frac{1}{\omega^2LC}$$

   or Attenuation of ripple components is inversely proportional to ω^2. i.e., the higher the switching rate, the lesser the ripple. So the electronic switching circuit is used in SMPS circuits. The Diode D in the circuit is required to provide a path for the continuous current n the inductor when the switch is open.

   The Inductor L_2 in the filter circuit offers zero resistance to DC component because $X_L = 0$ for DC and large impedance to high ripple AC components (because $X_L = j\omega L$). The capacitor C_2 gets charged to the mean value of the chopped voltage.

8.8.1 Single Transistor Switched Mode Power Supply Using Transformer

SMPS circuit is basically a DC to DC converter. For switching action, power transistor or MOSFETs can be used.

If power transistors are used as switching devices, the switching rate frequency is to be limited to 40 KHzs.

If MOSFETs are used, this frequency can be upto approximately 200 KHzs. The size of the device can also be small.

By using a transformer in the circuit, the advantages are :

1. Transformer isolation can be achieved between input and output which is essential in electronic circuits.

2. The range of output voltage levels can be changed, by having two or more secondaries for the transformer.

Such a circuit diagram is shown in Fig. 8.43.

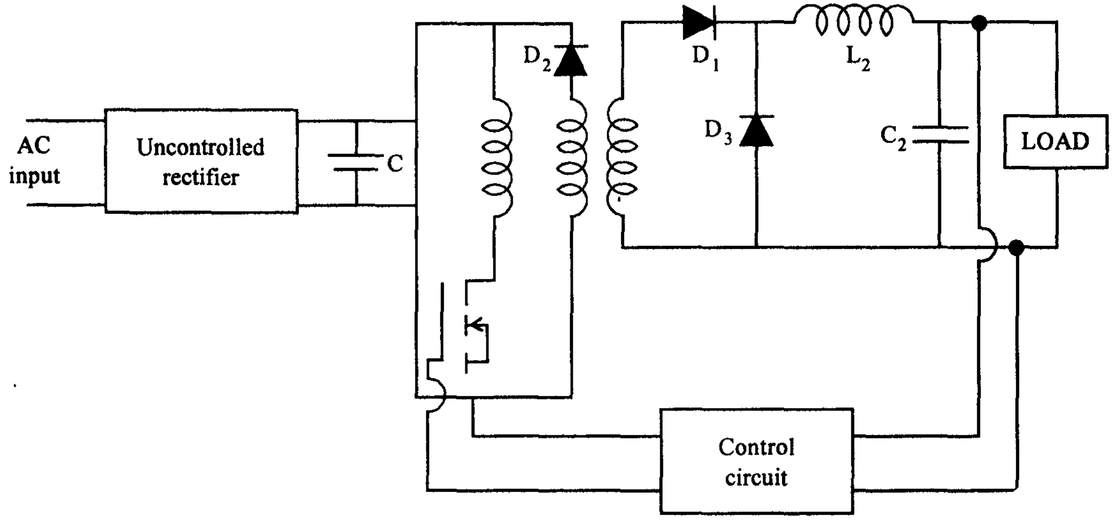


Fig. 8.43 SMPS using transformer.

The different types of circuits configurations used for SMPS are :

1. Step-Down or forward or Buck type
2. Step-Up or flyback or Boost type
3. Configuration of (1) and (2) Buck and Boost type.

The circuit for step-Down or forward SMPS is shown in Fig. 8.44.

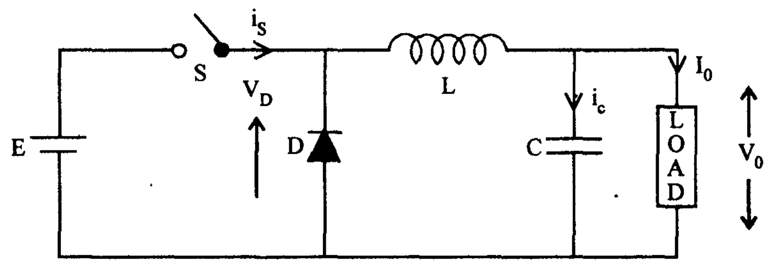


Fig. 8.44 Buck type converter.

The energy is transferred from the source to load. Th value of the load voltage is less than the source voltage. When the switch is closed, the core magnetic flux in the inductor rises. The inductor current rises at a rate such that its voltage $L\left(\frac{di}{dt}\right)$ is equal to the voltage difference $(V_p - V_o)$. When the switch is open, the source current collapses to zero. So the inductor current falls. The mean value of the output load voltage is given by the ratio of switch ON period to the total time of each cycle.

The duty cycle $S = \dfrac{t_1}{t_1 + t_2}$.

The wave forms are shown in Fig. 8.45.

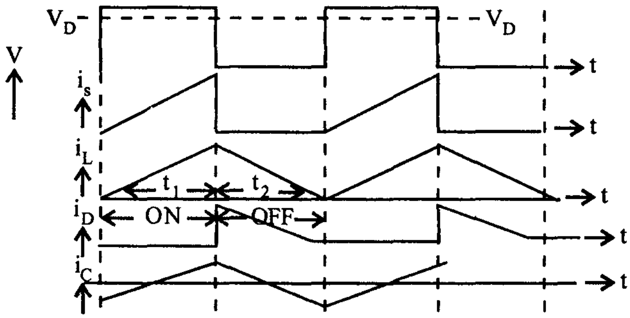


Fig. 8.45 Waveforms.

8.8.2 Boost converter

This circuit is also known as flyback or step-up converter. The circuit diagram is shown in Fig. 8.46. In this circuit, the mean value of the load voltage in greater than that of source voltage. When the switch is closed, current builds up to give stored magnetic every in the inductor. When the switch is opened, the current transferes to the capacitor and load via the diode.

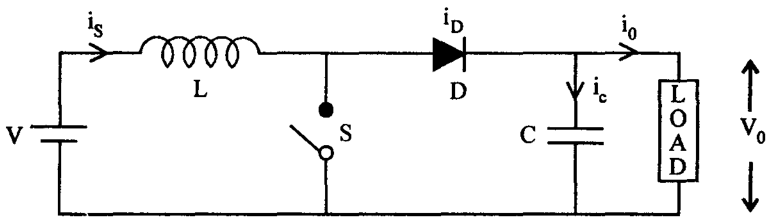


Fig. 8.46 Boost converter.

The waveforms are as shown in Fig. 8.47.

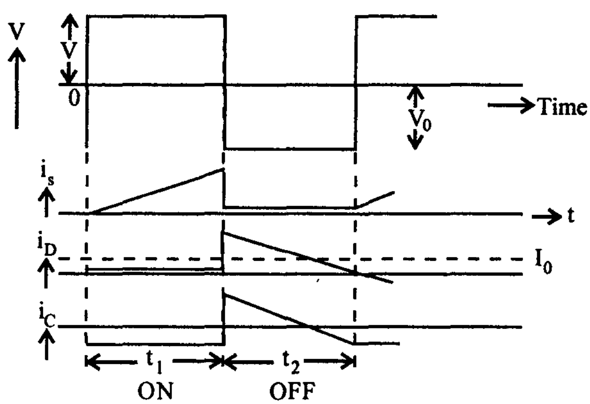


Fig. 8.47 Waveforms

Buck and Boost type is the combination of both these circuits.

Objective Type Questions

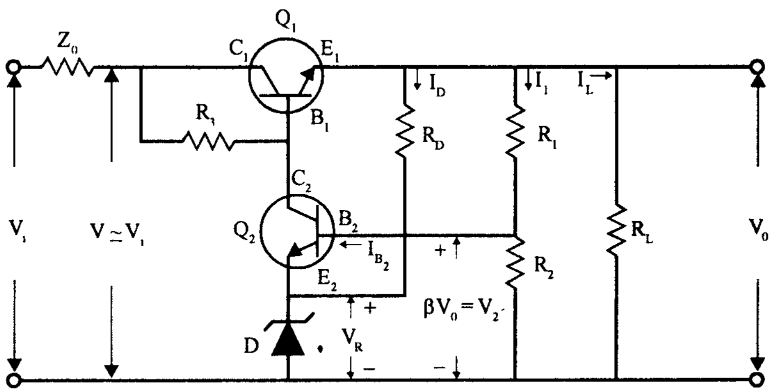
1. The IC 7908 is a ________________ Type IC. Output V_o = ________________.
2. The IC 7805 is a ________________ Type IC_1 giving out put of ________________.
3. Example of Non-dissipative type Voltage Regulator Circuit is ________________.
4. What is a regulator ?
5. What are the types of regulators ?
6. What is line regulation ?
7. What factors does the o/p voltage of a regulator depend on ?
8. What is rippe rejection ?
9. What is the drawback of Zener regulator ? How do we avoid it ?
10. Draw the circuit diagram of a series voltage regulator.
11. What is a preregulator ?
12. Why do we go for a switching regulators ?
13. Draw the circuit of a voltage multiplier of multiplication factor 'n'.

Essay Type Questions

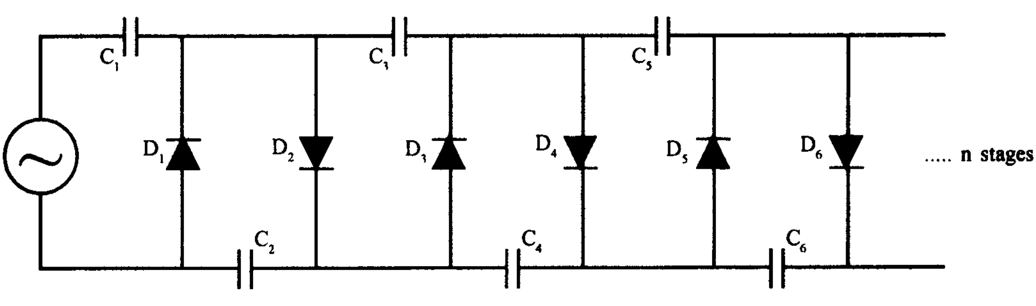
1. Give the Internal Block schematic and Pin Configuration of 723 Voltage Regulator IC.
2. Draw the circuit for 7805 Voltage Regulator IC and explain its working.

Answers of Objective Type Questions

1. Negative Voltage Regulator. I_C. $V_o = -8V$
2. Positive Voltage Regulator. I_C. $V_o = +5V$
3. Switching Voltage Regulator.
4. Regulator gives constant dc voltage irrespective of variations in the input parameters.
5. Zener regulator
   Shunt regulator
   Series regulator
   Switching regulator.
6. Ratio of change in output voltage to the change in input voltage.
7. $V_0 = f(V_i, I_L, T)$
8. It is the ratio of output ripple voltage to the input ripple voltage.
9. It is a fixed voltage regulator. So we go for series voltage regulator.
10. Circuit diagram.



11. To achieve high stability, there should be a constant current source or a high impedance before the series pass transistor this is termed as a preregulator.
12. If there are very high frequency fluctuations in the there would be more dissipation in the series pass transistor. This can be avoided using a switching regulator.
13. Circuit diagram.



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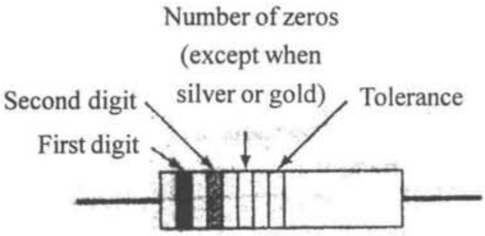
APPENDIX - 1

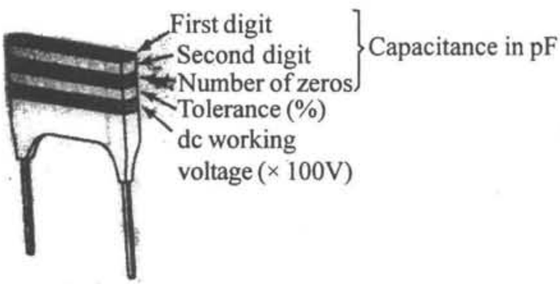
Colour Codes for Electronic Components

RESISTOR COLOUR CODE :



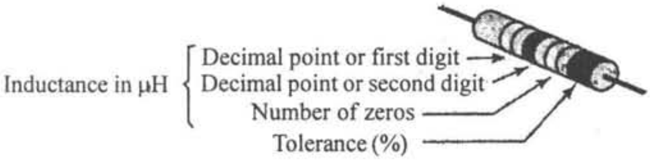
First Three Bands		Fourth Band
Black – 0	Blue – 6	Gold ± 5%
Brown – 1	Violet – 7	Silver ± 10%
Red – 2	Grey – 8	None ± 20%
Orange – 3	White – 9	
Yellow – 4	Silver 0.01	
Green – 5	Gold 0.1	

CAPACITOR COLOUR CODE :



Colour	Figure Significant	Tolerance (%)
Black	0	20
Brown	1	1
Red	2	2
Orange	3	3
Yellow	4	4
Green	5	5
Blue	6	6
Violet	7	7
Grey	8	8
White	9	9
Silver	0.01	10
Gold	0.1	5
No Band		20

INDUCTOR COLOUR CODE :



Color	Significant Figure	Tolerance (%)
Black	0	
Brown	1	
Red	2	
Orange	3	
Yellow	4	
Green	5	
Blue	6	
Violet	7	
Grey	8	
White	9	
Silver		10
Gold	Decimal point	5
No Band		20

COLOUR CODE MEMORY AID : W_G VIBGYOR BB (W_G Vibgyor BB)

Memory aid	Color	Number	
Black	Black	0	
Bruins	Brown	1	
Relish	Red	2	
Ornery	Orange	3	
Young	Yellow	4	
Greenhorns	Green	5	
Blue	Blue	6	
Violets	Violet	7	
Growing	Grey	8	
Wild	White	9	
Smell	Silver	0.01	10%
Good	Gold	0.1	5%

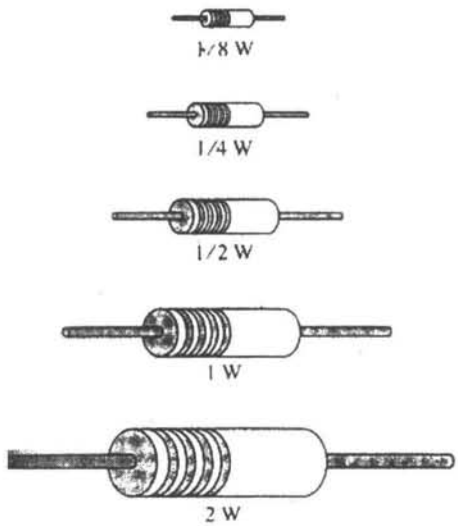


Fig. A-1.1 Relative size of carbon composition resistors with various power ratings

Specifications of Power Transistors

Device	Type	P_D(W)	I_C(A)	V_{CEO}(V)	V_{CBO}(V)	h_{FE} MIN	Max	f_T M.HZs
2N 6688	NPN	200	20	200	300	20	80	20
2N 3442	NPN	117	10	140	160	20	70	0.08
BUX 39	NPN	120	30	90	120	15	45	8
ECP 149	PNP	30	4	40	50	30	–	2.5

Darlington Pair

2N 6052	PNP	150	12	100	100	750	–	4
2N 6059	NPN	150	12	100	100	750	–	4

APPENDIX - 2

Resistor and Capacitor Values

Typical Standard Resistor Values (± 10% Tolerance)							
Ω	Ω	Ω	kΩ	kΩ	kΩ	MΩ	MΩ
–	10	100	1	10	100	1	10
–	12	120	1.2	12	120	1.2	–
–	15	150	1.5	15	150	1.5	15
–	18	180	1.8	18	180	1.8	–
–	22	220	2.2	22	220	2.2	22
2.7	27	270	2.7	27	270	2.7	–
3.3	33	330	3.3	33	330	3.3	–
3.9	39	390	3.9	39	390	3.9	–
4.7	47	470	4.7	47	470	4.7	–
5.6	56	560	5.6	56	560	5.6	–
6.8	68	680	6.8	68	680	6.8	–
–	82	820	8.2	82	820	–	–

Typical Standard Resistor Values (± 10% Tolerance)

pF	pF	pF	pF	µF	µF	µF	µF	µF	µF	µF
5	50	500	5000		0.05	0.5	5	50	50	5000
–	51	510	5100		–	–	–	–	–	–
–	56	560	5600		0.056	0.56	5.6	56	–	5600
–	–	–	6000		0.06	–	6	–	–	6000
–	62	620	6200		–	–	–	–	–	–
–	68	680	6800		0.068	0.68	6.8	–	–	–
–	75	750	7500		–	–	–	75	–	–
–	–	–	8000		–	–	8	80	–	–
–	82	820	8200		0.082	0.82	8.2	82	–	–
–	91	910	9100		–	–	–	–	–	–
10	100	1000		0.01	0.1	1	10	100	1000	10,000
–	110	1100		–	–	–	–	–	–	
12	120	1200		0.012	0.12	1.2	–	–	–	
–	130	1300		–	–	–	–	–	–	
15	150	1500		0.015	0.15	1.5	15	150	1500	
–	160	1600		–	–	–	–	–	–	
18	180	1800		0.018	0.18	1.8	18	180	–	
20	200	2000		0.02	0.2	2	20	200	2000	
24	240	2400		–	–	–	–	240	–	
–	250	2500		–	0.25	–	25	250	2500	
27	270	2700		0.027	0.27	2.7	27	270	–	
30	300	3000		0.03	0.3	3	30	300	3000	
33	330	3300		0.033	0.33	3.3	33	330	3300	
36	360	3600		–	–	–	–	–	–	
39	390	3900		0.039	0.39	3.9	39	–	–	
–	–	4000		0.04	–	4	–	400	–	
43	430	4300		–	–	–	–	–	–	
47	470	4700		0.047	0.47	4.7	47	–	–	

Physical constants

Charge of an electron	:	e	:	1.60×10^{-19} coulombs
Mass of an electron	:	m	:	9.09×10^{-31} Kg
e/m ratio of an electron	:	e/m	:	1.759×10^{11} C/Kg
Plank's constant	:	h	:	6.626×10^{-34} J-sec
Boltzman's constant	:	$\overline{K}$	:	1.381×10^{-23} J/°K
	:	K	:	8.62×10^{-5} ev/°K
Avogadro's number	:	N_A	:	6.023×10^{23} molecules/mole
Velocity of light	:	c	:	3×10^{8} m/sec
Permeability of free space	:	m_o	:	1.257×10^{-6} H/m
Permittivity of free space	:	$\hat{I}_o$	:	8.85×10^{-12} F/m
Intrinsic concentration in silicon at 300 °K	:	n_i		$= 1.5 \times 10^{10}$ /cm^3
Intrinsic resistivity in silicon at 300 °K	:	r_i		= 230,000 W–cm
Mobility of electronics in silicon	:	m_n		= 1300 cm^2/ V–sec
Mobility of holes in silicon	:	m_p		= 500 cm^2/ V–sec
Energy gap at in silicon at 300 °K	:			= 1.1 ev.

APPENDIX - 3

Capacitors

Capacitance

The farad (F) *is the SI unit of capacitance.*

The farad is the capacitance of a capacitor that contains a charge of 1 coulomb when the potential difference between its terminals is 1 volt.

Leakage Current

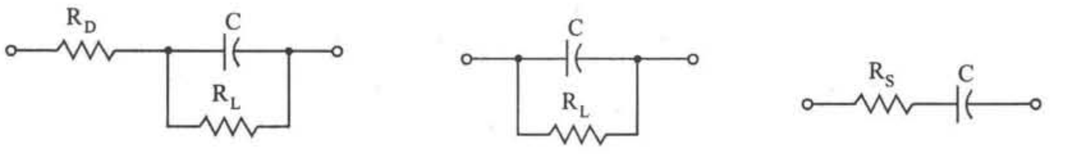
Despite the fact that the dielectric is an insulator, small leakage currents flow between the plates of a capacitor. The actual level of leakage current depends on the insulation resistance of the dielectric. Plastic film capacitors, for example, may have insulation resistances higher than 100,000 MΩ. At the other extreme, an electrolytic capacitor may have a *microampere* (or more) of leakage current, with only 10 V applied to its terminals.

Polarization

Electrolytic capacitors normally have one terminal identified as the most positive connection. Thus, they are said to be polarized. This usually limits their application to situations where the polarity of the applied voltage will not change. This is further discussed for electrolytic capacitors.

Capacitor Equivalent Circuit

An ideal capacitor has a dielectric that has an infinite resistance and plates that have zero resistance. However, an ideal capacitor does not exist, as all dielectrics have some leakage current and all capacitor plates have some resistance. The complete equivalent circuit for a capacitor [shown in Fig. A-3.1(a)] consists of an ideal capacitor C in series with a resistance R_D representing the resistance of the plates, and in parallel with a resistance R_L representing the leakage resistance of the dielectric. Usually, the plate resistance can be completely neglected, and the equivalent circuit becomes that shown in Fig. A-3.1(b). With capacitors that have a very high leakage resistance (e.g., mica and plastic film capacitors), the parallel resistor is frequently omitted in the equivalent circuit, and the capacitor is then treated as an ideal capacitor. This cannot normally be done for electrolytic capacitors, for example, which have relatively low leakage resistances. The parallel R_C circuit in,



(a) Complete equivalent circuit (b) Parallel equivalent circuit (c) Series equivalent circuit

Fig. A. 3.1

A capacitor equivalent circuit consists o©f the capacitance C, the leakage resistance R_L *in parallel with* C, *and the plate resistance* R_D *in series with C and* R_L.

Fig. A. 3.1 (b) can be shown to have an equivalent series *RC* circuit, as in Fig. A. 3.1(c). This is treated in Section 20-6.

A variable air capacitor is made up of a set of movable plates and a set of fixed plates separated by air.

Because a capacitor's dielectric is largely responsible for determining its most important characteristics, capacitors are usually identified by the type of dielectric used.

Air Capacitors

A typical capacitor using air as a dielectric is illustrated in Fig. A.3.2. The capacitance is variable, as is the case with virtually all air capacitors. There are two sets of metal plates, one set fixed and one movable. The movable plates can be adjusted into or out of the spaces between the fixed plates by means of the rotatable shaft. Thus, the area of the plates opposite each other is increased or decrea and the capacitance value if altered.

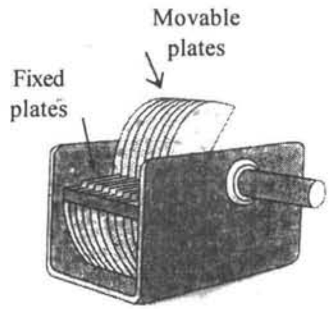


Fig. A. 3.2 A variable air capacitor is made up of a set of movable plates and a set of fixed plates separated by air

Paper Capacitors

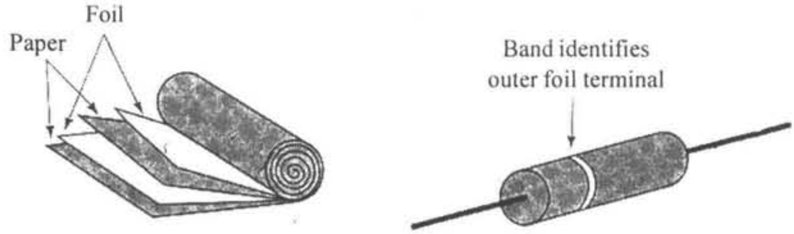
In its simplest form, a paper capacitor consists of a layer of paper between two layers of metal foil. The metal foil and paper are rolled up, as illustrated in Fig. A.3.3 (a); external connections are brought out from the foil layers, and the complete assembly is dipped in wax or plastic. A variation of this is the metalized paper construction, in which the foil is replaced by thin films of metal deposited on the surface of the paper. One end of the capacitor sometimes has a band around it [see Fig. A.3.3 (b)]. This does not mean that the device is polarized but simply identifies the terminal that connects to the outside metal film, so that it can be grounded to avoid pickup of unwanted signals.

Paper capacitors are available in values ranging from about 500 pF to 50μF, and in dc working voltages up to about 600 V. They are among the lower-cost capacitors for a given capacitance value but are physically larger than several other types having the same capacitance value.

Plastic Film Capacitors

The construction of plastic film capacitors is similar to that of paper capacitors, except that the paper is replaced by a thin film that is typically polystyrene or Mylar. This type of dielectric gives insulation resistances greater than 100 000 MΩ. Working voltages are as high as 600 V, with the capacitor surviving 1500 V surges for a brief period. Capacitance tolerances of ± 2.5% are typical, as are temperature coefficients of 60 to 150 ppm/°C.

Plastic film capacitors are physically smaller but more expensive than paper capacitors. They are typically available in values ranging from 5 pF to 0.47 μF.



(a) Construction of a paper capacitor (b) Appearance of a paper capacitor

Fig. A. 3.3 In a paper capacitor, two sheets of metal foil separated by a sheet of paper are rolled up together. External connections are made to the foil sheets.

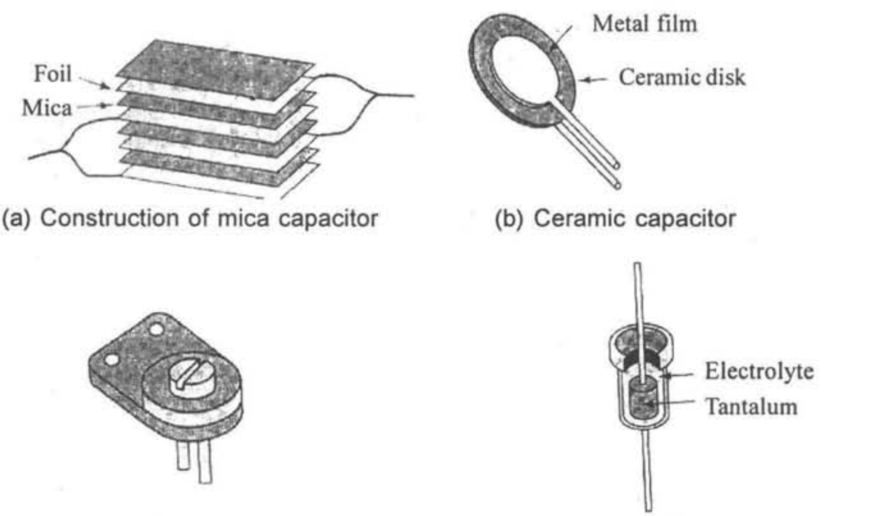
Mica Capacitors

As illustrated in Fig. A. 3.4(a), mica capacitors consist of layers of mica alternated with layers of metal foil. Connections are made to the metal foil for capacitor leads, and the entire assembly is dipped in plastic or encapsulated in a molded plastic jacket. Typical capacitance values range from 1pF to 0.1μF, and voltage ratings as high as 35 000 V are possible. Precise capacitance values and wide operating temperatures are obtainable with mica capacitors. In a variation of the process, silvered mica capacitors use films of silver deposited on the mica layers instead of metal foil.

Ceramic Capacitors

The construction of a typical ceramic capacitor is illustrated in Fig. A. 3.4(b). Films of metal are deposited on each side of a thin ceramic disc, and copper wire terminals are connected to the metal. The entire units is then encapsulated in a protective coating of plastic. Two different types of ceramic are used, one of which has extremely high relative permitivity. This gives capacitors that are much smaller than paper or mica capacitors having the same capacitance value. One disadvantage of this particular ceramic dielectric is that its leakage resistance is not as high as with other types. Another type of ceramic gives leakage resistances on the order of 7500 MΩ. Because of its lower permitivity, this ceramic produces capacitors that are relatively large for a given value of capacitance.

The range of capacitance values available with ceramic capacitors is typically 1 pF to 0.1 μF, with dc working voltages up to 1000 V.



(a) Construction of mica capacitor

(b) Ceramic capacitor

(c) Ceramic trimmer

(d) Construction of tantalum capacitor

Fig. A. 3.4 Mica capacitors consist of sheets of mica interleaved with foil. A ceramic disc silvered on each side makes a ceramic capacitor; in a ceramic trimmer, the plates area is screwdriver adjustable. A tantalum capacitor has a relatively large capacitance in a small volume.

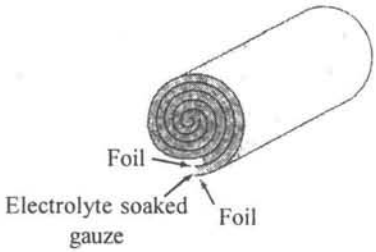
Fig. A. 3.4(c) shows a variable ceramic capacitor known as a *trimmer*. By means of a screwdriver, the area of plate on each side of a dielectric can be adjusted to alter the capacitance value. Typical ranges of adjustment available are 1.5 pF to 3 pF and 7 pF to 45 pF.

Electrolytic Capacitors

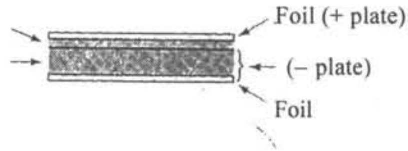
The most important feature of electrolytic capacitors is that they can have a very large capacitance in a physically small container. For example, a capacitance of 5000 μF can be obtained in a cylindrical package approximately 5 cm long by 2 cm in diameter. In this case the dc working voltage is only voltage is only 10V. Similarly, a 1 F capacitor is available in a 22 cm by 7.5 cm cylinder, with a working voltage of only 3 V. Typical values for electrolytic capacitors range from 1 μF through 100 000 μF.

The construction of an electrolytic capacitor is similar to that of a paper capacitor (Fig. A.3.5(a)). Two sheets of aluminium foil separated by a fine gauze soaked in electrolyte are rolled up and encased in an aluminium cylinder for protection. When assembled, a direct voltage is applied to the capacitor terminals, and this causes a thin layer of aluminium oxide to form on the surface of the positive plate next to the electrolyte (Fig. A.3.5(b)). The aluminium oxide is the dielectric, and the electrolyte and positive sheet of foil are the capacitor plates. The extremely thin oxide dielectric gives the very large value of capacitance.

It is very important that electrolytic capacitors be connected with the correct polarity. When incorrectly connected, gas forms within the electrolyte and the capacitor may **explode**! Such an explosion blows the capacitor apart and spreads its contents around. This could have **tragic consequences** for the eyes of an experimenter who happens to be closely examining the circuit when the explosion occurs. The terminal designated as positive must be connected to the most positive of



(a) Rolled-up foil sheets and electrolyte-soaked gauze

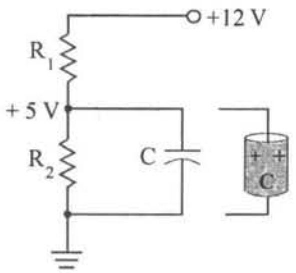


(b) The dielectric is a thin layer of aluminium oxide

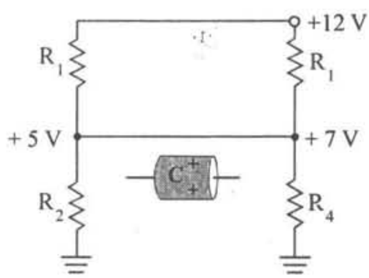
Fig. A. 3.5 An electrolyte capacitor is constructed of rolled-up foil sheets separated by electrolyte-soaked gauze, the dielectric is a layer of aluminium oxide at the positive plate

the two points in the circuit where the capacitor is to be installed. Fig. A. 3.6 illustrates some circuit situations where the capacitor must be correctly connected. Nonpolarized electrolytic capacitors can be obtained. They consist essentially of two capacitors in one package connected *back to back*, so one of the oxide films is always correctly biased.

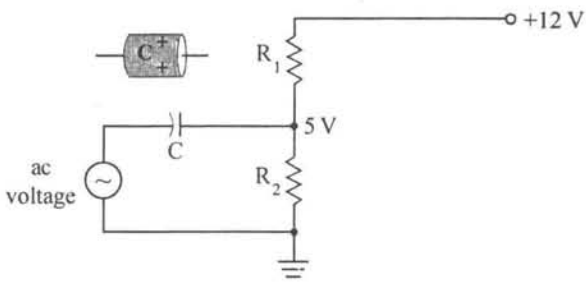
Electrolytic capacitors are available with dc working voltages greater than 400 V, but in this case capacitance values do not exceed 100 mF. In addition to their low working voltage and polarized operation. Another disadvantage of electrolytic capacitors is their relatively high leakage current.



(a) Capacitor connected between +5 V and ground



(b) Connected between +7 V and +5 V



(c) Connected between + 5.7 V and a grounded ac voltage source

Fig. A. 3.6 It is very important that polarized capacitors be correctly connected. The capacitor positive terminal voltage must be more positive than the voltage at the negative terminal.

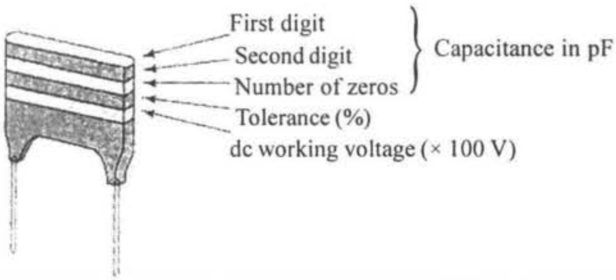
Tantalum Capacitors

This is another type of electrolytic capacitor. Powdered tantalum is sintered (or baked), typically into a cylindrical shape. The resulting solid is quite porous, so that when immersed in a container of electrolyte, the electrolyte is absorbed into the tantalum. The tantalum then has a large surface area in contact with the electrolyte (Fig. A. 3.5). When a dc *forming voltage* is applied, a thin oxide film is formed throughout the electrolyte-tantalum contact area. The result, again, is a large capacitance value in a small volume.

Capacitor Color Codes

Physically large capacitors usually have their capacitance value, tolerance and dc working voltage printed on the side of the case. Small capacitors (like small resistors) use a code of colored bands (or sometimes colored dots) to indicate the component parameters.

There are several capacitor color codes in current use. Here is one of the most common.



Color	Significant Figure	Tolerance (%)
Black	0	20
Brown	1	1
Red	2	2
Orange	3	3
Yellow	4	4
Green	5	5
Blue	6	6
Violet	7	7
Grey	8	8
White	9	9
Silver	0.01	10
Gold	0.1	5
No band		20

A typical tantalum capacitor in a cylindrical shape 2 cm by 1 cm might have a capacitance of 100 mF and a dc working voltage of 20 V. Other types are available with a working voltage up to 630 V, but with capacitance values on the order of 3.5 mF. Like aluminium-foil electrolytic capacitors, tantalum capacitors must be connected with the correct polarity size of the inductor, the maximum current can be anything from about 50 mA to 1 A. The core in such an inductor may be made adjustable so that it can be screwed into or partially out of the coil. Thus, the coil inductance is variable. Note the graphic symbol for an inductor with an adjustable core [Fig. A. 3.6(b)].

APPENDIX - 4

Inductors

Magnetic Flux and Flux Density

*The weber** (Wb) *is the SI unit of magnetic flux.*

The weber is defined as the magnetic flux which, linking a single-turn coil, produces an emf of 1 V when the flux is reduced to zero at a constant rate in 1 s.

*The tesla**** (T) *is the SI unit of magnetic flux density.*

The tesla is the flux density in a magnetic field when 1 Wb of flux occurs in a plane of 1 m^2*; that is, the tesla can be described as 1* Wb/m^2.

Inductance

The SI unit of inductance is the henry (H).

The inductance of a circuit is 1 henry (1 H) when an emf of 1 V is induced by the current changing at the rate of 1 A/s.

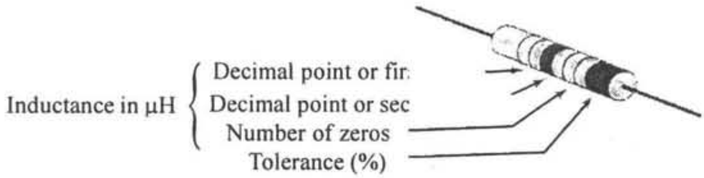
Molded Inductors

A small molded inductor is shown in Fig. A. 4.2(c). Typical available values for this type range from 1.2 μH to 10 mH, maximum currents of about 70 mA. The values of molded inductors are identified by a color code, similar to molded resistors. Fig. A. 4.2(d) shows a tiny-film inductor used in certain types of electronic circuits. In this case the inductor is simply a thin metal film deposited in the form of a spiral on ceramic base.

Laboratory Inductors

Laboratory-type variable inductors can be constructed in decade box format, in which precision inductors are switched into or out of a circuit by means of rotary switches. Alternatively, two coupled coils can be employed as a variable inductor. The coils may be connected in series or in parallel, and the total inductance is controlled by adjusting the position of one coil relative to the other.

Color Code For Small Inductors



Color	Significant Figure	Tolerance (%)
Black	0	
Brown	1	
Red	2	
Orange	3	
Yellow	4	
Green	5	
Blue	6	
Violet	7	
Grey	8	
White	9	
Silver		10
Gold	decimal point	5
No band		20

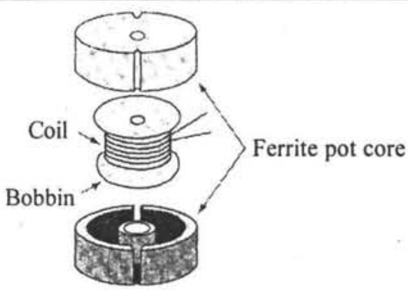
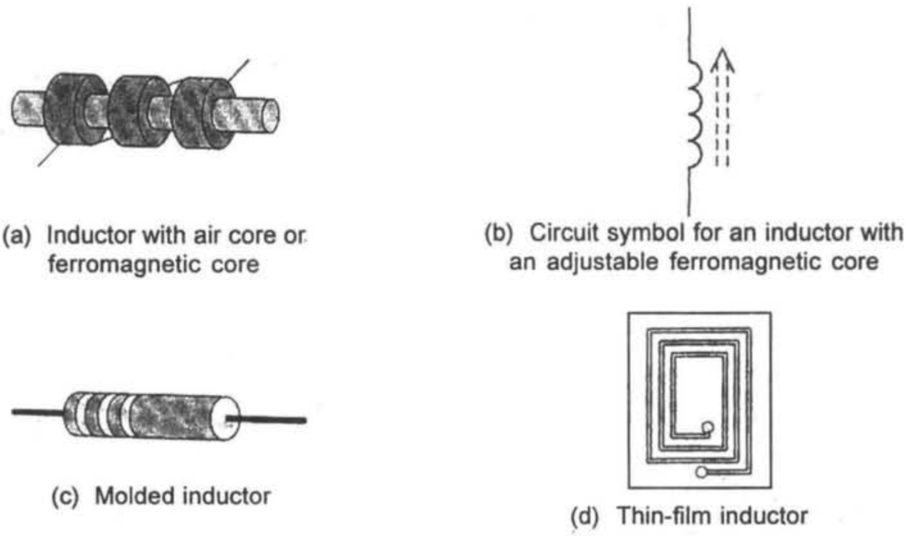


Fig. A. 4.1 Some low-current, high-frequency inductors are wound on bobbins contained in a ferrite pot core. The ferrite core increases the winding inductance and screens the inductor

Coil to protect adjacent components against flux leakage and to protect the coil from external magnetic fields. The coil is wound on a bobbin, so its number of turns is easily modified.

Three different types of low-current inductors are illustrated in Fig. A. 4.2. Fig. A 4.2(a) shows a type that is available either as an air-cored inductor or with a ferromagnetic core. With an air core, the inductance values up to about 10 mH can be obtained. Depending on the thickness of wire used and the physical.



(a) Inductor with air core or ferromagnetic core

(b) Circuit symbol for an inductor with an adjustable ferromagnetic core

(c) Molded inductor

(d) Thin-film inductor

Fig. A. 4.2 Small inductors may be wound on an insulating tube with an adjustable ferrite core, molded like small resistors, or deposited as a conducting film on an insulating material

If the mutual inductance between two adjacent coils is not known, it can be determined by measuring the total inductance of the coils in series-aiding and series-opposing connections. Then,

$$L_a = L_1 + L_2 + 2M \qquad \text{for series-aiding}$$

and

$$L_b = L_1 + L_2 - 2M \qquad \text{for series-opposing}$$

Subtracting,

$$L_a - L_b = 4M$$

Therefore,

$$\boxed{M = \frac{L_a - L_b}{4}}$$

$$M = k\sqrt{L_1 L_2}$$

From these two equations, the coefficient of coupling of the two coils can be determined.

Stray Inductance

Inductance is (change in flux linkages) / (change in current). So every current-carrying conductor has some self-inductance, and every pair of conductors has inductance. These *stray inductance* are usually unwanted, although they are sometimes used as components in a circuit design. In dc applications, stray inductance is normally unimportant, but in radio frequency ac circuits it can be considerable nuisance. Stray inductance is normally minimized by keeping connecting wires as short as possible.

Summary of Formulae

Induced emf	:	$e_L = \dfrac{\Delta\Phi}{\Delta t}$
Induced emf	:	$e_L = \dfrac{\Delta\Phi}{\Delta t}$
Inductance	:	$L = \dfrac{e_L}{\Delta i / \Delta t}$
Inductance	:	$L = \dfrac{\Delta\Phi N}{\Delta i}$
Flux change	:	$\Delta\Phi = \mu, \mu_0 \, \Delta i \, N \, \dfrac{A}{t}$
Self - inductance	:	$L = \mu, \mu_0 \, \Delta i \, N^2 \, \dfrac{A}{t}$
Mutual inductance	:	$M = \dfrac{e_L}{\Delta i / \Delta t}$
Induced emf	:	$e_L = \dfrac{\Delta\Phi N_s}{\Delta t}$
Mutual inductance	:	$M = \dfrac{\Delta\Phi N_s}{\Delta i}$
Mutual inductance	:	$M = k \, \dfrac{\Delta\Phi N_s}{\Delta i}$
Mutual inductance	:	$M = k\sqrt{L_1 L_2}$
Energy stored	:	$W = \dfrac{1}{2} LI^2$
Energy stored	:	$W = \dfrac{B^2 Al}{2\mu_0}$
Inductances in series	:	$L_s = L_1 + L_2 + L_3 + ...$
Inductances in parallel	:	$\dfrac{1}{L_P} = \dfrac{1}{L_1} + \dfrac{1}{L_2} + \dfrac{1}{L_3} + ...$
Total inductance (series-aiding)	:	$L = L_1 + L_2 + 2M$
Total inductance (series-opposing)	:	$L = L_1 + L_2 - 2M$
Mutual inductance	:	$M = \dfrac{L_o - L_b}{4}$

Miscellaneous

Ionic Bonding

In some insulating materials, notably rubber and plastics, the bending process is also covalent. The valence electrons in these bonds are very strongly attached to their atoms, so the possibility of current flow is virtually zero. In other types of insulating materials, some atoms have parted with outer-shell electrons, but these have been accepted into the orbit of other atoms. Thus, the atoms are *ionized*; those which gave up electrons have become *positive ions*, and those which accepted the electrons become negative ions. This creates an electrostatic bonding force between the atoms, termed ionic bonding. Ionic bonding is found in such materials as glass and porcelain. Because there are virtually no free electrons, no current can flow, and the material is an insulator.

Insulators

Fig. A. 5.1 shows some typical arrangements of conductors and insulators. Electric cable usually consists of conducting copper wire surrounded by an insulating sheath of rubber or plastic. Sometimes there is more than one conductor, and these are, of course, individually insulated.

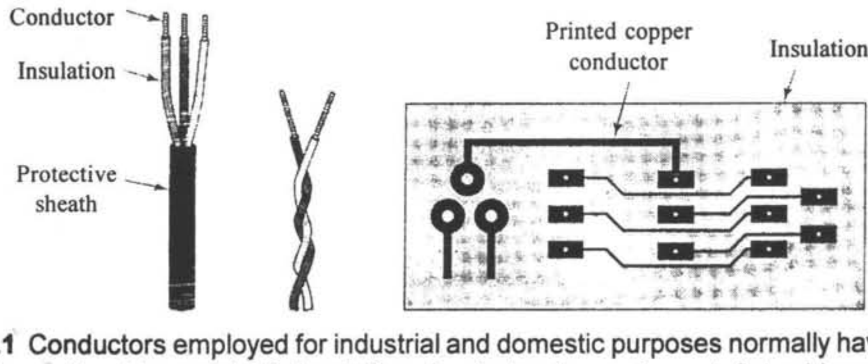


Fig. A. 5.1 Conductors employed for industrial and domestic purposes normally have stranded copper wires with rubber or plastic insulation. In electronics equipment, flat cables of fine wires and thin printed circuit conductors are widely used.

Conductors

The function of a conductor is to conduct current form one point to another in an electric circuit. As discussed, electric cables usually consist of copper conductors sheathed with rubber or plastic

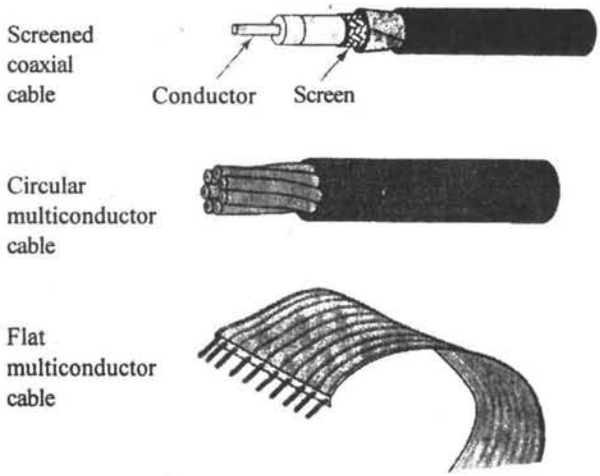
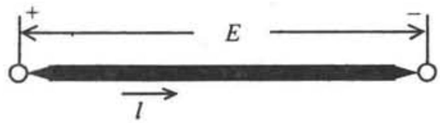


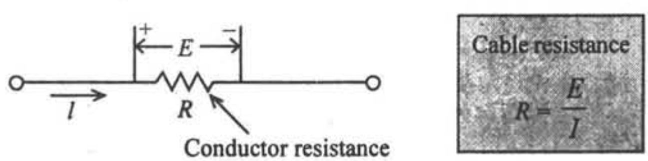
Fig. A. 5.2 Many different types of cables are used with electronics equipment.

insulating material. Cables that have to carry large currents must have relatively thick conductors. Where very small currents are involved, the conductor may be a thin strip of copper or even an aluminium film. Between these two extremes, a wide range of conductors exist for various applications. Three different types of cables used in electronics equipment are illustrated in Fig. A. 5.2 conductor and a circular plaited conducting screen, as well as an outer insulating sheath. The other two are multiconductor cables, one circular, and one flat.

Because each conductor has a finite resistance, a current passing through it causes a voltage drop from one end of the conductor to the other (Fig. A. 5.3). When conductors are long and/or carry large currents, the conductor voltage drop may cause unsatisfactory performance of the equipment supplied. Power (I^2 R) is also dissipated in every current-carrying conductor, and this is, ofcourse, wasted power.

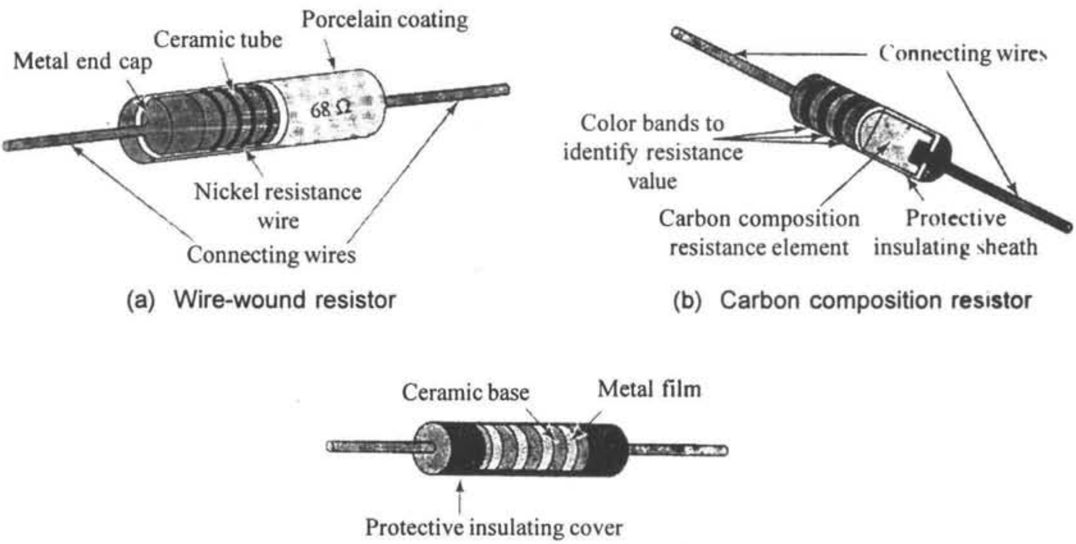


(a) Current flow through a conductor produces a voltage drop along the conductor



(b) Conductor resistance causes voltage drop when a current flows

Fig. A. 5.3 Conductor resistance (R) is determined by applying the voltage drop and current level to Ohm's law. The resistance per unit length (R/l) is then used to select a suitable wire gauge.



(a) Wire-wound resistor

(b) Carbon composition resistor

(c) Metal film resistor

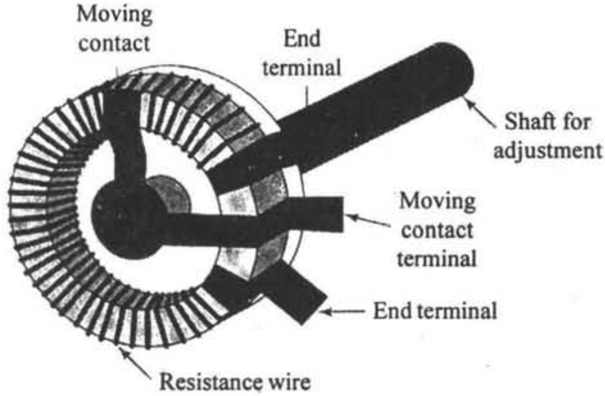
Fig. A. 5.4 Individual resistors are typically wire-wound or carbon composition construction. Wirewound resistors are used where high power dissipation is required. Carbon composition type is the least expensive. Metal film resistance values can be more accurate than carbon composition type.

The illustration in Fig. A. 5.5(a) shows a coil of closely wound insulated resistance wire formed into partial circle. The coil has a low-resistance terminal at each end, and a third terminal is connected to a movable contact with a shaft adjustment facility. The movable contact can be set to any point on a connecting track that extends over one (unisulated) edge of the coil. Using the adjustable contact, the resistance from either end terminal to the center terminal may be adjusted from zero to the maximum coil resistance.

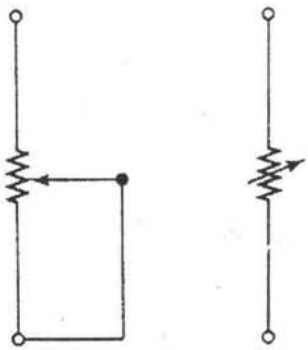
Another type of variable resistor, known as a decade resistance box, is shown in Fig. A. 5.5(c). This is a laboratory component that contains precise values of switched series-connected resistors. As illustrated, the first switch (from the right) controls resistance values in 1Ω steps from 0Ω to 9Ω and the second switches values of 10Ω, 20Ω, 30Ω, and so on. The decade box shown can be set to within $+ 1\Omega$ of any value from 0Ω to 9999Ω. Other decade boxes are available with different resistance ranges.

Resistor Tolerance

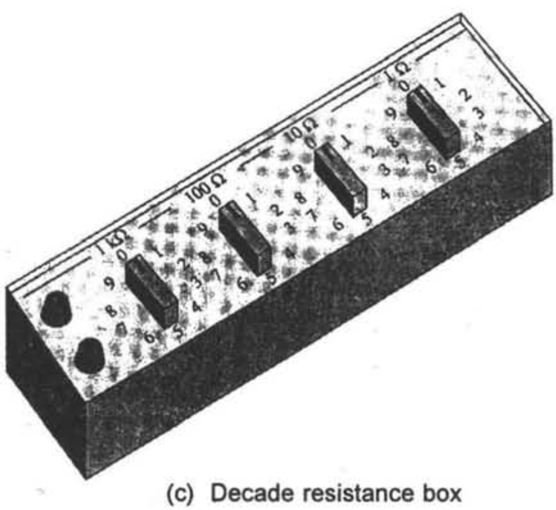
Standard (fixed-value) resistors normally range from 2.7Ω to $22M\Omega$. The resistance tolerances on these standard values are typically $\pm$ 20%, $\pm$ 10%, $\pm$ 5% or $\pm$ 1%. A tolerance of + 10% on a 100Ω resistor means that the actual resistance may be as high as 100Ω + 10% (i.e., 110Ω) or as low as 100Ω – 10% (i.e., 90Ω). Obviously, the resistors with the smallest tolerance are the most accurate and the most expensive.



(a) Typical construction of a resistor variable resistor (and potentiometer)



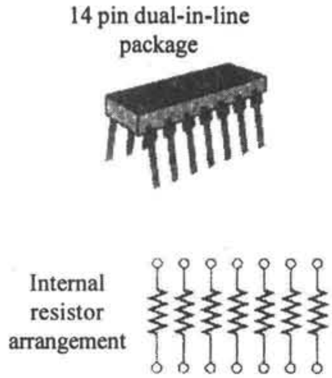
(b) Circuit symbols for a variable resistor



(c) Decade resistance box

Fig. A. 5.5 Small variable resistors are used in electronic circuit construction. Large decade resistance boxes are employed in electronics laboratories.

More Resistors

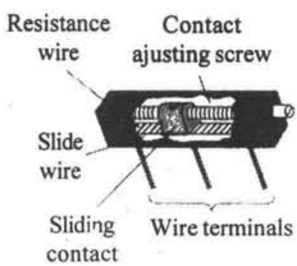


Resistor Networks

Resistor networks are available in *integrated circuits* type *dual-in-lin* package. One construction method uses a *thick film* technique in which conducting solutions are deposited in the required form.

Photoconductive Cell

This is simply a resistor constructed of photoconductive material (cadmium selenide or cadmium sulfide). When dark, the cell resistance is very high. When illuminated, the resistance decreases in proportion to the level of illumination.



Low Power Variable Resistor

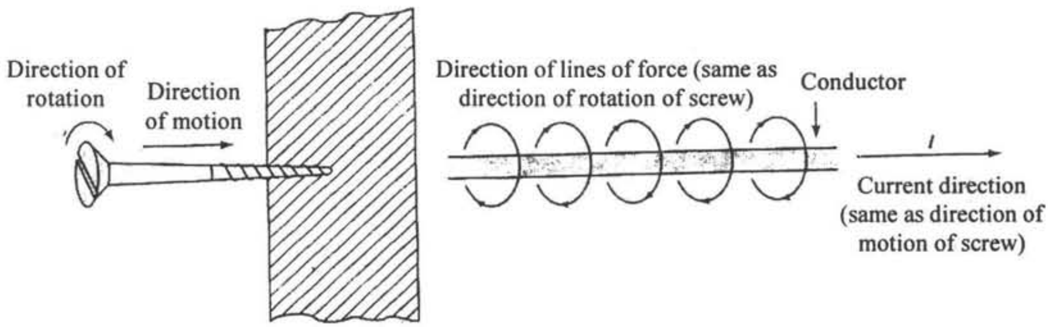
A small variable resistor suitable for mounting directly on a circuit board. A threaded shaft, which is adjustable by a screwdriver, sets the position of the moving contact on a resistance wire.

High Power Resistor

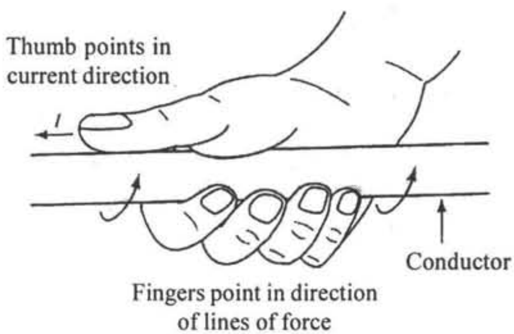
High power resistors are usually wire-wound on the surface of a ceramic tube. Air flow through the tube helps to keep the resistor from overheating.

Two memory aids for determining the direction of the magnetic flux around a current-carrying conductor are shown in Fig. A. 5.6. The right-hand-screw rule as illustrated in Fig. A. 5.6(a) shows a wood screw being turned clockwise and progressing into a piece of wood. The horizontal direction of the screw is analogous to the direction of current in a conductor, and the circular motion of the screw shows the direction of magnetic flux around the conductor. In the right-hand rule, illustrated in Fig. A. 5.6(b), a right hand is closed around a conductor with the thumb ointing in the (conventional) direction of current flow. The fingers point in the direction of the magnetic lines of force around the conductor.

Because a current-carrying conductor has a magnetic field around it, when two current-carrying conductors are brought close together there will be interaction between the fields. Fig. A. 5.7(a) shows the effect on the fields when two conductors carrying in opposite direction are adjacent. The directions of the magnetic passes through the center of the coil. Therefore, the one-turn coil acts like a little magnet and has a magnetic field with an identifiable N pole and S pole. Instead of a single turn, the coil may have many turns, as illustrated in Fig. A. 5.7(c). In this case the flux generated by each of the individual current-carrying turns tends to link up and pass out of one end of the coil and back into the other end. This type of coil, known as a solenoid, obviously has a magnetic field pattern very similar to that of a bar magnet.



(a) Right-hand screw rule



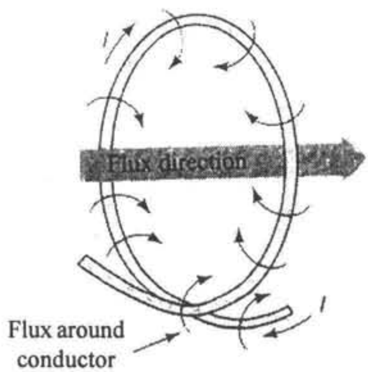
(b) Right-hand rule

Fig. A. 5.6 The right-hand-screw rule and the right-hand rule can be used for determining the direction of the magnetic lines of force around a current-carrying conductor.

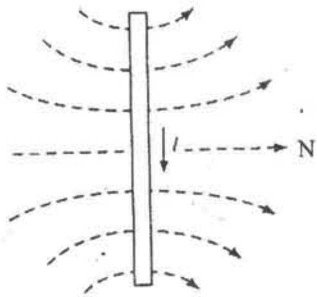
The right-hand rule for determining the direction of flux from a solenoid is illustrated in Fig. A. 5.7(d). When the solenoid is gripped with the right hand so that the fingers are pointing in the direction of current flow in the coils, the thumb points in the direction of the flux (i.e., toward the N-pole end of the solenoid).

Electromagnetic Induction

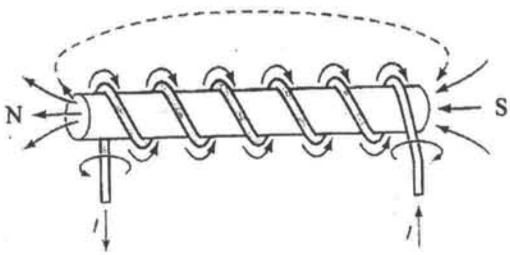
It has been demonstrated that a magnetic flux is generated by an electric current flowing in a conductor. The converse is also possible; that is, a magnetic flux can produce a current flow in a conductor.



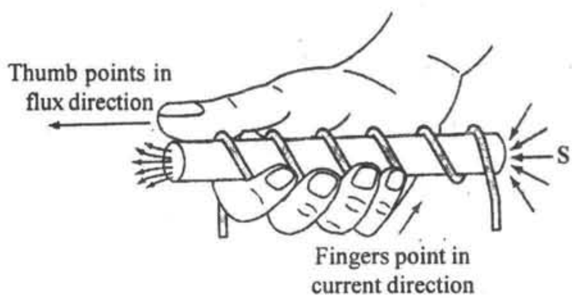
(a) All of the flux passes through the center of the coil turn



(b) Side view of coil turn and flux



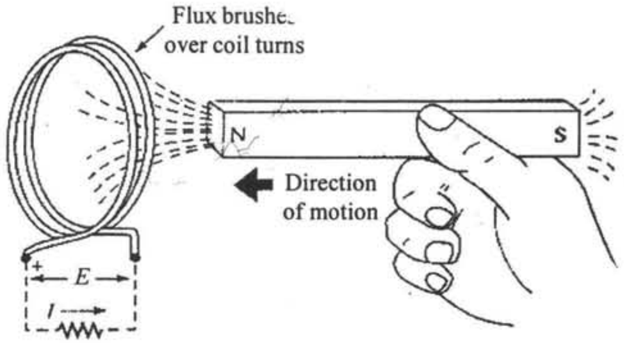
(c) A solenoid sets up a flux like a bar magna



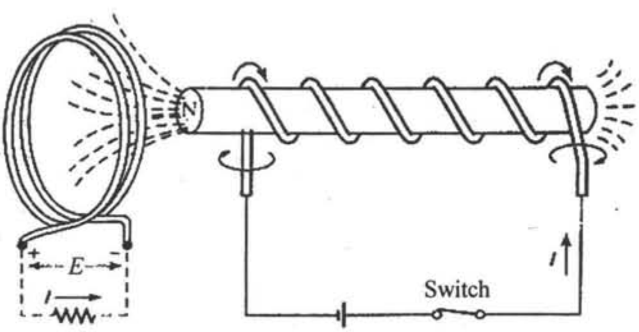
(d) Right-hand rule for solenoid flux direction

Fig. A. 5.7 In current-carrying coils, the magnetic lines of force around the conductors all pass through the center of the coil.

Consider Fig. A. 5.8(a), in which a handled bar magnet is shown being brought close to a coil of wire. As the bar magnet approaches the coil, the flux from the magnet *brushes across* the coil conductors or cuts the conductors. This produces a current flow in the conductors proportional to the total flux that cuts the coil. If the coil circuit is closed by a resistor (as shown broken in the figure), a current flows. Whether or not the circuit is closed, an *electromotive force* (emf) can be measured at the coil terminals. This effect is known as *electromagnetic* induction.

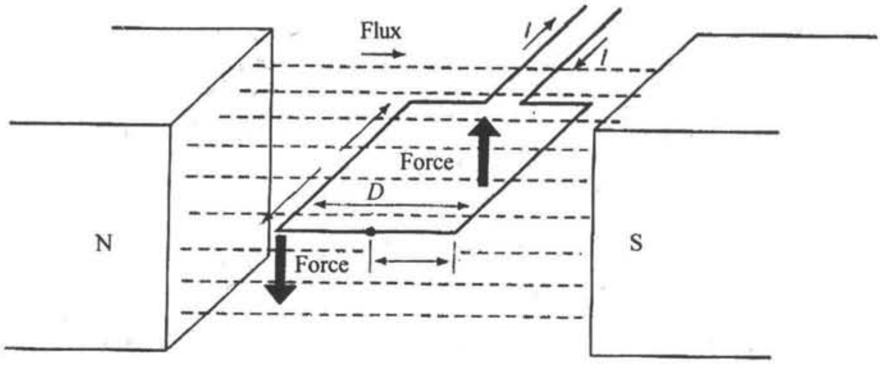


(a) emf induced in a coil by the motion of the flux from the bar magnet

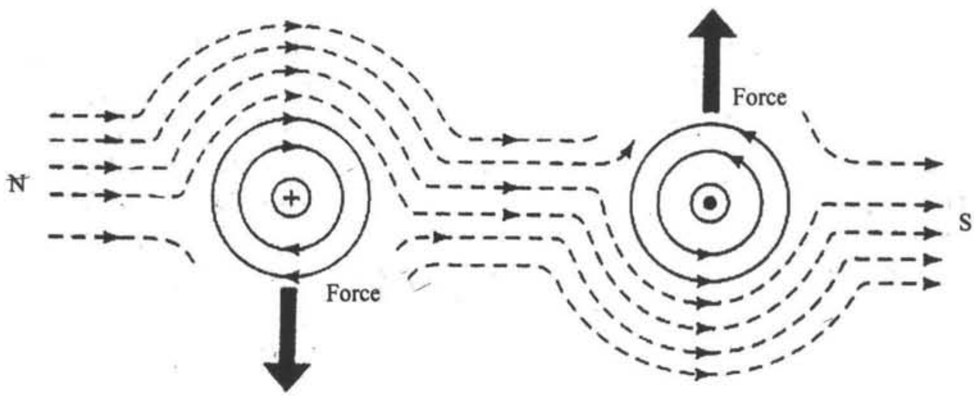


(b) emf induced in a coil by the motion of the flux from the solenoid when the current is switched on or off

Fig. A. 5.8 An electromotive force (emf) is induced in a coil when the coil is brushed by a magnetic field. The magnetic field may be from a bar magnet or from a current-carrying coil.



(a) Single-turn coil pivoted in a magnetic field



(b) Showing the force on each side of a single-turn pivoted in a magnetic field

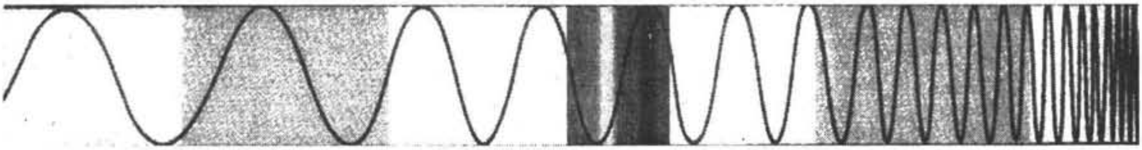
Fig. A. 5.9 A force is exerted on each side of a current-carrying coil pivoted in a magnetic field. This force tends to cause the coil to rotate

Fibre Optic Cables :

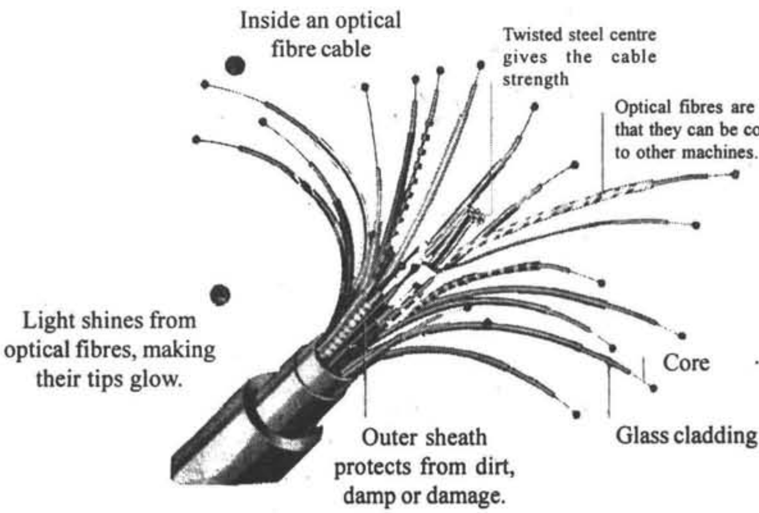
Light and Other Rays

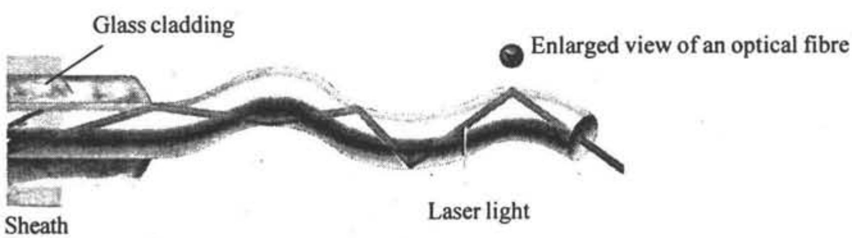
Light rays or waves are a type of energy called electromagnetic energy. They shine out, or radiate, from their source, so they are called electromagnetic radiation. Light rays are just a tiny part of a huge range of rays and waves called the electromagnetic spectrum (EMS)

- The parts of the electromagnetic spectrum have different wavelengths and different names.



Radio waves | Micro-waves | Infra-red waves | Light waves | Ultra-violet waves | X-rays | Gamma rays

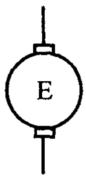




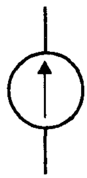
Circuit Symbols

dc voltage source or single-cell battery

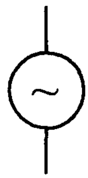
Multicell battery



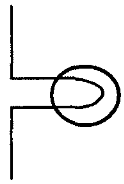
Generator



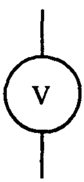
Current source



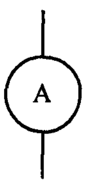
ac voltage source



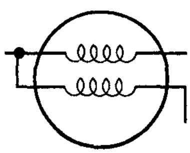
Lamp



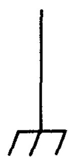
Voltmeter



Ammeter



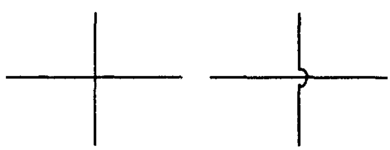
Wattmeter



Chassis

Ground

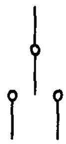
Conductor connection or junction

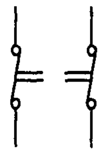


Unconnected crossing conductors

Fuse

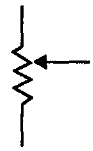

dc voltage source or single-cell battery


Two-way switch


Double-pole switch


Resistor


Variable resistor

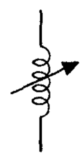

Potentiometer


Capacitor


Variable capacitor


Air-cored inductor


Iron-cored inductor


Variable inductor

APPENDIX - 7

Unit Conversion Factors

The following factors may be used for conversion between non-SI units and SI units.

To Convert	To	Multiply By
Area Units		
acres	square meters (m^2)	4047
acres	hectares (ha)	0.4047
circular mils	square meters (m^2)	5.067×10^{-10}
square feet	square meters (m^2)	0.0909
square inches	square centimeters (cm^2)	6.452
square miles	hectares (ha)	259
square miles	square kilometers (km^2)	2.59
square yards	square meters (m^2)	0.8361
Electric and Magnetic Units		
amperes/inch	amperes/meter (A/m)	39.37
gauses	teslas (T)	10^{-4}
gilberts	ampere (turns) (A)	0.7958
lines/sq. inch	teslas (T)	1.55×10^{-5}
Maxwells	webers (Wb)	10^{-8}
mhos	Siemens (S)	1
Oersteds	amperes/meter	79.577
Energy and Work Units		
Btu	joules (J)	1054.8
Btu	kilowatt-hours (kWh)	2.928×10^{-4}
ergs	joules (J)	10^{-7}
ergs	kilowatt-hours (kWh)	0.2778×10^{-13}
foot-pounds	joules (J)	1.356
foot-pounds	kilogram meters (kgm)	0.1383

Force Units		
dynes	grams (g)	1.02×10^{-3}
dynes	newtons (N)	10^{-5}
pounds	newtons (N)	4.448
poundals	newtons (N)	0.1383
grams	newtons (N)	9.807×10^{-3}
Illumination Units		
foot-candles	lumens/cm^2	10.764

To Convert	To	Multiply By
Linear Units		
angstroms	meters (m)	1×10^{-10}
feet	meters (m)	0.3048
fathoms	meters (m)	1.8288
inches	centimeters (cm)	2.54
microns	meters (m)	10^{-6}
miles (nautical)	kilometers (km)	1.853
miles (statute)	kilometers (km)	1.609
mils	centimeters (cm)	2.54×10^{-3}
yards	meters (m)	0.9144
Power Units		
horsepower	watts (W)	745.7
Pressure Units		
atmospheres	kilograms/sq. meter (kg/m^2)	10 332
atmospheres	kilopascals (kPa)	101.325
bars	kilopascals (kPa)	100
bars	kilograms/sq.meter (kg/m^2)	1.02 × 10–4
pounds/sq. foot	kilograms/sq.meter (kg/m^2)	4.882
pounds/sq. inch	kilograms/sq.meter (kg/m^2)	703
Temperature Units		
degrees Fahrenheit (°F)	degrees celsius (°C)	(°F – 32)/1.8
degrees Fahrenheit (°F)	degrees kelvin (K)	273.15 + (°F – 32)/1.8

Velocity Units

miles/hour (mph)	kilometers/hour (km/h)	1.609
knots	kilometers/hour (km/h)	1.853

Volume Units

bushels	cubic meters (m^3)	0.035 24
cubic feet	cubic meters (m^3)	0.028 32
cubic inches	cubic centimeters (cm^3)	16.387
cubic inches	liters (1)	0.016 39
cubic yards	cubic meters (m^3)	0.7646
gallons (U.S.)	cubic meters (m^3)	3.7853×10^{-3}
gallons (imperial)	cubic meters (m^3)	4.546×10^{-3}
gallons (U.S.)	liters (1)	3.7853
gallons (imperial)	liters (1)	4.546
gills	liters (1)	0.1183
pints (U.S.)	liters (1)	0.4732
pints (imperial)	liters (1)	0.5683

Gauge	Diameter (mm)	Copper Wire Resistance (Ω/km)	Diameter (mil)	Copper Wire Resistance (Ω/km)
36	0.127	1360	5	415
37	0.113	1715	4.5	523
38	0.101	2147	4	655
39	0.090	2704	3.5	832
40	0.080	3422	3.1	1044

To Convert	To	Multiply By
quarts (U.S.)	liters (1)	0.9463
quarts (imperial)	liters (1)	1.137

Weight Units

ounces	grams (g)	28.35
pounds	kilograms (kg)	0.453 59
tons (long)	kilograms (kg)	1016
tons (short)	kilograms (kg)	907.18

The siemens* is the unit of conductance.

$$\text{conductance} = \frac{1}{\text{resistance}}$$

American Wire Gauge Sizes and Metric Equivalents

Gauge	Diameter (mm)	Copper wire Resistance (Ω/km)	Diameter (mill)	Copper wire Resistance (Ω/1000 ft)
0000	11.68	0.160	460	0.049
000	10.40	0.203	409.6	0.062
00	9.266	0.255	364.8	0.078
0	8.252	0.316	324.	0.098
1	7.348	0.406	289.3	0.124
2	6.543	0.511	257.6	0.156
3	5.827	0.645	229.4	0.197
4	5.189	0.813	204.3	0.248
5	4.620	1.026	181.9	0.313
6	4.115	1.29	162	0.395
7	3.665	1.63	144.3	0.498
8	3.264	2.06	128.5	0.628
9	2.906	2.59	114.4	0.792
10	2.588	3.27	101.9	0.999
11	2.30	4.10	90.7	1.26
12	2.05	5.20	80.8	1.59
13	1.83	6.55	72	2
14	1.63	8.26	64.1	2.52
15	1.45	10.4	57.1	3.18
16	1.29	13.1	50.8	4.02
17	1.15	16.6	45.3	5.06
18	1.02	21.0	40.3	6.39

19	0.912	26.3	35.9	8.05
20	0.813	33.2	32	10.1
21	0.723	41.9	28.5	12.8
22	0.644	52.8	25.3	16.1
23	0.573	66.7	22.6	20.3
24	0.511	83.9	20.1	25.7
25	0.455	106	17.9	32.4
26	0.405	134	15.9	41
27	0.361	168	14.2	51.4
28	0.321	213	12.6	64.9
29	0.286	267	11.3	81.4
30	0.255	337	10	103
31	0.227	425	8.9	130
32	0.202	537	8	164
33	0.180	676	7.1	206
34	0.160	855	6.3	261
35	0.143	1071	5.6	329

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