Refreshing Thoughts on DRAM
Power Saving vs. Data Integrity

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DRAM Refresh

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- Probabilistic memory

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- Energy vs. accuracy trade-off
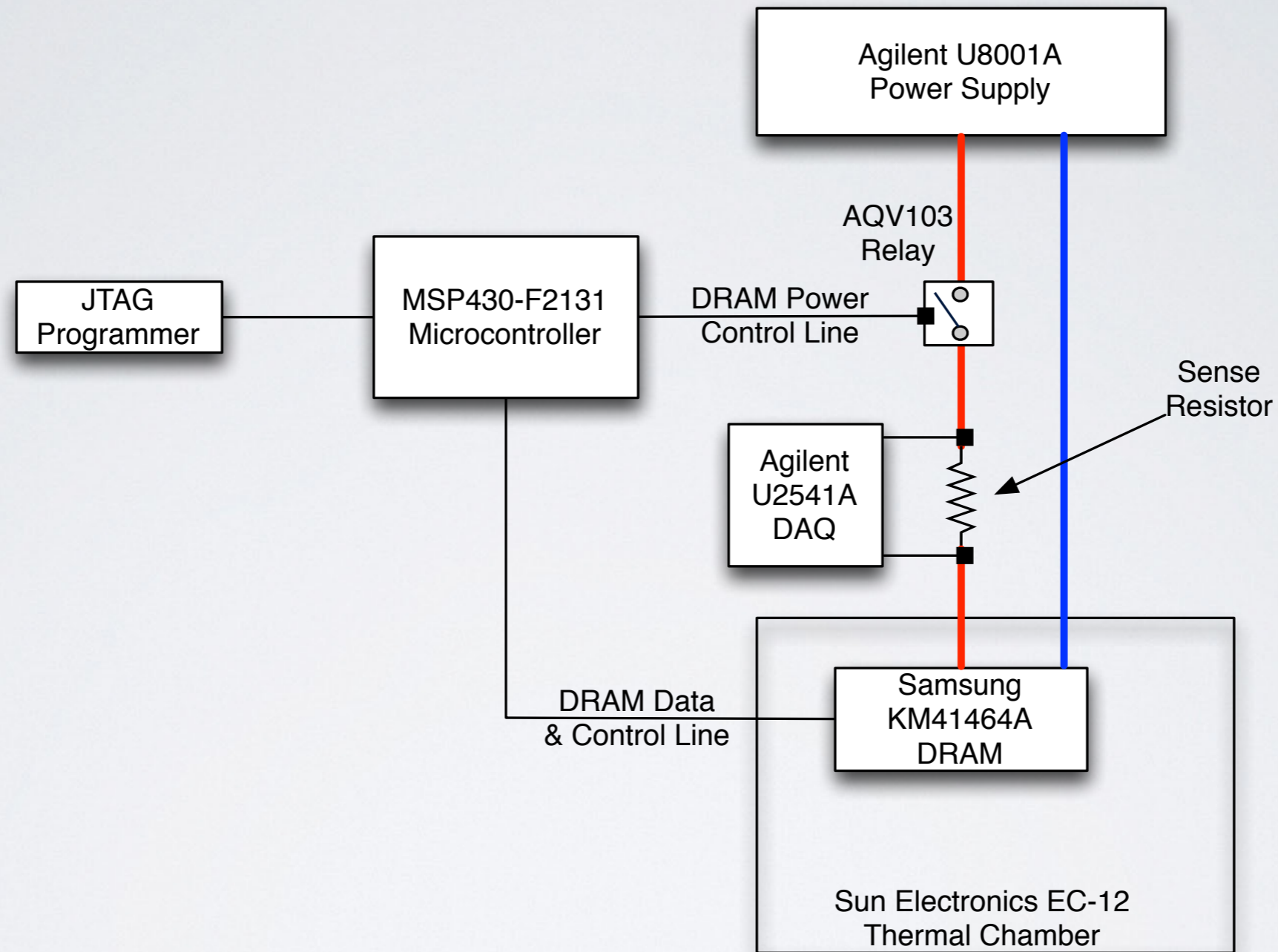
DRAM Refresh

- Probabilistic memory

- Energy vs. accuracy trade-off

- Mathematical models of disparate systems

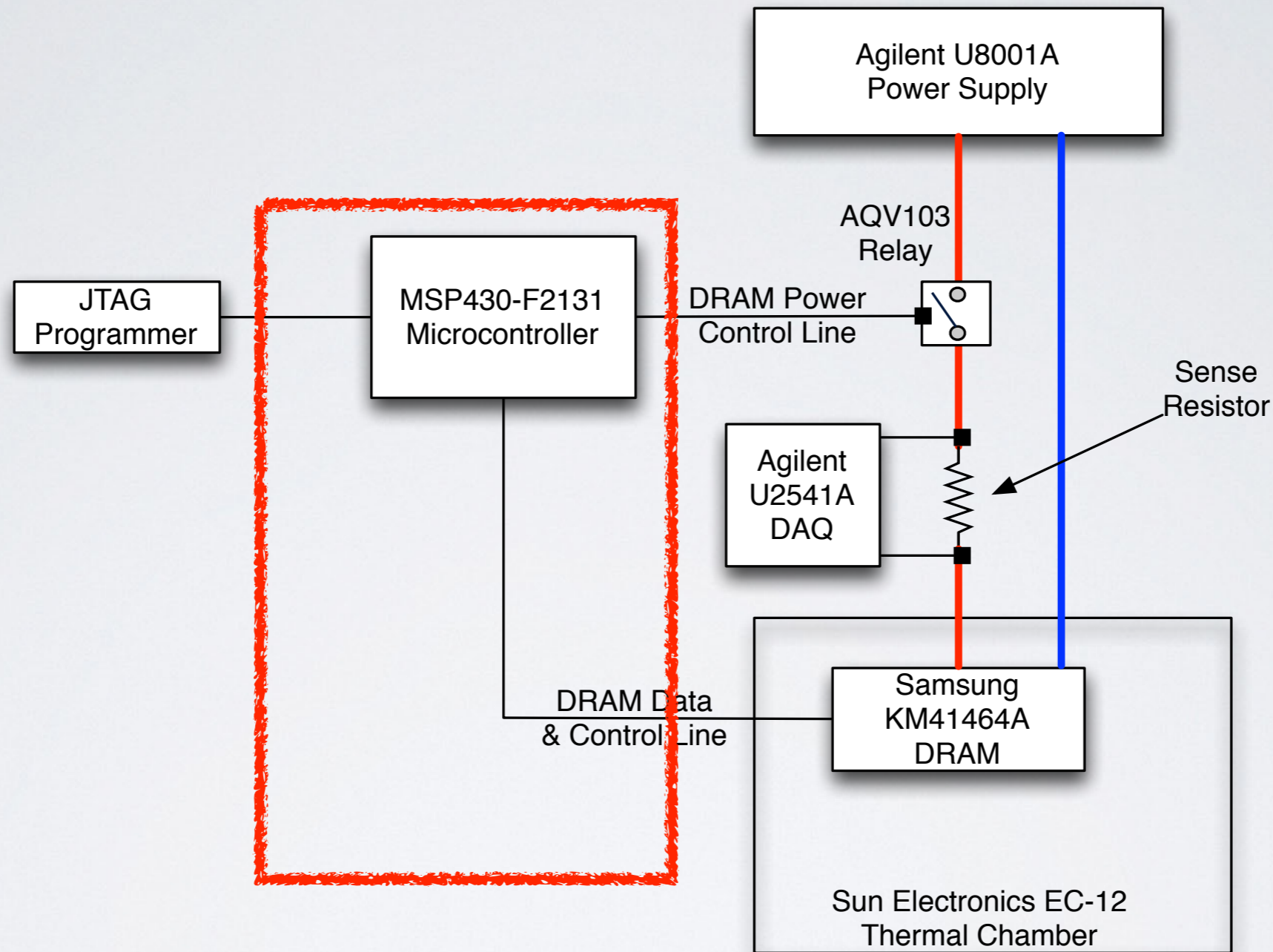# Our Goal

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- Implement a reproducible platform

- Reproduce key experiments

- Reanalyze previous proposals
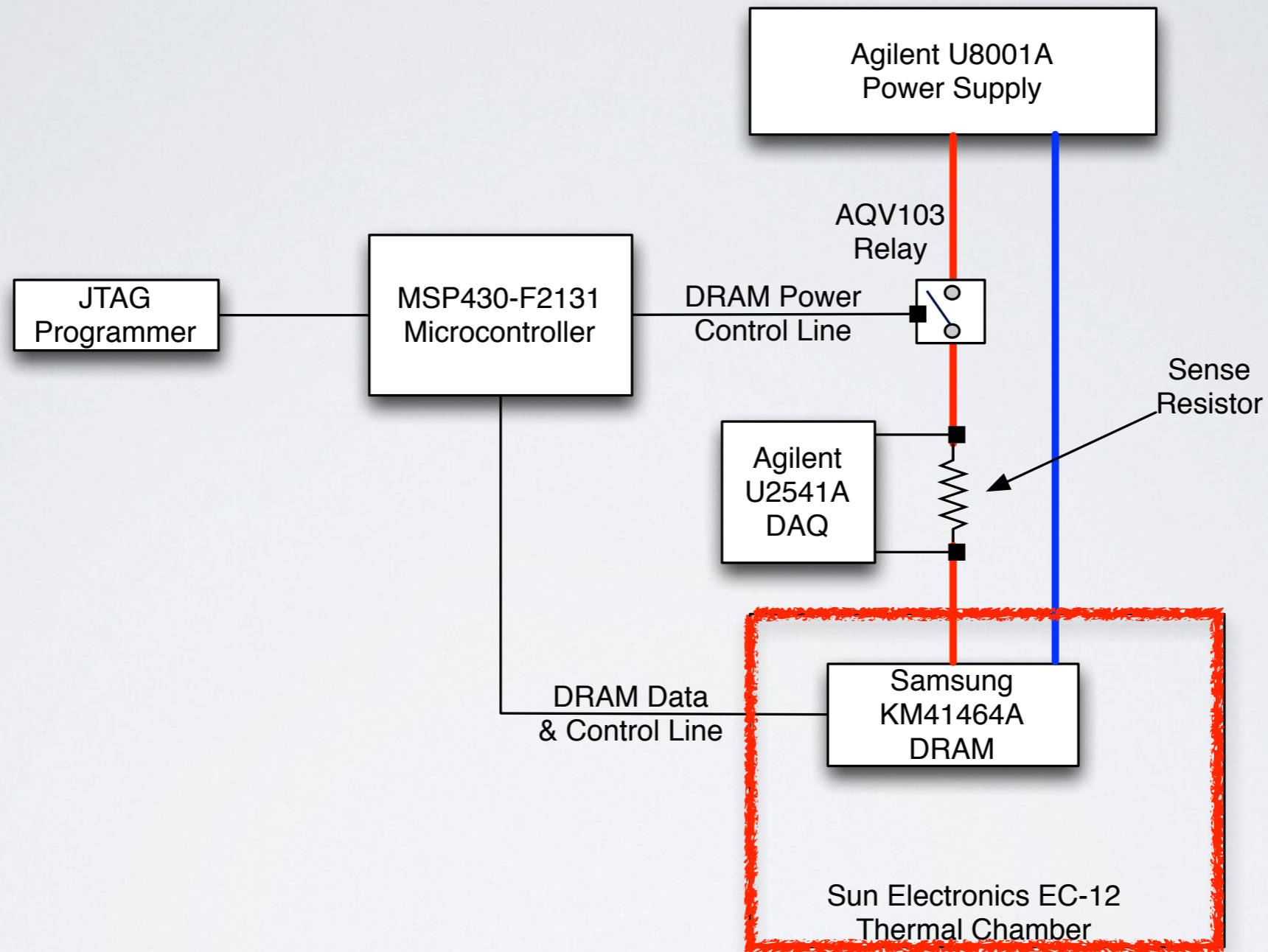
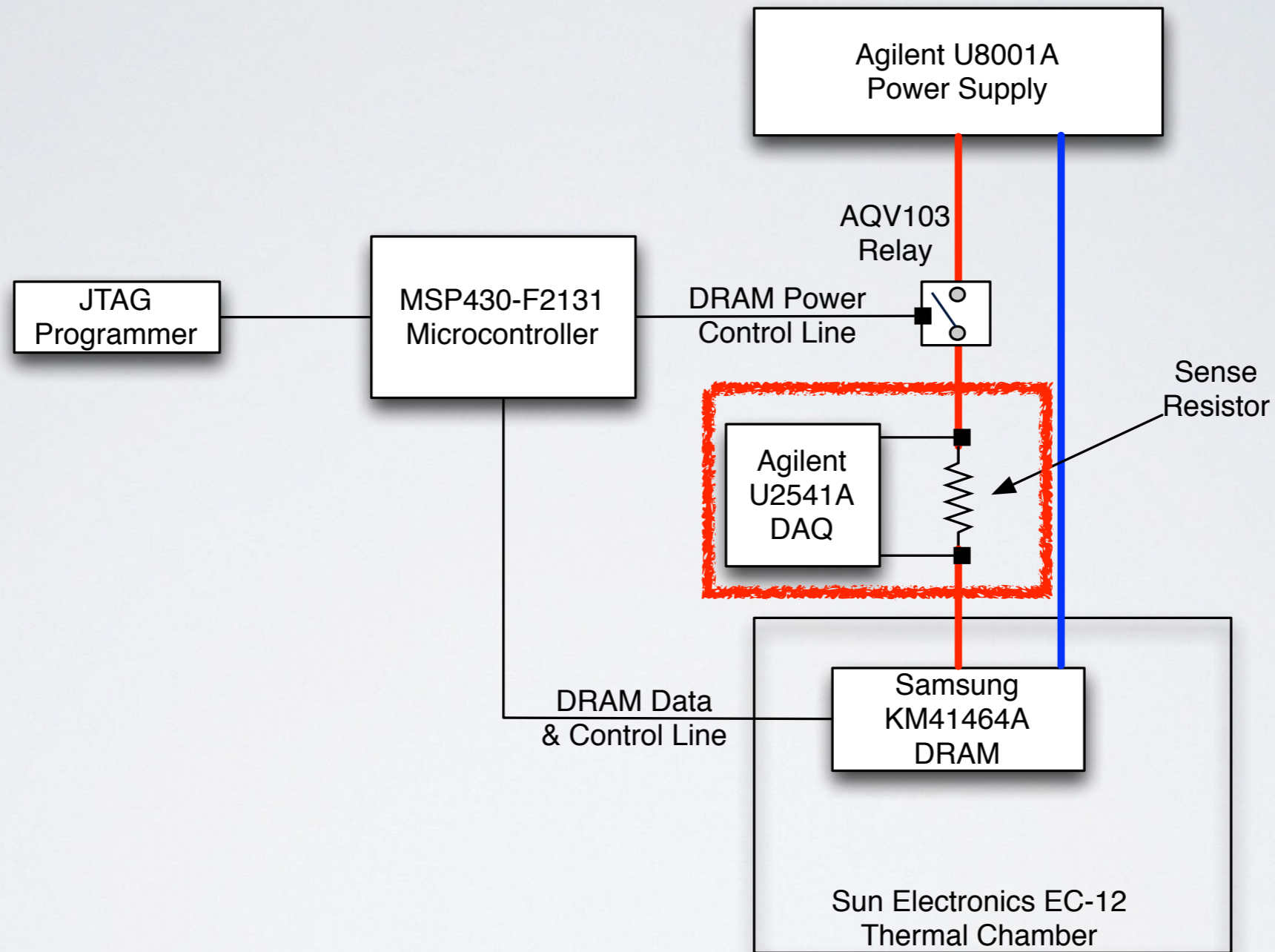# Experimental Platform

Experimental Platform

Fine grain control over memory

Experimental Platform

Controlled environment

Experimental Platform

Agilent U8001A
Power Supply

AQV103
Relay

JTAG
Programmer

MSP430-F2131
Microcontroller

DRAM Power
Control Line

Sense
Resistor

Agilent
U2541A
DAQ

DRAM Data
& Control Line

Samsung
KM41464A
DRAM

Sun Electronics EC-12
Thermal Chamber

Power measurements

Experimental Platform

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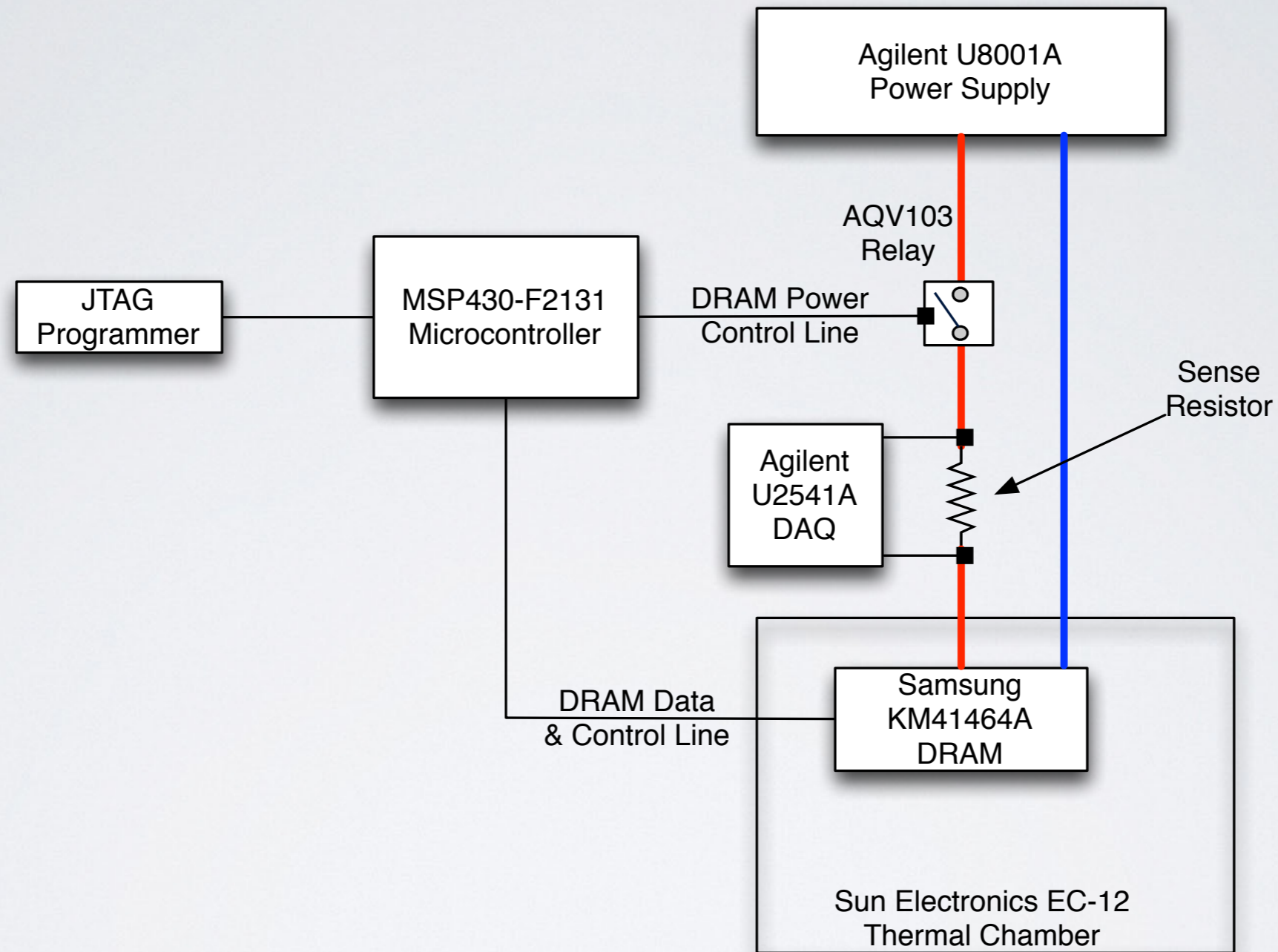Power Supply

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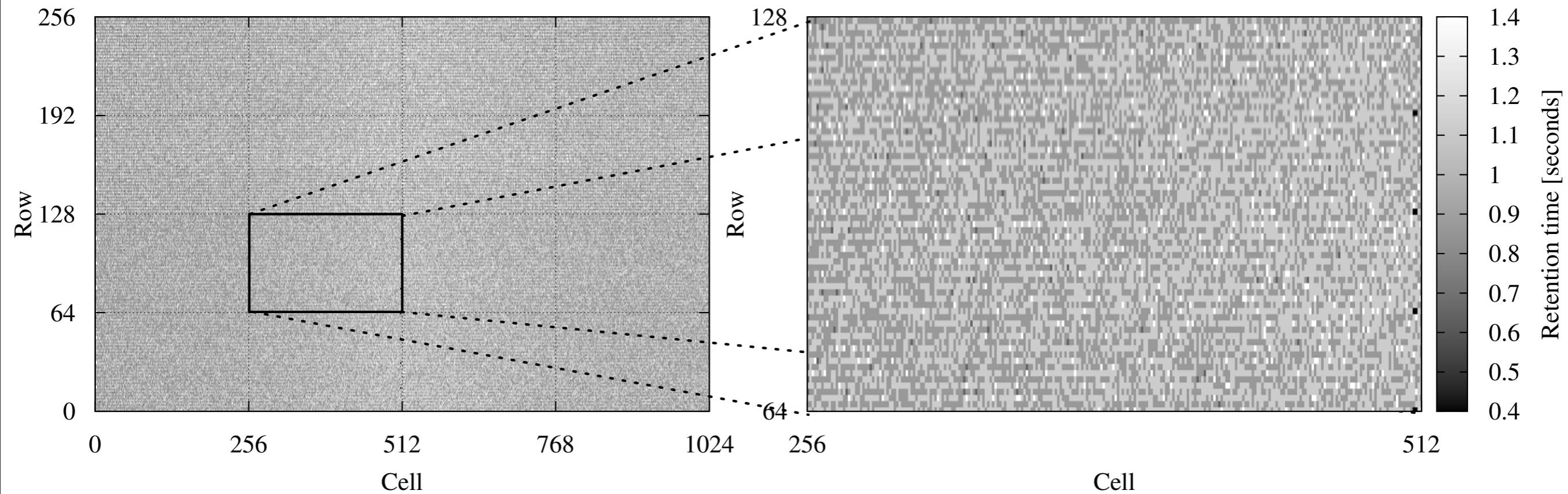
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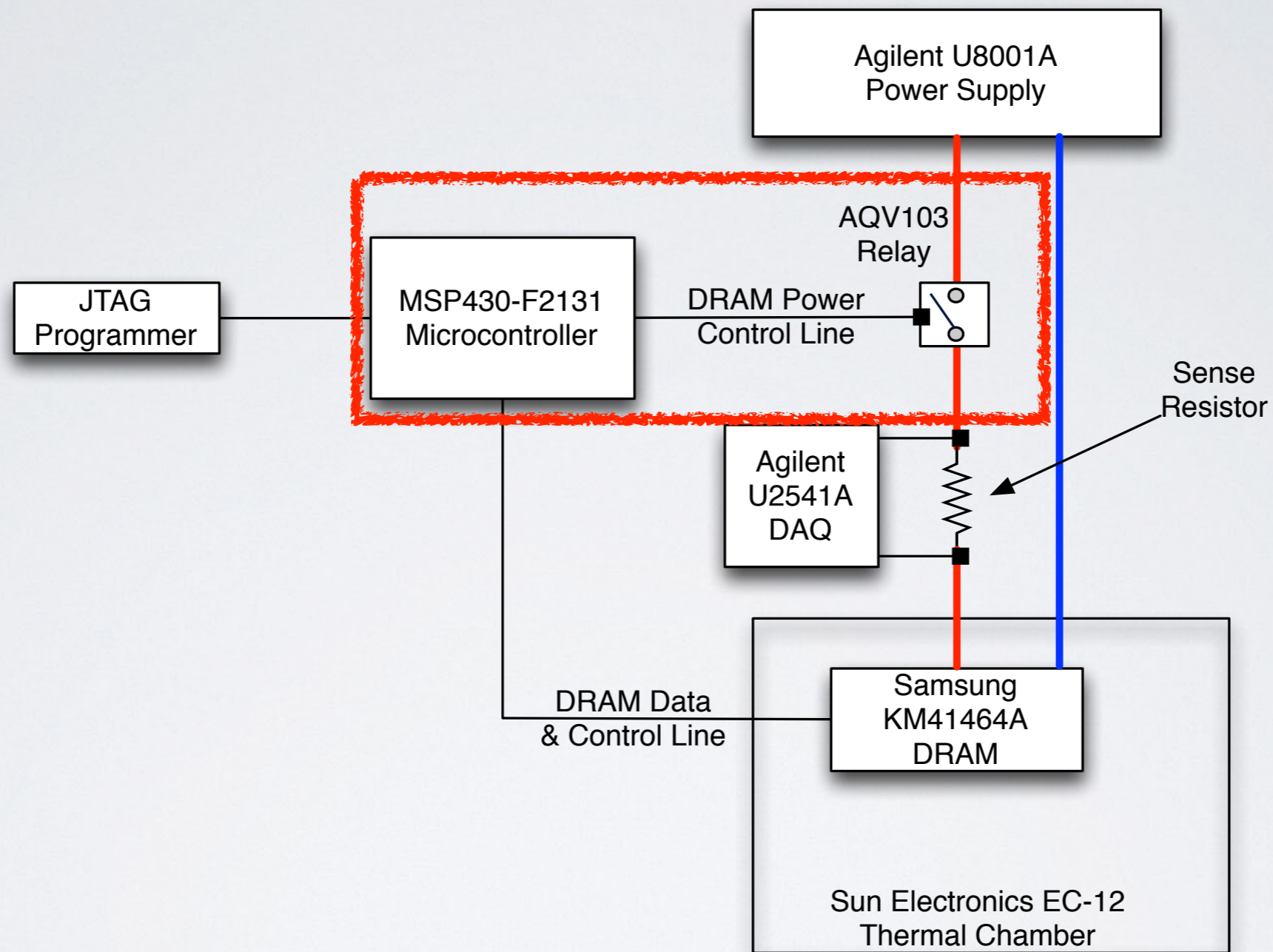
Power-gating

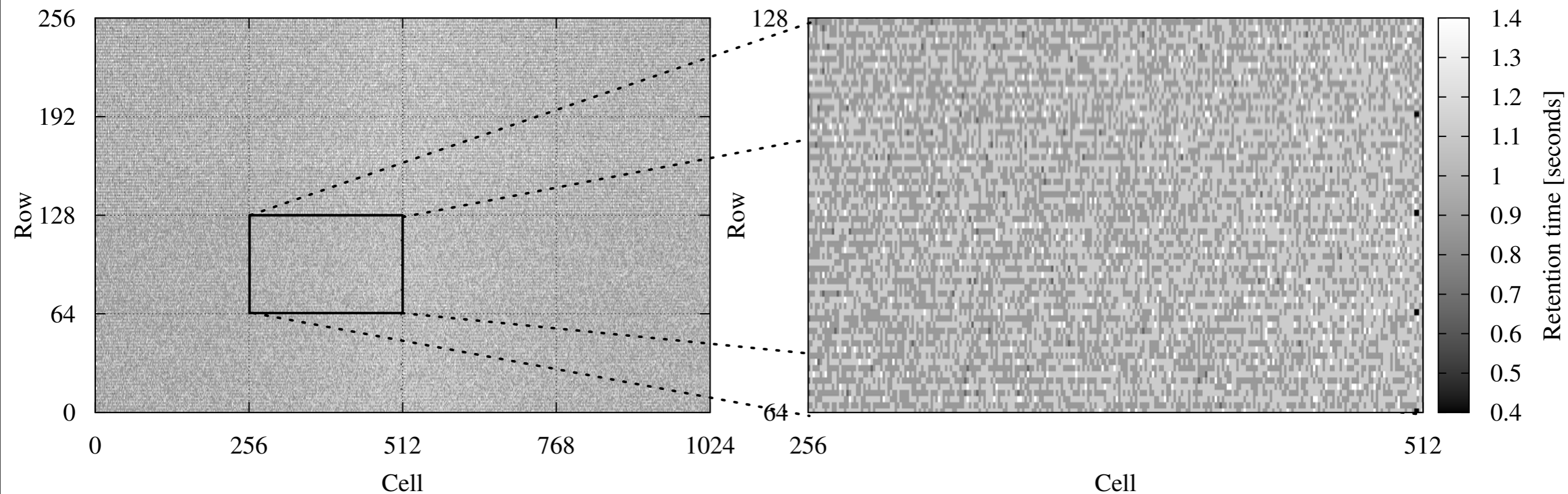# Experimental Platform

Spacial Locality

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Partitioning or isolating volatile cells
require per-cell control

Power Consumption

Mode	Avg. Current Draw	Avg. Power Usage
Refresh	$2.6mA$	$11.65mW$
Idle	$2.0mA$	$9.20mW$

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- Refresh: 4.5% - 8% of idle time
- 0.5% - 1% power saving on **complete** elimination of refresh

Conclusion

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Modeling based on
disparate platforms
leads to ambiguous evaluation