

DESIGN AND IMPLEMENTATION OF MEMRISTOR BASED 11T-SRAM

**A Project Report submitted in partial fulfilment of the requirement for the award of the
degree of**

BACHELOR OF TECHNOLOGY

IN

**ELECTRONICS AND COMMUNICATION
ENGINEERING**

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CERTIFICATE

This is to certify that the Project entitled "**Design and implementation of memristor based 11T-SRAM**" is being submitted by **GANISETTI NARENDRA SAI (21PA1A0448), DOLA DILEEP (21PA1A0445), DHANANI TARUN (21PA1A0443), ALAPATI DHANA MADHU (21PA1A0408), BOLISETTY SAI KRISHNA RAJA (20PA1A0417)** in partial fulfilment for the award of the degree of **Bachelor of Technology in Electronics and Communication Engineering** is a record of Bonafide work carried out by them under my guidance and supervision during academic year 2024–2025 and it has been found worthy of acceptance according to the requirements of the university.

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LIST OF ACRONYMS

CAD	Computer-Aided Design
CMOS	Complementary Metal-Oxide Semiconductor
DRAM	Dynamic Random-Access Memory
IC	Integrated Circuit
LTspice	Linear Technology Simulation Program with Integrated Circuit Emphasis
MLC	Multi-Level Cell
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
M1-M11	Transistors
NVM	Non-Volatile Memory
RSNM	Read Static Noise Margin
SNM	Static Noise Margin
SRAM	Static Random-Access Memory
STT-MRAM	Spin-Transfer Torque Magnetic RAM
VDD	Supply Voltage
VLSI	Very Large-Scale
WSNM	Write Static Noise MarginN

LIST OF NOTATIONS

ns	Nanoseconds (10^{-9} Joules)
.meas	Measurement directive in SPICE simulation
V or DD	Voltage
pj	Picojoule (10^{-12} Watts)
RSNM	Read Static Noise Margin
SNM	Static Noise Margin
S	Seconds
T	Pulse duration
WSNM	Wire Static Noise Margin
I	Current
$I(V)$	Current through voltage source V
V	Transistor
μw	Microwatt (10^{-6} Watts)
tPLH	Propagation Delay (Low to High)
tPHL	Propagation Delay (High to Low)
.tran	Transient Analysis

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ABSTRACT

The design of an 11T SRAM cell focuses on achieving enhanced stability, power efficiency, and reliable read/write operations compared to conventional SRAM designs. The core architecture consists of six transistors forming a cross-coupled inverter pair for stable data storage, complemented by five additional transistors to decouple read and write operations. This separation ensures non-destructive read operations, minimizes disturbances on storage nodes, and improves the overall stability of the memory cell. The write operation is facilitated by two access transistors controlled by the word line (WL), enabling data transfer between the bit lines (BL and BLB) and the storage nodes. The read path is distinct, involving transistors connected to the read bit line (RBL) and controlled by a separate read word line (RWL). This design decision reduces the risk of voltage fluctuations and enhances read stability by isolating the storage node during read operations.

Memristor-based SRAM can achieve faster switching times and lower power consumption while maintaining compact size, making it a promising candidate for next-generation memory technologies. Despite the challenges of switching speed, wear-out issues, and integration with existing CMOS circuits, the potential benefits of memristor-based memory are considerable, especially in emerging fields like embedded systems, the Internet of Things (IoT), and neuromorphic computing. This work discusses the architectural design, potential advantages, challenges, and application scenarios, emphasizing the transformative role memristors could play in the evolution of memory technology.

KEYWORDS: Efficiency, Embedded Systems Memristor-based Memory, Embedded Systems, IOT, Neuromorphic Computing, Power, Stability, 11T-SRAM,

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CHAPTER 1

INTRODUCTION

1. INTRODUCTION

1.1 Static Random-Access Memory (SRAM):

Static Random-Access Memory (SRAM) is a type of volatile semiconductor memory that stores data using bistable latching circuitry. Unlike Dynamic RAM (DRAM), which requires periodic refreshing to retain data, SRAM maintains its stored information as long as power is supplied. This makes SRAM significantly faster and more efficient in read and write operations, making it an essential component in applications requiring high-speed data access, such as cache memory in processors, networking devices, and AI accelerators. However, SRAM's advantages come at the cost of increased silicon area and higher power consumption per bit due to its complex circuit design.

1.2 SRAM Cell Design and Configurations

The basic unit of SRAM is the memory cell, which is commonly designed using six-transistor (6T), eight-transistor (8T), ten-transistor (10T), eleven-transistor (11T), or twelve-transistor (12T) topologies. The most widely used configuration, the 6T SRAM cell, consists of two cross-coupled inverters forming a bistable latch and two access transistors that control read and write operations. While 6T SRAM is efficient in terms of speed and stability, alternative designs like 8T, 10T, 11T, and 12T offer improved noise immunity, reduced leakage power, and enhanced read/write performance, particularly for ultra-low-power and high-performance applications. SRAM operates at significantly lower latency compared to DRAM, making it ideal for L1, L2, and L3 cache memory in CPUs and GPUs, where rapid data retrieval is crucial.

1.3 11T SRAM: Enhancing Performance and Power Efficiency

The 11T SRAM cell, as illustrated in Figure 1.1, is an advanced memory design that enhances power efficiency and read stability while maintaining high-speed access. This figure shows the structural layout of the 11-transistor configuration, which incorporates additional transistors compared to the conventional 6T design. These extra transistors help mitigate read disturbance issues and improve noise immunity. The 11T configuration includes separate read and write ports, as shown in the figure, which significantly reduces the risk of read failure and enables lower voltage operation—making it an ideal choice for energy-efficient applications.

This design is particularly beneficial in ultra-low-power embedded systems, AI accelerators, and biomedical electronics, where energy efficiency and data reliability are critical. As

demonstrated in Figure 1.1, the cell structure minimizes leakage currents, making it suitable for deep submicron and nanoscale technologies where power constraints are stringent. As SRAM technology continues to evolve, the 11T variant is gaining attention for applications that require a careful balance between performance, stability, and energy efficiency.

One of the major advantages of SRAM, highlighted by the 11T design, is that it does not require refresh cycles like DRAM. This simplifies operation and results in lower power consumption during active read/write processes. However, the trade-off is that each SRAM cell—especially with an 11-transistor layout—requires more area, making it less dense and more costly than DRAM. Consequently, SRAM is commonly used for cache memory rather than as main memory. Despite this, it remains widely employed in high-speed computing, microcontrollers, networking equipment, biomedical applications, and AI accelerators, where performance and reliability are prioritized over cost and density.

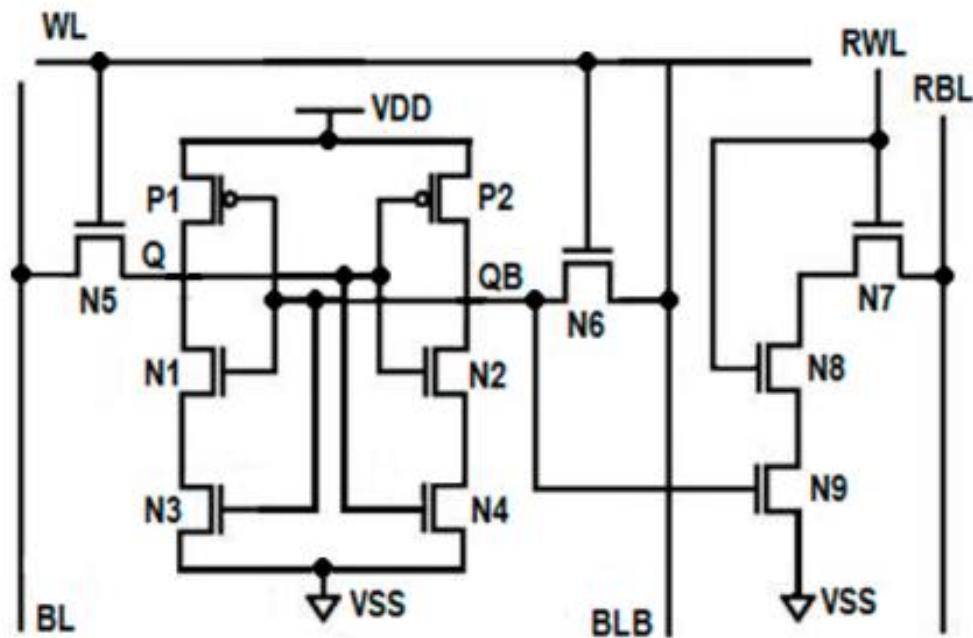


Fig 1.1 11T-SRAM

1.4 Memristors: A Revolutionary Circuit Element

A Memristor (memory resistor) is a fundamental passive circuit element, as shown in Figure 1.2, which illustrates its standard symbol. Unlike traditional resistors with fixed resistance, memristors exhibit memory-dependent resistance, meaning they can retain their resistance state even after power is removed. This non-volatility makes them highly valuable for modern

memory applications.

Memristors function by changing their resistance in response to the magnitude and polarity of an applied voltage or current. This behavior, symbolized in Figure 1.2, enables them to store and process information similarly to synaptic connections in the human brain, positioning them as promising components for neuromorphic computing and AI. In addition to their brain-like processing ability, memristors offer advantages in power efficiency, high-speed data processing, and reduced circuit complexity, making them a central focus in next-generation semiconductor technology research.

These devices are being actively explored in domains like resistive RAM (ReRAM), where they serve as the core storage element. Their capability to retain data non-volatilely while supporting high-speed operations positions them as potential alternatives to traditional DRAM and Flash memory. Moreover, memristors are gaining momentum in ultra-low-power computing applications, such as edge AI devices, biomedical electronics, and in-memory computing architectures, where they help overcome limitations of conventional memory systems.

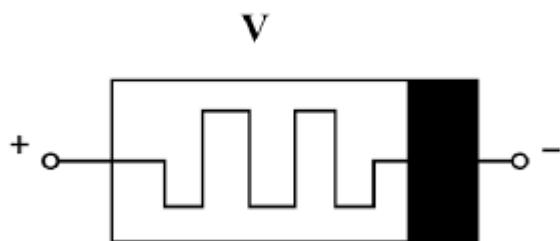


Fig 1.2 Memristor Circuit Diagram

1.5 Applications and Advancements in SRAM Technology

In modern semiconductor design, researchers focus on optimizing SRAM for power efficiency, stability, and reduced leakage currents, especially in deep submicron and nanoscale technologies. Emerging SRAM architectures, including FinFET-based and GDI (Gate Diffusion Input) logic-based SRAMs, are being developed to address challenges related to power and area efficiency. As the demand for high-performance computing and AI-driven applications continues to grow, advancements in SRAM technology play a crucial role in shaping the future of memory design. Over the years, many types of SRAM have been developed with different designs and to suit different applications. The most common type is

binary SRAM, where a memory cell stores a bit in one of two binary states: 0 or 1. This SRAM is best for applications that require low latency and fast data access. Ternary SRAM stores three states per cell, providing higher data density and more efficient read/write operations. SRAM is also available in synchronous and asynchronous variants. Synchronous SRAM is synchronized to the system clock, whereas asynchronous SRAM works out of sync with the system clock. The former is suitable for high-speed digital signal processing in digital communications and other applications where data timing must be precisely coordinated between SRAM and the system clock. The latter is best for high-speed applications. Quad data rate SRAM is a specific type of synchronous SRAM that provides high speed and efficiency by synchronizing data access with the rising and falling edges of the system clock signal. Low-power SRAM is also available. This type of SRAM consumes less power than other types, particularly in active and standby modes. It is suitable for portable devices where such modes are common occurrences.

1.6 Advantages of SRAM

Speed is the biggest advantage of SRAM. As long as power is supplied, SRAM retains data. Also, since it does not require time-consuming refresh cycles, SRAM enables fast data access and offers lower latency. Those two qualities make SRAM ideal for applications where speed is essential. Data integrity is another area where SRAM has an advantage over some other memory types. The integrity of data is consistently maintained because SRAM does not use capacitors and, again, because it does not require constant refreshing. Modern SRAM is now available that uses techniques like power gating and dynamic voltage scaling. As a result, it consumes less power -- both in active and standby modes -- making it more energy-efficient than its predecessors. Even so, SRAM is best suited for applications where power efficiency is less of a priority than high access speeds and responsiveness -- ideally real time -- low latency and data integrity.

Additionally, SRAM offers exceptional endurance compared to other memory technologies, such as NAND Flash, which has a limited number of program/erase cycles. Since SRAM does not rely on wear-prone components, it is highly reliable and durable, making it ideal for mission-critical applications, including aerospace, medical devices, and industrial automation. Furthermore, its low latency and deterministic performance make it an optimal choice for real-time systems, where predictability in data retrieval and processing is essential. These advantages reinforce SRAM's role as a key memory technology in high-performance and low-power computing environments.

1.7 Summary

Static Random-Access Memory (SRAM) is a type of volatile memory that stores data using bistable latching circuitry, enabling it to retain information without the need for refreshing, as long as power is continuously supplied. This feature provides SRAM with significantly lower latency and faster access speeds compared to Dynamic RAM (DRAM), making it ideal for performance-critical applications such as processor cache memory, AI accelerators, networking devices, and embedded systems.

SRAM cells come in several configurations, including 6T, 8T, 10T, 11T, and 12T designs. Each configuration presents a trade-off between area, power consumption, and stability. The 11T SRAM cell, for instance, adds extra transistors to improve read reliability, minimize noise, and reduce leakage currents—making it particularly suitable for ultra-low-power and high-performance applications. These improvements are essential in modern electronics, especially as devices shrink in size and demand more efficient memory solutions.

Alongside SRAM, memristors represent a revolutionary class of circuit elements that retain their resistance based on historical voltage or current, even when power is off. This unique ability allows memristors to act as non-volatile memory, storing data persistently with minimal power usage. Because they mimic biological synapses, memristors are also considered promising for neuromorphic computing and artificial intelligence, offering compact, energy-efficient solutions for future memory and logic systems.

Technological advancements in SRAM, including the use of Fin FETs and GDI (Gate Diffusion Input) techniques, aim to improve its power efficiency, area optimization, and stability. Moreover, variants like synchronous, asynchronous, quad-data-rate, and low-power SRAM are designed to cater to specific needs across different applications.

SRAM stands out for its speed, low latency, high data integrity, and resistance to soft errors. These characteristics make it a preferred choice in systems where real-time responsiveness and reliability are more important than memory density or cost. As digital technologies continue to evolve, both SRAM and memristor technologies play a crucial role in shaping the future of computing and memory architectures.

CHAPTER 2

LITERATURE SURVEY

2. LITERATURE SURVEY

In relevance to SRAM and memristor-based memory systems, a brief review of existing technologies has been conducted. The following sections highlight key developments and approaches in volatile and non-volatile memory designs, providing context for current advancements.

2.1 Literature Review

Static Random-Access Memory (SRAM) has been a critical component in modern memory technology, offering high-speed data access with low latency for applications like processor caches, AI accelerators, and embedded systems. While traditional SRAM cell designs, such as 6T, 8T, and 10T configurations, provide efficient operation, they encounter challenges like stability degradation, half-select problems, and power leakage [1][2][3]. To address these challenges, researchers have proposed alternative topologies that aim to enhance noise immunity, improve read/write performance, and reduce power consumption.

One notable advancement is the Schmitt Trigger-based 9T SRAM design [1][4], which effectively mitigates noise disturbances and enables near-threshold voltage operations. This architecture improves power efficiency while maintaining operational reliability, making it ideal for low-power devices. Similarly, the standard 8T SRAM cell [2][9][14][17] employs decoupled read and write paths and differential writing modes, optimizing memory stability and reducing leakage currents. These designs demonstrate significant improvements over conventional 6T cells [3][8], particularly in nanoscale technologies.

The conventional C6T SRAM cell [3] is widely adopted for high-speed computing applications due to its simple design and rapid data access capabilities. However, studies highlight its limitations in terms of process variation sensitivity and read/write conflicts, prompting the development of advanced configurations. Researchers have introduced variability-resilient designs like the E2VR11T SRAM cell [5][6], which integrates dedicated read/write paths to improve stability and reduce power consumption during memory operations.

Process variations in deep submicron technologies have posed significant challenges to conventional SRAM architectures, limiting operational stability and scalability. For example, the 10T SRAM cell [10][11][18] addresses these concerns by incorporating robust transistor

layouts that minimize leakage currents and enhance noise margins. Additionally, high-performance configurations like the 12T SRAM cell [23] are designed for applications requiring enhanced reliability and stability in high-speed environments. These architectures exhibit superior metrics for read/write stability and noise immunity, making them suitable for critical applications like edge computing and biomedical systems [24].

An emerging trend in SRAM technology is the integration of memristors into conventional designs, offering transformative benefits for next-generation memory systems. Memristor-based SRAM [7][19][20] leverages resistive-switching properties to achieve non-volatility, enabling data retention even during power loss. Unlike conventional SRAM, which relies on charge-based storage mechanisms, memristors dynamically adjust resistance based on applied voltage, optimizing power usage and reducing leakage currents [13][21][22]. This makes memristor-based designs particularly valuable for power-sensitive applications such as IoT devices and neuromorphic computing.

Hybrid CMOS-memristor architectures blend the high-speed operation of traditional SRAM with the energy-efficient and non-volatile properties of memristors. For instance, adding two memristors to the VDD power supply enables dynamic voltage regulation, minimizing unnecessary power dissipation [6]. Expanding this to four memristors distributes the load evenly, further reducing power wastage and enhancing stability in larger SRAM arrays [16][17]. These advancements ensure scalability and efficiency, addressing the challenges posed by shrinking transistor dimensions in nanoscale technologies.

2.2 SUMMARY

The literature explores the evolution of SRAM cell architectures, addressing limitations in conventional designs and highlighting innovations for enhanced performance and energy efficiency. The traditional 6T SRAM cell is widely used for its simplicity and speed but suffers from stability issues and leakage in nanoscale technologies. To overcome these, advanced designs such as 8T, 9T, 10T, 11T, and 12T cells have been proposed.

The 8T SRAM improves read stability by decoupling read/write paths, while the 9T Schmitt Trigger-based design enhances noise immunity and supports near-threshold operation. The 10T and 12T SRAM configurations focus on robustness against process variations, improving read/write margins and reliability for high-speed and low-voltage operations.

Emerging research emphasizes memristor-based SRAM, integrating resistive switching elements to achieve non-volatility, reduced leakage, and dynamic power regulation. Hybrid CMOS-memristor architectures offer significant promise in ultra-low power applications such as IoT devices, AI accelerators, and biomedical electronics, combining the speed of SRAM with the efficiency of memristors.

These advancements reflect a trend toward power-aware, scalable, and reliable memory designs suitable for next-generation computing needs.

CHAPTER 3

DESIGN AND IMPLEMENTAION OF

MEMRISTOR BASED 11T SRAM

3.1 Existing Methodology: Design of 11T SRAM

The proposed methodology for designing the 11-transistor (11T) SRAM cell centers around achieving a balance between high performance and low power consumption. The initial stage involves defining functional goals such as improved read stability, enhanced write efficiency, and minimized power usage. These requirements guide the selection and layout of transistors to form a stable and reliable memory cell that functions effectively under low power conditions. Figure 3.1 illustrates the schematic of the 11T SRAM cell, highlighting the arrangement of transistors including the core inverters and separate read/write paths.

At the core of the 11T SRAM cell are six transistors arranged in a cross-coupled inverter configuration. This fundamental structure is responsible for robust and stable data storage. In addition to the core six, five auxiliary transistors are strategically incorporated to provide separate read and write access paths, which greatly enhance operational reliability. Dedicated transistors for read and write operations ensure non-destructive reads and efficient data writing without compromising internal node integrity.

The read mechanism involves an independent read word line (RWL) and read bit line (RBL), completely separated from the write path. This separation eliminates read-disturb issues, a common problem in traditional SRAM architectures. During read operations, only specific transistors are activated, thereby reducing power consumption and avoiding any disturbance to the stored data.

To further optimize the design, efforts are made to minimize leakage and dynamic power through careful transistor sizing and strategic circuit architecture. These features make the 11T SRAM well-suited for energy-sensitive applications such as mobile devices, IoT systems, and wearable electronics. Ultimately, the 11T SRAM architecture ensures high stability, reduced power consumption, and reliable memory performance.

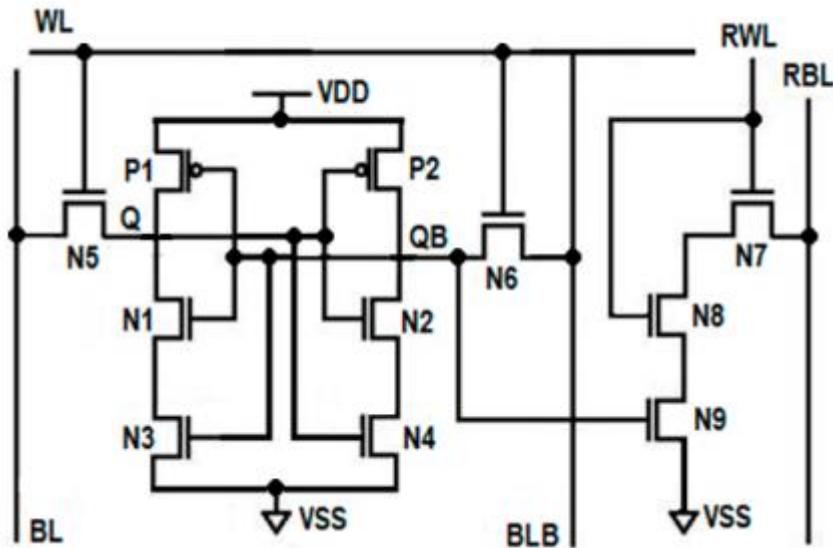


Fig 3.1: Schematic of 11T SRAM Cell depicting core cross-coupled inverters and separate read/write paths.

3.2 Limitations of Conventional 11T SRAM

Increased Area: The integration of additional transistors expands the footprint of each memory cell, making it less area-efficient than traditional 6T SRAM designs. This increased area is a limitation in scenarios demanding high-density memory integration.

Design Complexity: The additional transistors increase circuit complexity, requiring intricate routing and extended design cycles. This complexity also makes verification and layout processes more challenging.

Higher Manufacturing Costs: The complexity and increased component count result in higher fabrication costs, limiting its cost-efficiency for large-scale applications.

Reduced Fabrication Yield: The more complex the architecture, the greater the risk of defects during manufacturing, leading to lower production yields and scalability challenges.

3.3 Memristor Technology and Integration

Memristors, theorized by Leon O. Chua in 1971, are the fourth fundamental passive circuit element alongside resistors, capacitors, and inductors. They are defined by a unique relationship between magnetic flux (Φ) and electric charge (q), characterized by memristance (M), with the unit of Ohm. Memristors are known for their non-volatility, scalability, fast

read/write cycles, and CMOS compatibility, making them ideal for low-power memory desi

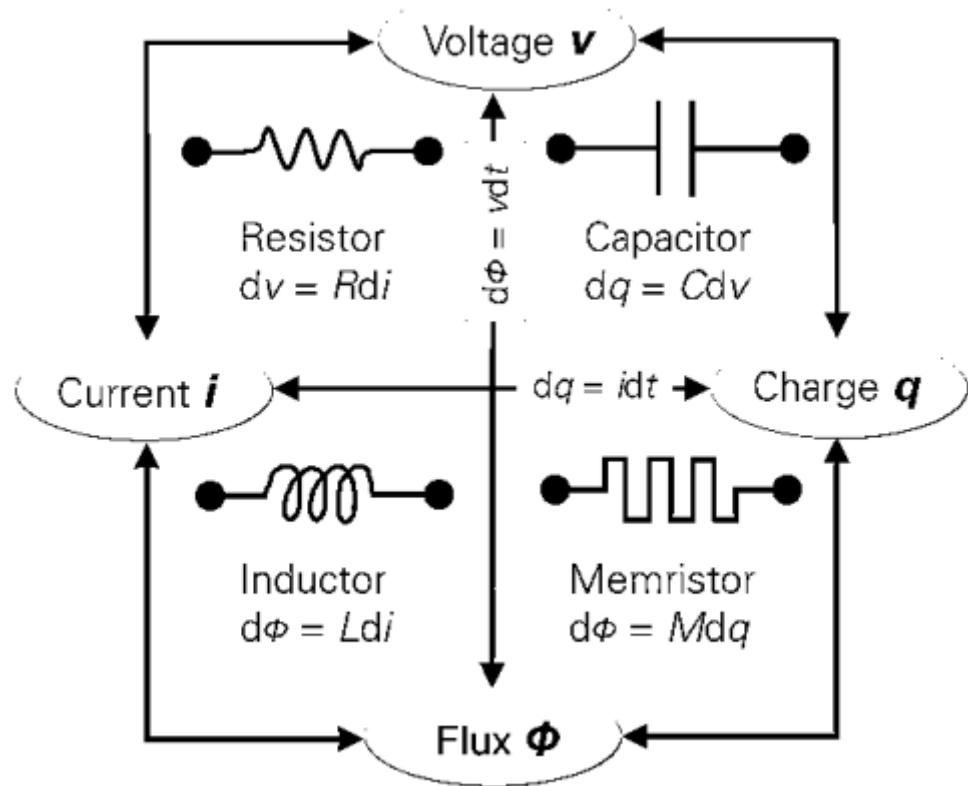


Fig 3.2: Symbolic Representation of Memristor Behavior

Memristor is characterized as a two terminal non-volatile device in which the magnetic flux (Φ) between the terminals is an element of the measure of electric charge (q) that has gone through the device and it is indicated by M and its unit is ohm. Memristor has non-volatile, fast read/write time, good scalability and compatibility with CMOS technology over the simple SRAM as shown in Figure 3.2. These advantages of Memristor help in the design of low power SRAM.

3.3.1 Memristor's Impact on SRAM Power Supply

When incorporated into the power supply line, memristors can dynamically adjust resistance, effectively optimizing the voltage and current delivered to the SRAM. This dynamic adjustment allows for better energy management and reduced power consumption.

3.3.2 Reduction in Power-Delay Product

By reducing energy loss during idle and active states, memristors contribute to lowering the power-delay product (PDP). This makes memory systems more efficient and responsive, enhancing performance in time-sensitive applications

3.4 Suggested Methodology: Design and Implementation of 2-Memristor Based 11T SRAM

The 2-memristor-based 11T SRAM cell integrates two memristive devices into the traditional architecture, as shown in Fig. 3.3. These memristors are connected at the internal storage nodes of the cross-coupled inverters. This configuration allows the memory to retain its state even when power is off, providing non-volatile behavior.

During write operations, memristors switch between high and low resistance states, corresponding to logic values '0' and '1'. These resistive states enhance the stored logic at internal nodes, reinforcing data stability. Read operations utilize an isolated read path, maintaining data integrity without disturbances.

The use of memristors helps in minimizing leakage current and power dissipation. However, transistor sizing must be carefully optimized to align with memristor switching characteristics. This hybrid integration brings non-volatility to traditional SRAM while preserving its standard functionalities. Additionally, this implementation allows for fast read/write cycles and reduced standby power, extending its suitability to devices that experience intermittent power availability such as energy-harvesting or remote sensor nodes.

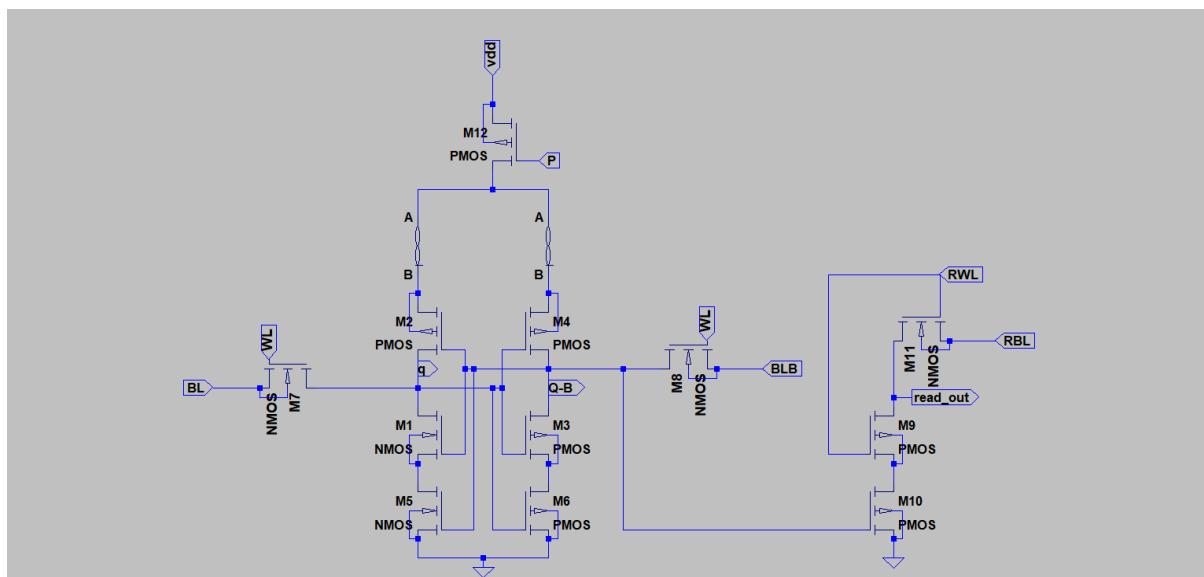


Fig 3.3: 2-Memristor Based 11T SRAM Cell Schematic

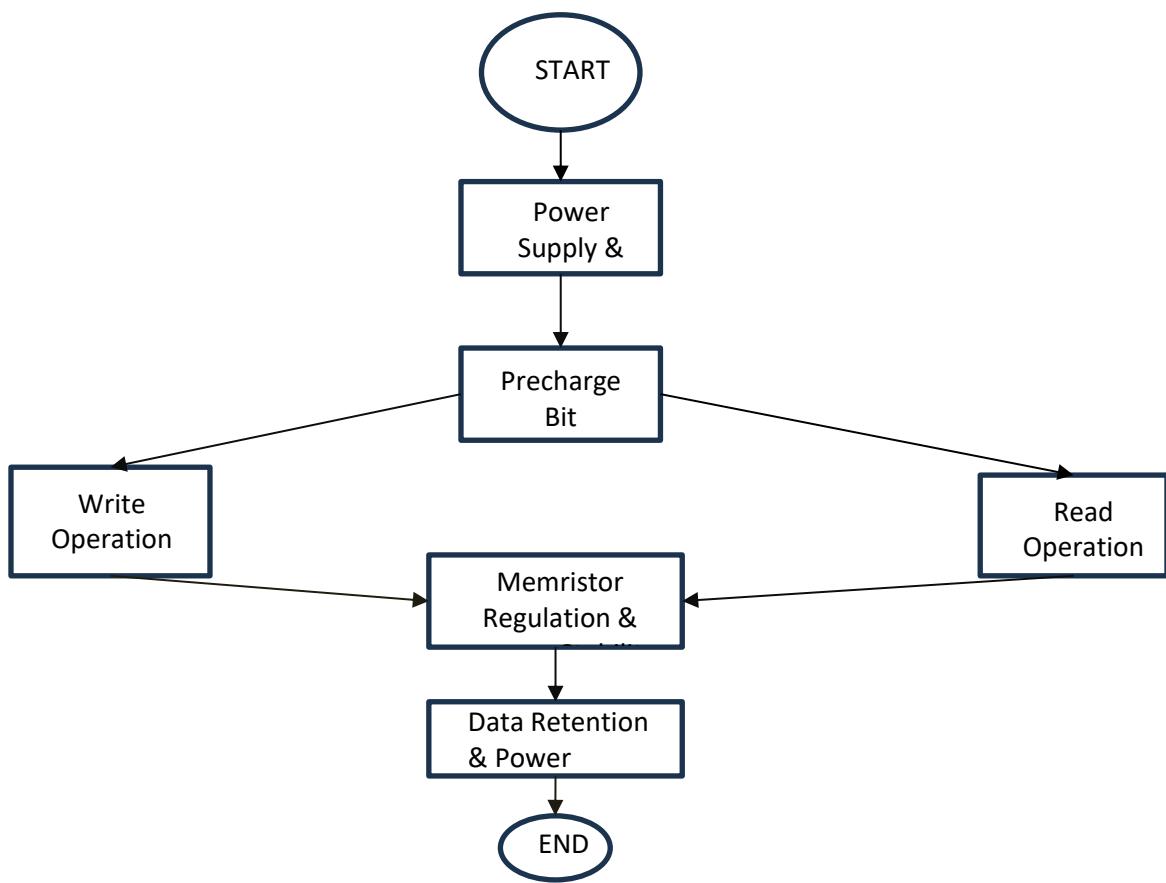


Fig 3.4: Flow chart architecture for 11TSRAM

Fig 3.4 Illustrate the architecture of 11TSRAMThe process begins with defining design objectives, such as reducing power consumption and enhancing performance. After constructing the SRAM cell schematic, simulations are performed to assess circuit behavior. Waveform analysis follows, focusing on power consumption and signal delays, with key metrics like average power and propagation delay (t_{PHL} , t_{PLH}) extracted. If the results are unsatisfactory, adjustments are made, such as altering transistor sizes or memristor placements. The design is then compared with existing SRAM architectures to evaluate improvements. The process concludes once an optimized and reliable design is verified.

3.5 Design and Implementation of 4-Memristor Based 11T SRAM

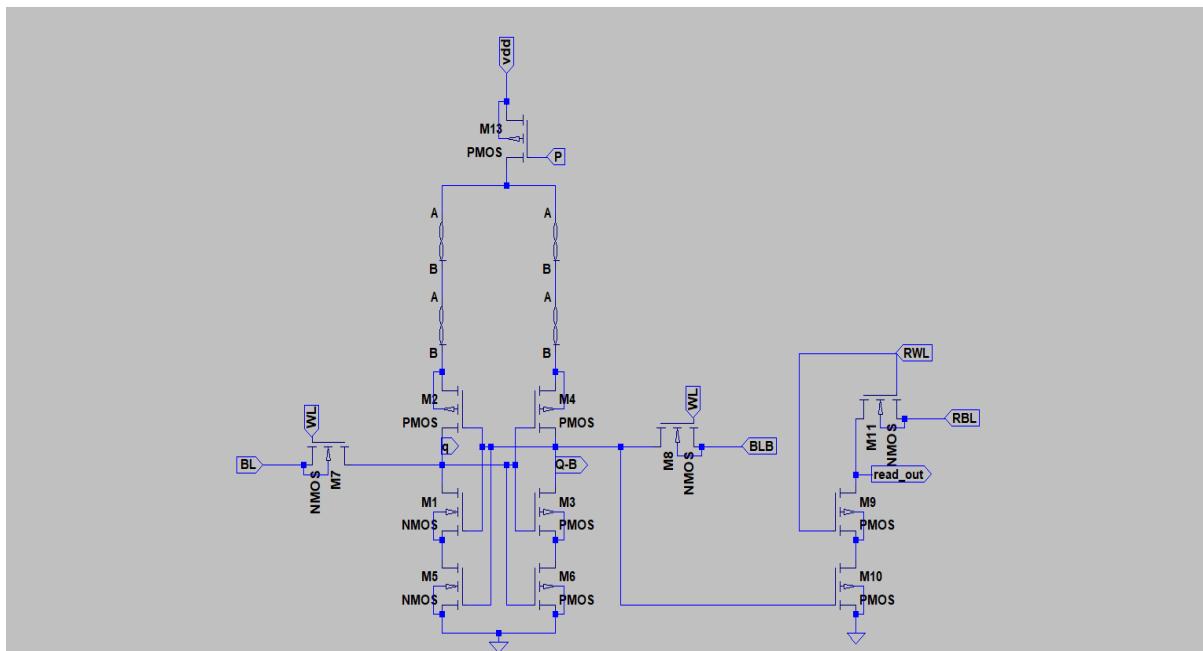
The 4-memristor-based 11T SRAM cell, as illustrated in Fig. 3.5, extends the design by incorporating memristors both at the storage nodes and access paths. Two memristors at the cross-coupled inverter nodes maintain non-volatile logic states. The other two, placed along the access transistors, regulate current flow during read/write operations, thus minimizing dynamic power loss.

This configuration supports improved access control, further isolation of read and write paths,

and better energy efficiency. It ensures stable data retention and robust read/write operations, even under variable power supply conditions. This makes it highly reliable in systems subject to voltage scaling or irregular power supply, such as battery-powered or remote devices.

Moreover, the addition of memristors to the access paths helps suppress sneak path currents and limits unnecessary power draw, thus contributing to reduced total power consumption. The enhanced control and non-volatile features make this architecture ideal for critical data storage in mission-critical systems, aerospace applications, or medical devices where data retention and fault tolerance are paramount.

Additionally, the use of four memristors introduces a new dimension to control logic behavior through resistance modulation. Designers can now explore the integration of programmable memory modes, dynamic access latency adjustments, and reconfigurable logic states. These features pave the way for smart memory cells capable of adaptive performance tuning based on application-specific demands. While fabrication complexity increases, the potential for reconfigurable and secure data storage significantly enhances its value in emerging computing paradigms like neuromorphic and edge AI applications.



3.5: 4-Memristor Based 11T SRAM Cell Schematic

3.6 Summary

The 11T SRAM cell is designed to achieve high performance with low power consumption by using six core transistors in cross-coupled inverters for stable data storage, along with five additional transistors for separate read and write paths. This separation enhances read stability and write efficiency while reducing power usage, making the design suitable for low-power applications like mobile and IoT devices.

However, the conventional 11T SRAM design faces limitations such as increased area due to more transistors, higher design complexity, greater manufacturing costs, and reduced fabrication yield. To overcome these challenges, memristors—non-volatile, two-terminal devices—are integrated into SRAM designs. Known for their scalability, fast switching, and CMOS compatibility, memristors help lower power consumption and optimize voltage delivery by dynamically adjusting resistance.

In the 2-memristor-based 11T SRAM, two memristors are connected to the internal nodes, providing non-volatile behavior, minimizing leakage, and improving stability during read/write operations. This design is ideal for systems with intermittent power like remote sensors. The 4-memristor-based 11T SRAM further improves the architecture by adding memristors to both the storage nodes and access paths. This enhances access control, reduces dynamic power loss, and enables programmable features like adaptive latency and reconfigurable logic. It is especially beneficial for critical applications in aerospace, medical, and edge AI systems.

CHAPTER 4

TOOL CONTENT

LT-SPICE

TOOL CONTENT

LTspice

To begin circuit design in LTspice, click the “SwCAD III” shortcut created during installation. Then, navigate to “File” in the menu bar and select “New Schematic” to launch the schematic editor window where circuit components can be added and connected as shown in fig 4.1.

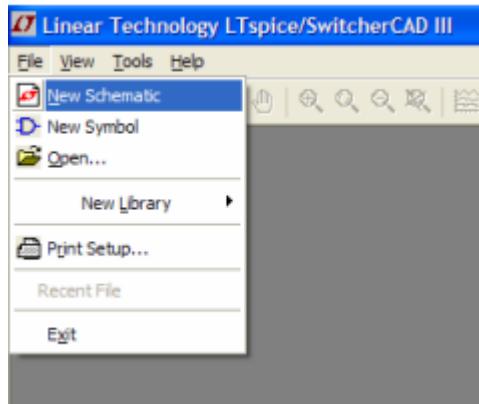


Fig 4.1: Opening a New Schematic in LTspice (SwCAD III)

4.1 Add a component

The LTspice toolbar, shown in Fig. 4.2, provides quick access to essential tools such as placing components (resistor, capacitor, inductor, diode), drawing wires, labeling nodes, running simulations, and editing operations like move, rotate, undo, redo, and placing SPICE directives. It is essential for schematic creation and circuit simulation.

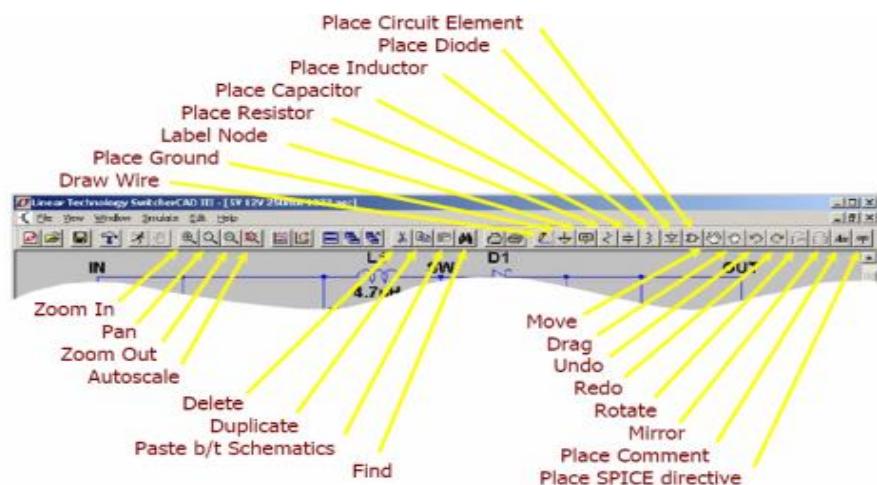


Fig 4.2: LTspice Toolbar Overview

Add a resistor

Press “R” or click the resistor button to insert a resistor. If you want to rotate the resistor before placing, press “ctrl+R” or click the rotate button. Left click where you want to place the resistor. Press “esc” to quit adding resistors.

Add an inductor

Press “L” or click the inductor button to insert an inductor. If you want to rotate the inductor before placing, press “ctrl+R” or click the rotate button. Left click where you want to place the inductor. Press “esc” to quit adding inductors.

Add a capacitor

Press “C” or click the capacitor button to insert a capacitor. If you want to rotate the capacitor before placing, press “ctrl+R” or click the rotate button. Left click where you want to place the capacitor. Press “esc” to quit adding capacitors.

Add other components

Press “F2” or click the component button to insert a component. A “Select Component Symbol” window will open. Take a minute to browse through the list of available components. Note that sources are labeled as “current” and “voltage”.

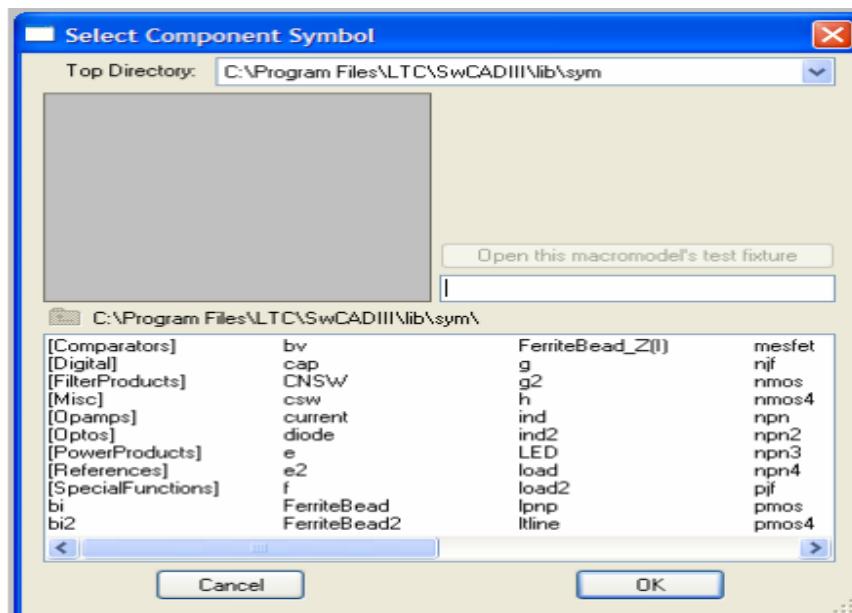


Fig 4.3: Select Component Symbol window in LTspice

In the Select Component Symbol window of LTspice, choose the component you want to add and click “OK”. If you want to rotate the component before placing it, press Ctrl+R or click

the rotate button. Then, left-click where you want to place the component in the schematic. To stop adding the component, simply press Esc.

Figure 4.3 shows the Select Component Symbol window in LTspice, where various categories and components can be browsed for circuit design.

4.2 Modify Component Values

To modify the value of an added component, right click on the component. Enter the value of the component in the default units (ohms, farads, henrys, etc.).

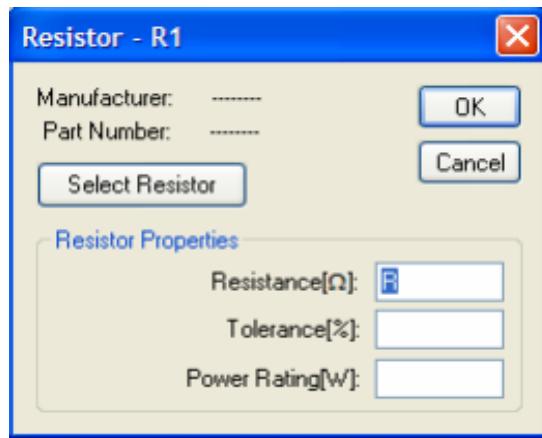


Fig 4.4: Resistor Properties Window in LTspice

The value can also be edited by right clicking on the value of the component shown on the schematic instead of the component itself as shown in fig 4.4.

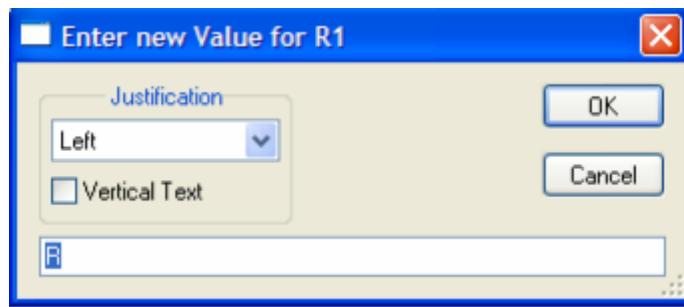


Fig 4.5: Enter New Value Window for R1 in LTspice

For a DC voltage source, enter the voltage and series resistance. For all other voltage sources, click “Advanced”. Select the type of voltage source and enter the required parameters.

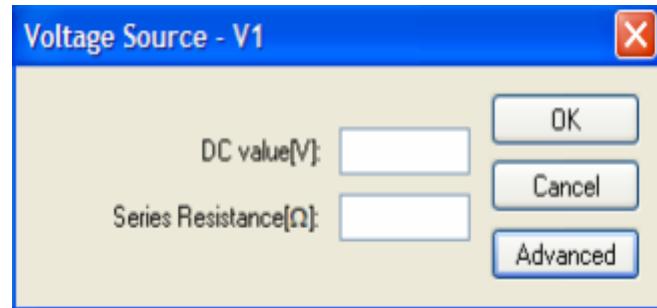


Fig 4.6: Voltage Source Editing Window in LTspice

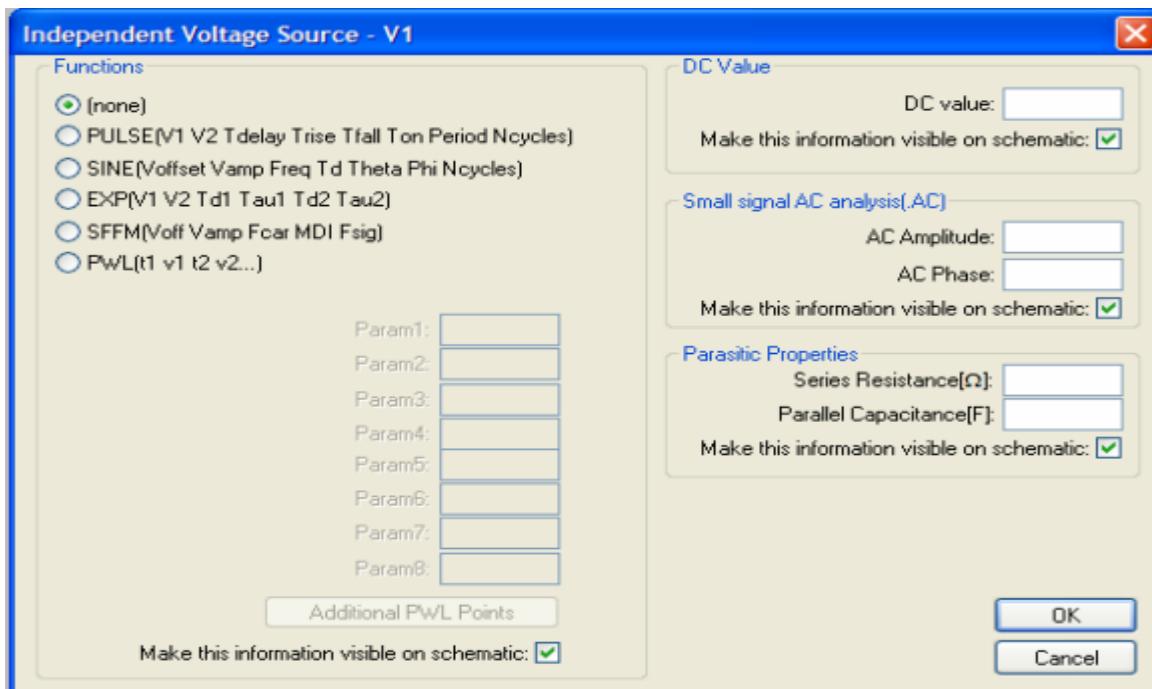


Fig 4.7: Independent Voltage Source Editing Window in LTspice

For example, simulate $v(t) = 5 + 10 \sin(2\pi 60 t + 45^\circ)$ V for 500ms (30 cycles) as a transient analysis as shown in fig 4.8.

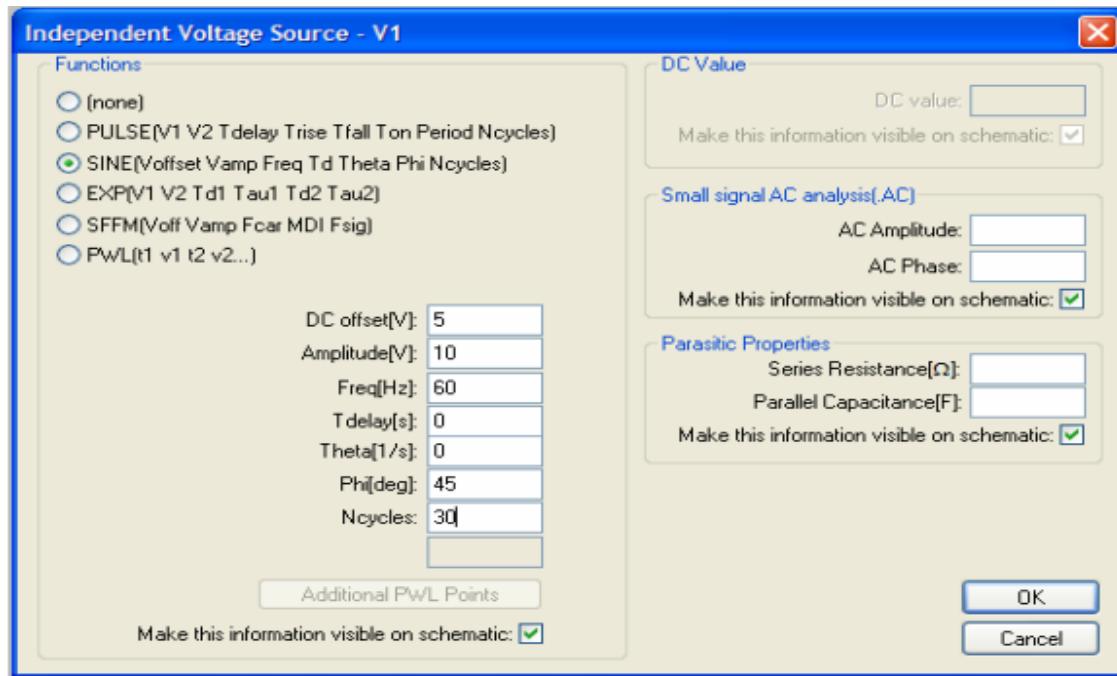


Fig4.8: SINE Waveform Voltage Source Parameters Window in LTspice

- A few things to note about the alternating current source. First, there are two possible analyses which can be done and so there are two sets of parameters.
- For an ac analysis, the parameters are:
 - **AC Amplitude** which is the peak value of the voltage.
 - **AC Phase** which is the phase angle of the voltage For a transient analysis, the parameters are:
 - **DC offset** is the DC offset voltage. It should be set to zero if you need a pure sinusoid.
 - **Amplitude** is the undamped amplitude of the sinusoid; i.e., the peak value measured from zero no DC offset value.
 - **Freq** is the frequency in Hz of the sinusoid.
 - **Tdelay** is the time delay in seconds. Set this to zero for the normal sinusoid.
 - **Theta** is the damping factor. (Not the phase angle!) Also set this to zero for the normal sinusoid. This is used to apply an exponential decay to the sinusoid; theta is the decay constant in 1/seconds.
 - **PHI** is the phase advance in degrees. Set this to 90 if you need a cosine wave form.
 - **Ncycles** is the number of cycles of the pulse that should happen. Leave it as zero if you want ongoing pulses.

For this analysis, LTspice takes it to be a sine source, so if you want to simulate a cosine wave

you need to add (or subtract) a 90° phase shift. Note that the phase angle if left unspecified will be set by default to 0° .

This information is shown on the schematic view in fig 4.9.

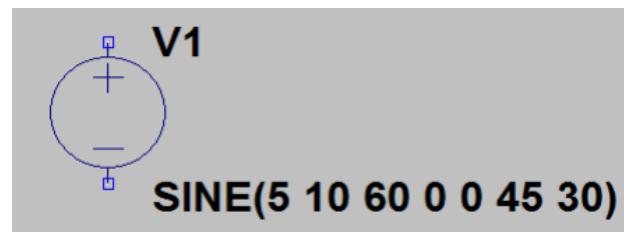


Fig 4.9: SINE Waveform Voltage Source Symbol with Parameters in LTspice

To edit the input information, you can right click on the component as above or right click on the value of the SINE information as shown in fig 4.10.

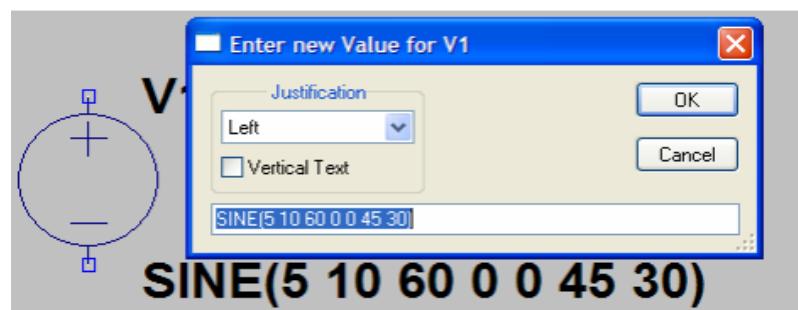


Fig 4.10: Entering SINE Waveform Parameters for Voltage Source in LTspice

To simulate this same function using an ac analysis, enter the magnitude and phase offset in the “Small Signal AC Analysis” fields.

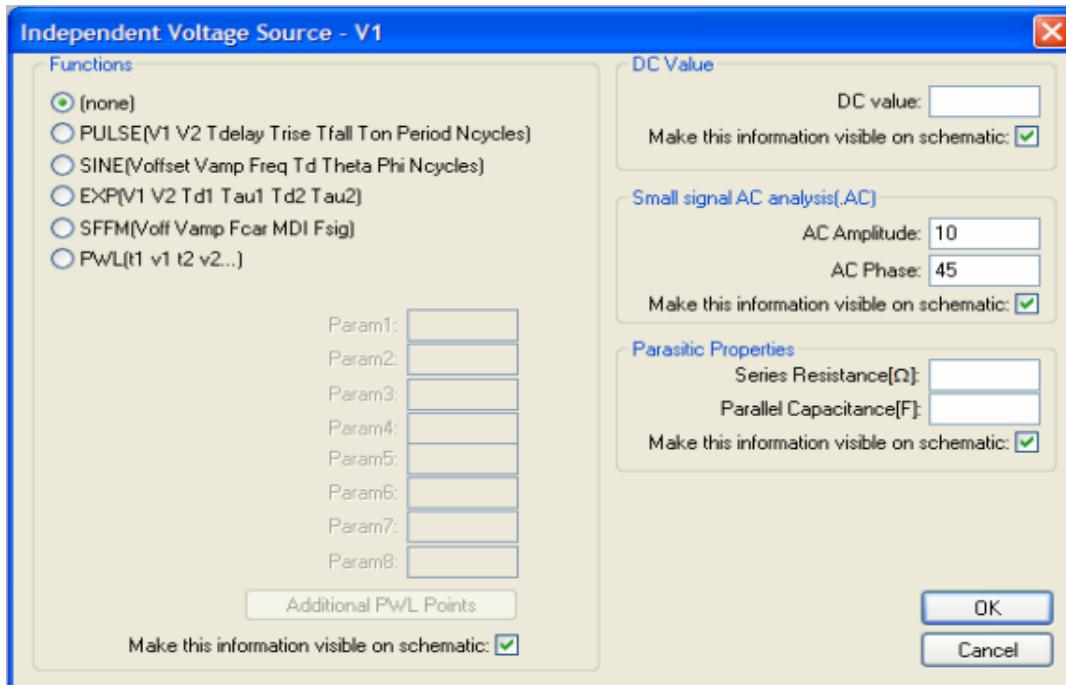


Fig 4.11: Independent Voltage Source Dialog Box in LTspice

PULSE is often used for a transient simulation of a circuit where we want to make it act like a square wave source. It should never be used in a frequency response study because LTspice assumes it is in the time domain, and therefore your probe plot will give you inaccurate results.

- **Vinitial** is the value when the pulse is not "on." So for a square wave, the value when the wave is 'low'. This can be zero or negative as required. For a pulsed current source, the units would be "amps" instead of "volts."
- **Von** is the value when the pulse is fully turned 'on'. This can also be zero or negative. (Obviously, V1 and V2 should not be equal.) Again, the units would be "amps" if this were a current pulse.
- **Tdelay** is the time delay. The default units are seconds. The time delay may be zero, but not negative.
- **Trise** is the rise time of the pulse. LTspice allows this value to be zero, but zero rise time may cause convergence problems in some transient analysis simulations. The default units are seconds.
- **Tfall** is the fall time in seconds of the pulse.
- **Ton** is the pulse width. This is the time in seconds that the pulse is fully on.
- **Tperiod** is the period and is the total time in seconds of the pulse.
- **Ncycles** is the number of cycles of the pulse that should happen. Leave it as zero if you

want ongoing pulses.

- This is a very important source for us because we do a lot of work with the square wave on the wave generator to see how various components and circuits respond to it.
- The **PWL** source is a Piece Wise Linear function that you can use to create a wave form consisting of straight line segments drawn by linear interpolation between points that you define. Since you can use as many points as you want, you can create a very complex wave form. This source type can be a voltage source or a current source.
- The syntax for this source type is flexible and has several optional parameters. The required parameters are two-dimensional points consisting of a time value and a voltage (or current) value. There can be many of these data pairs, but the time values must be in ascending order, and the intervals between time values need not be regular.

4.3 Adding Components:

Delete a component:

To delete a component, press the “delete” button and click the scissors on a component to delete. Press “esc” to quit deleting components.

Move a component:

To move a component, press “F7” or click the move button and left click on the component you want to move. Move the component to the new location, and left click to place the component. Press “esc” to quit moving components.

Add a wire:

To add a wire, press “F3” or click the add wire button. Left click on the starting location, move to the ending location and left click again. If the wire is not straight, click where a 90 degree change in direction is desired. Press “esc” to quit adding wires.

Add ground:

Press “G” or click the ground button and click on the schematic to add a ground. Press “esc” to quit adding grounds.

Label a net:

Press “F4” or click the add net button. Type the name of the net and click “OK”. Click to add the net to the schematic.

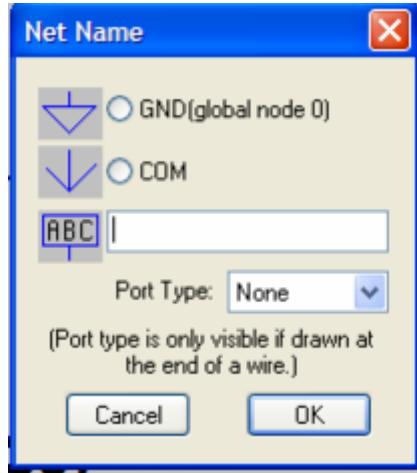


Fig 4.12: Net Name Dialog Box in LTspice

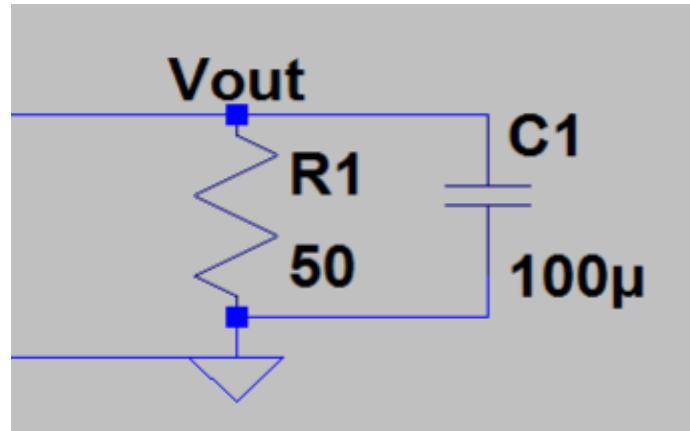


Fig 4.13: RC Low Pass Filter Circuit in LTspice

To run a circuit, select “Simulate” from the file menu and “Run” or click the run button as shown in 4.14.

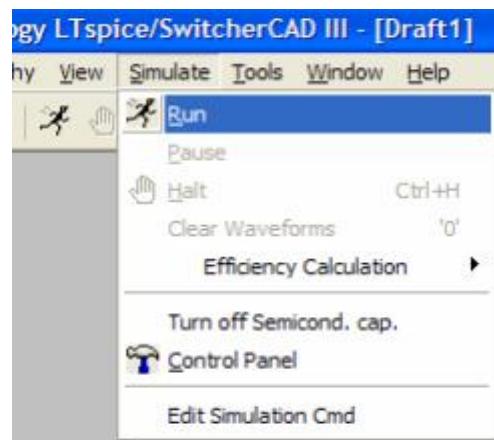


Fig 4.14: Simulation Menu in LTspice Showing 'Run' Option Selected

4.4 Transient Analysis:

The transient analysis is probably the most important analysis you can run in LTspice, and it computes various values of your circuit over time. Two very important parameters in the transient analysis are:

- Stop Time.
- Time to Start Saving Data
- Maximum Timestep
- (various checkboxes later)

The ratio of Stop Time: Maximum Time step determines how many calculations LTspice must make to plot a wave form. LTspice always defaults the start time to zero seconds and going until it reaches the user defined final time. It is incredibly important that you think about what timestep you should use before running the simulation, if you make the timestep too small the probe screen will be cluttered with unnecessary points making it hard to read, and taking extreme amounts of time for LTspice to calculate. However, at the opposite side of that coin is the problem that if you set the timestep too high you might miss important phenomenon that are occurring over very short periods of time in the circuit. Therefore play with step time to see what works best for your circuit. As illustrate in fig 4.15.

You can set a step ceiling which will limit the size of each interval, thus increasing calculation speed. Another handy feature is the Fourier analysis, which allows you to specify your fundamental frequency and the number of harmonics you wish to see on the plot. LTspice defaults to the 9th harmonic unless you specify otherwise, but this still will allow you to decompose a square wave to see it's components with sufficient detail.

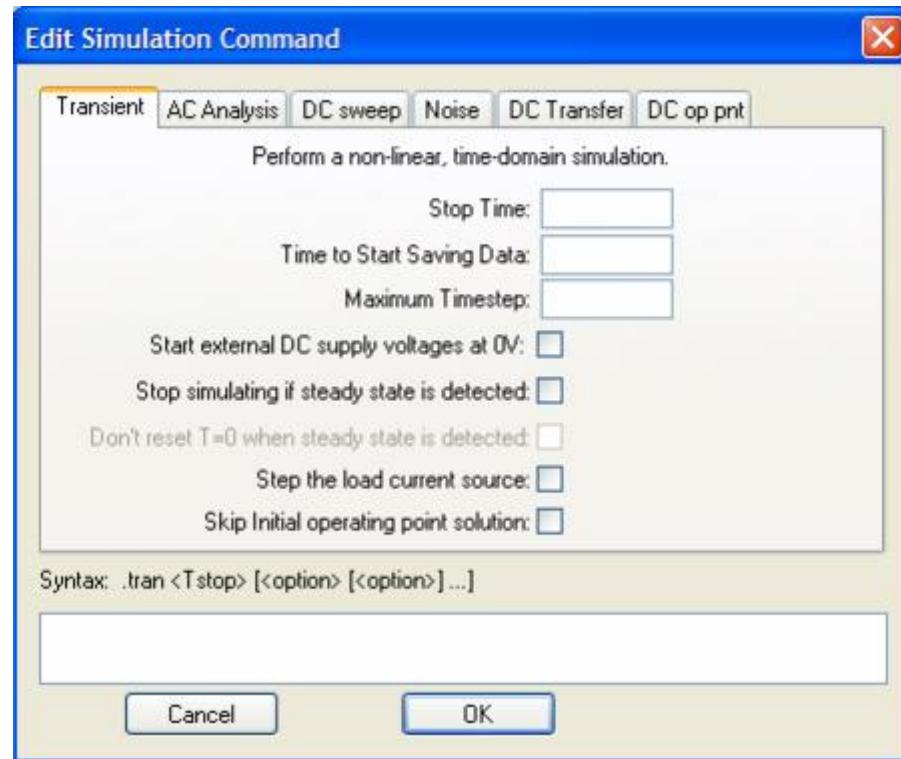


Fig 4.15 Edit Simulation Command Window in LTspice for Transient Analysis Configuration

Select the appropriate tab for simulation and enter the simulation options and click “OK” as shown in fig 4.16. For the AC source shown above, a Transient analysis would be desired to see the outputs for the desired 500ms. At a minimum, a stop time 0.5 seconds should be entered because the source was set to 30 cycles.

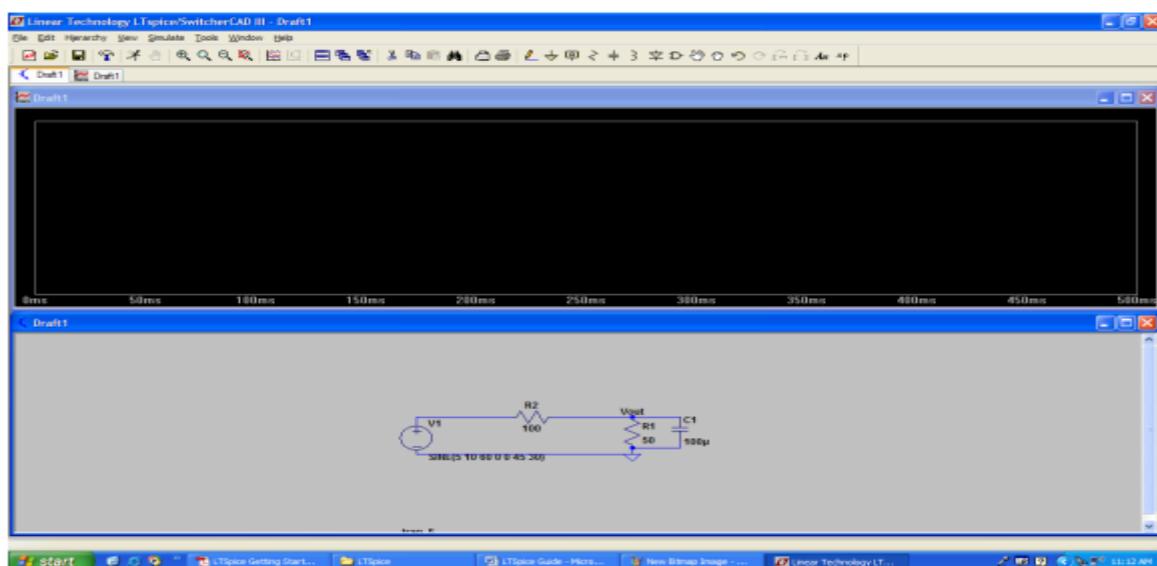


Fig 4.16: RC Low Pass Filter Circuit with Simulation Output Window inLTspice

4.5 Measurements –

NOTE: When making any measurements, a single click will add the measurement to the plot, while a double click will erase all existing measurements and plot the selected measurement by itself.

4.6 Graphing:

Go to the "View" menu as shown in fig 4.17.



Fig 4.17 View Menu Options in LTspice Including Grid

4.7 Adding/Deleting Traces:

- Use "Visible Traces" or on the toolbar to select all the traces you want.
- The add traces window allows you to choose various signals from the circuit, or to create mathematical expressions involving them.

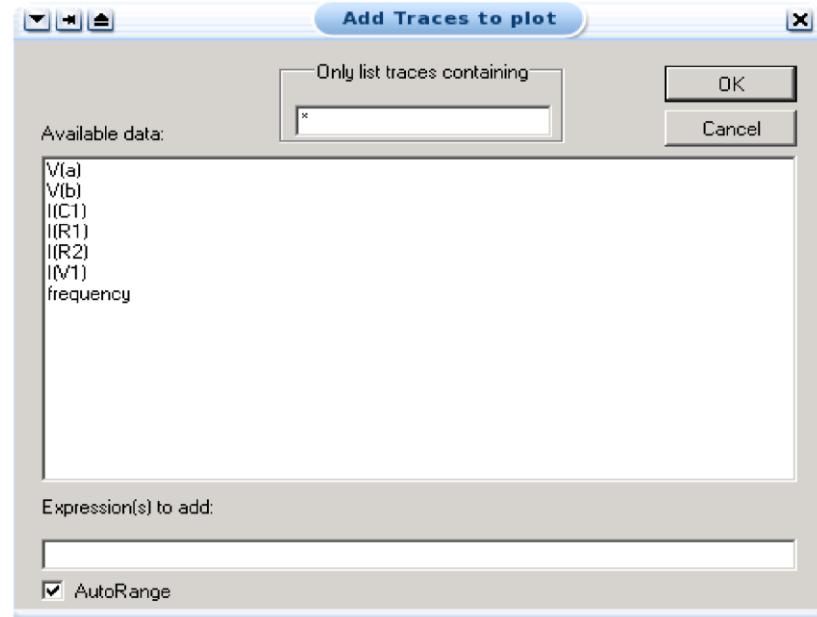


Fig 4.18 Finding Points:

Click on the name of the trace you want to look at and then a cursor window will appear, showing information about the point currently selected as shown in fig 4.18.

You can use the cursor keys to move back and forth through the data points

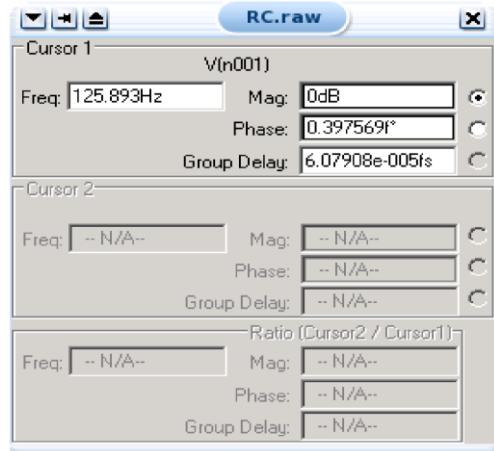


Fig 4.19: Frequency Response Data in LTspice Showing Cursor Measurements

Measure voltage

The voltage probe cursor will automatically appear when the mouse cursor hovers over an appropriate node, indicating that the voltage can be measured at that point. This allows users to quickly and accurately analyze node voltages during or after a simulation.



The above method will measure voltage with respect to ground. To measure voltage across a component, click on the positive node to be measured, drag the mouse to the negative node and release the mouse.



Measure current

To measure the current through a component, move the mouse cursor over the component and click. Note: The current probe will appear when the mouse cursor is above an appropriate component.



Average and RMS Voltage/Current

After selecting a voltage or current, hold the “ctrl” button and click on the name of the measurement in the measurement window. A new window will open displaying the average and RMS values as shown in fig 4.20.

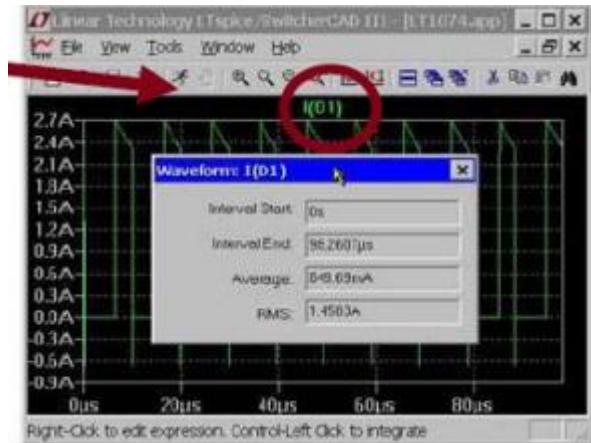


Fig 4.20 Output Current Waveform of Diode (ID1) in LTspice Simulation

Instantaneous Power

To measure the instantaneous power dissipated or supplied by a component, hold the “alt” key and click on the component to be measured.

Average Power

After selecting the instantaneous power of a component, hold the “ctrl” button and click on the name of the measurement in the measurement window. A new window will open displaying the average power.

Zoom

To zoom in on a measurement, left click and drag the mouse over the area. To zoom back to the normal area, right click and select zoom to fit or press “ctrl” – “E”.

NOTE: When selecting an area, the size of the area can be viewed in the lower left hand corner.

AC Analysis

To perform an AC analysis, click on the AC Analysis tab and enter the type of sweep, number of analysis points, and the stop and start frequencies.

The AC analysis allows you to plot magnitude and/or phase versus frequency for different inputs in your circuit.

4.8 Type of Sweep

In the AC analysis menu you have the choice of three types of analysis:

- Linear,
- Octave and
- Decade.

These three choices describe the X-axis scaling which will be produced in probe. For example, if you choose decade then a sample of your X-axis might be 10Hz, 1kHz, 100kHz, 10MHz, etc.... Therefore if you want to see how your circuit reacts over a very large range of frequencies choose the decade option.

You now have to specify at how many points you want LTspice to calculate frequencies, and what the start and end frequency will be. That is, over what range of frequencies do you want to simulate your circuit.

- Number of points
- Start Frequency
- Stop Frequency

For the voltage source above, we can start by looking only at the response at the frequency of the source. The AC analysis is set to 1 point with a start and stop frequency of 60Hz as shown in 4.21.

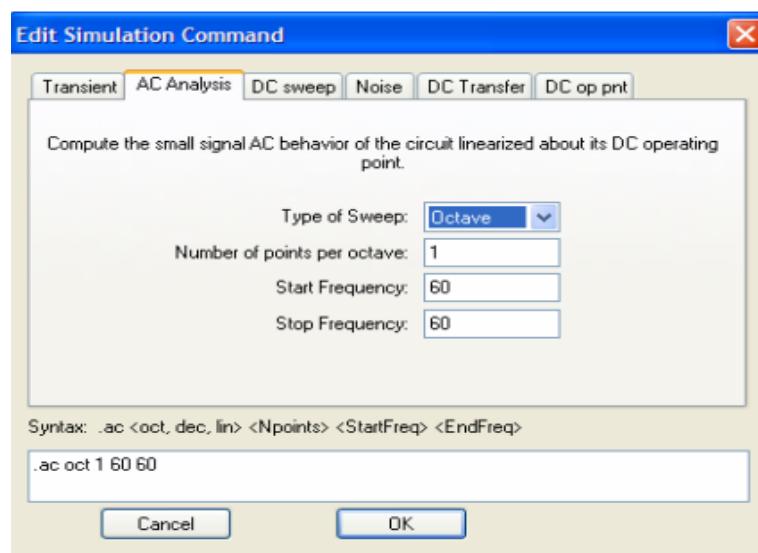
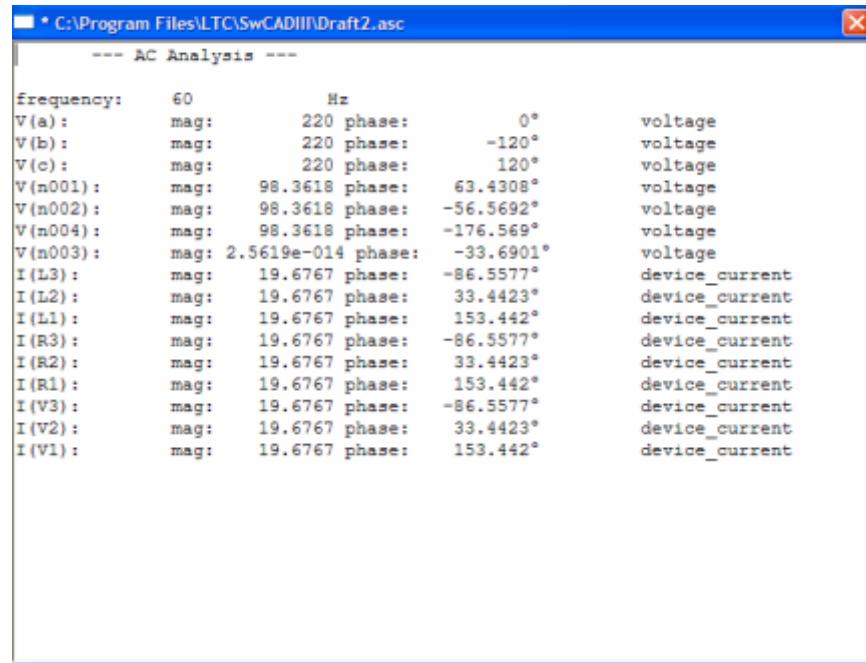


Fig 4.21: Output Current Waveform of Diode (ID1) in LTspice Simulation

When running the AC analysis, a window will open showing the magnitudes and phases of the voltages and currents in the circuit.



The screenshot shows a Windows application window titled "C:\Program Files\LTSpice\SwCADIII\Draft2.asc". The title bar also includes "AC Analysis ---". The main content area displays the results of an AC analysis. It starts with "frequency: 60 Hz" followed by a table of voltage and current values with their magnitudes and phases. The table includes:

	mag:	phase:	
V(a):	220	0°	voltage
V(b):	220	-120°	voltage
V(c):	220	120°	voltage
V(n001):	98.3618	63.4308°	voltage
V(n002):	98.3618	-56.5692°	voltage
V(n004):	98.3618	-176.569°	voltage
V(n003):	2.5619e-014	-33.6901°	voltage
I(L3):	19.6767	-86.5577°	device_current
I(L2):	19.6767	33.4423°	device_current
I(L1):	19.6767	153.442°	device_current
I(R3):	19.6767	-86.5577°	device_current
I(R2):	19.6767	33.4423°	device_current
I(R1):	19.6767	153.442°	device_current
I(V3):	19.6767	-86.5577°	device_current
I(V2):	19.6767	33.4423°	device_current
I(V1):	19.6767	153.442°	device_current

Fig 4.22 AC Analysis Output Results in LTspice

To view the circuit for multiple frequencies, increase the number of points and set the start and stop frequencies to view the desired frequencies. The voltages, currents, and power can be measured as described above in fig 4.22.

DC Sweep

The DC sweep allows you to do various different sweeps of your circuit to see how it responds to various conditions.

For all the possible sweeps,

- voltage,
- current,
- temperature, and
- parameter and global

you need to specify a start value, an end value, and the number of points you wish to calculate.

For example you can sweep your circuit over a voltage range from 0 to 12 volts. The main two

sweeps that will be most important to us at this stage are the voltage sweep and the current sweep. For these two, you need to indicate to LTspice what component you wish to sweep, for example V1 or V2.

Another excellent feature of the DC sweep in LTspice, is the ability to do a **nested sweep**.

A nested sweep allows you to run two simultaneous sweeps to see how changes in two different DC sources will affect your circuit.

Once you've filled in the main sweep menu, click on the nested sweep button and choose the second type of source to sweep and name it, also specifying the start and end values. (Note: In some versions of LTspice you need to click on **enable nested sweep**). Again you can choose Linear, Octave or Decade, but also you can indicate your own list of values, example: 1V 10V 20V. **DO NOT** separate the values with commas.

A nested sweep allows you to run two simultaneous sweeps to see how changes in two different DC sources will affect your circuit.

Once you've filled in the main sweep menu, click on the nested sweep button and choose the second type of source to sweep and name it, also specifying the start and end values. (Note: In some versions of LTspice you need to click on enable nested sweep). Again you can choose Linear, Octave or Decade, but also you can indicate your own list of values, example: 1V 10V 20V. **DO NOT** separate the values with commas.

Noise

LTspice will simulate noise for you either on the output or the input of the circuit. These noise calculations are performed at each frequency step and can be plotted in probe.

The two types of noise are:

- Output for noise on the outputs and
- Input for noise on the input source.
- Type of Sweep (same as for AC analysis)
- Number of points... (same as for AC analysis)
- Start Frequency (same as for AC analysis)
- Stop Frequency (same as for AC analysis)
- To use input noise you need to tell LTspice where you consider the 'input' in your circuit to be, for example, if your voltage source is labelled 'V1'.

4.9 DC Transfer

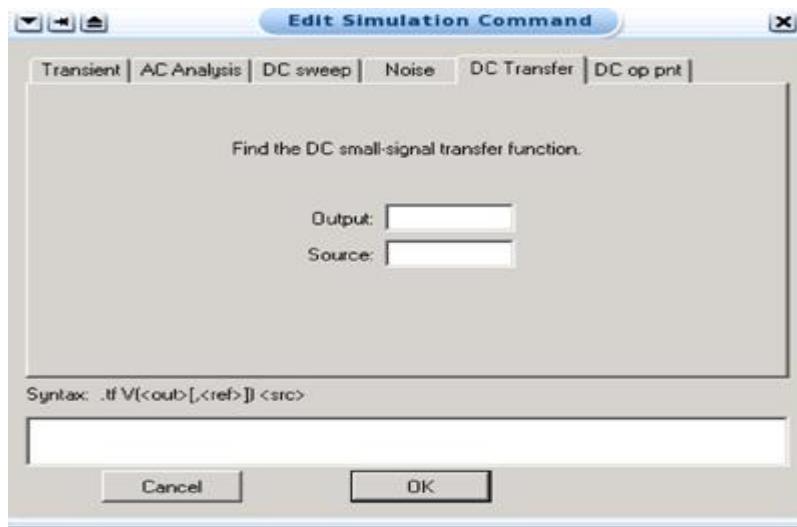


Fig 4.23: DC Transfer Function Simulation Command Window in LTspice

Other types of analysis

There are other SPICE analyses possible. Eventually I might get them in here, including

- parametric
- fourier
- sensitivity

4.10 Summary

This guide explains how to use LTspice for circuit design and simulation, starting with launching the application and opening a new schematic. It describes how to place and manipulate components like resistors, capacitors, inductors, voltage sources, and how to connect them using wires, add ground, and label nodes. Users can modify component values by right-clicking on them and entering the desired parameters. It covers configuring various voltage sources for both AC and transient simulations, including settings for sine, cosine, and square waveforms with options like amplitude, frequency, phase shift, and damping.

Transient analysis is highlighted for observing circuit behavior over time, emphasizing proper timestep settings to balance accuracy and performance. Voltage, current, power, average, and RMS values can be measured directly from the schematic or waveform window using cursor tools.

AC analysis allows for frequency response evaluation with linear, octave, or decade sweeps. Settings include start/stop frequencies and the number of data points. DC sweep analysis lets users examine how circuits respond to changing voltages or currents, with options for single and nested sweeps. Additional analysis options include noise analysis for evaluating input/output noise and DC transfer functions to examine signal gain or behavior under varying conditions. Overall, LTspice offers a powerful environment for designing, testing, and analyzing electronic circuits.

CHAPTER 5

RESULTS

RESULTS

Here are the results for the existing design and the proposed design, the proposed design consists of two design one is 2-memristor SRAM and other is 4-memristor design, the design were simulated in LTspice tool in 22nm technology

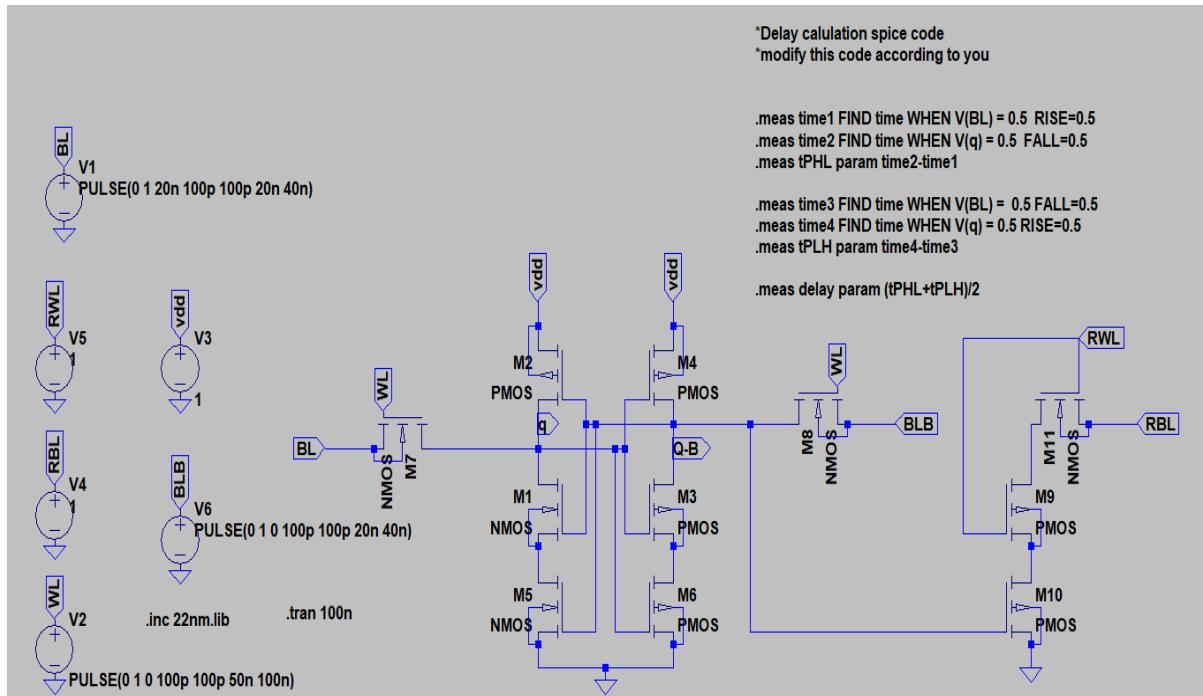


Fig 5.1: Schematic of 11T SRAM

Figure 5.1 represents the schematic of the 11TSRAM Design, which consists of 11 transistors

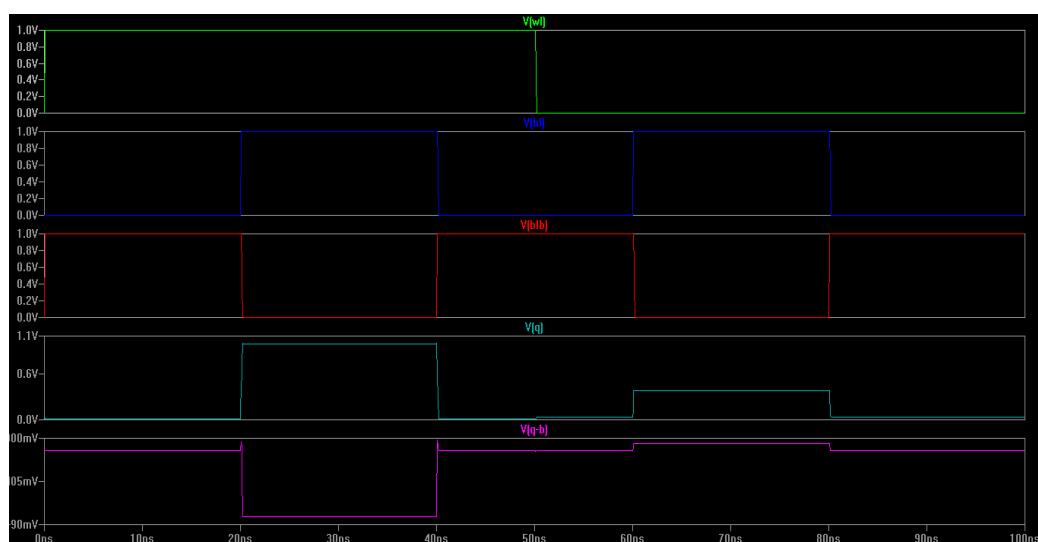


Fig 5.2: Waveform of 11T SRAM

Figure 5.2- the waveform for the 11T SRAM cell, illustrating the timing characteristics during

read and write operations. In the waveform, key signals such as the word , bit lines and output

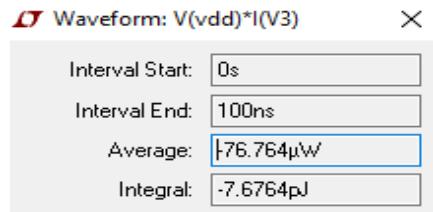


Fig 5.3: Power of 11T SRAM

Figure 5.3 shows the power values for the SRAM cell during its read and write operations

```

timel: time=2.005e-008 at 2.005e-008
time2: time=4.00958e-008 at 4.00958e-008
tphl: time2-time1=2.00458e-008
time3: time=4.015e-008 at 4.015e-008
time4: time=2.01152e-008 at 2.01152e-008
tplh: time4-time3=-2.00348e-008
delay: (tphl+tplh)/2=5.51983e-012

```

Fig 5.4: Delay of 11T SRAM

Figure 5.4 shows the delay values for the SRAM cell during its read and write operations

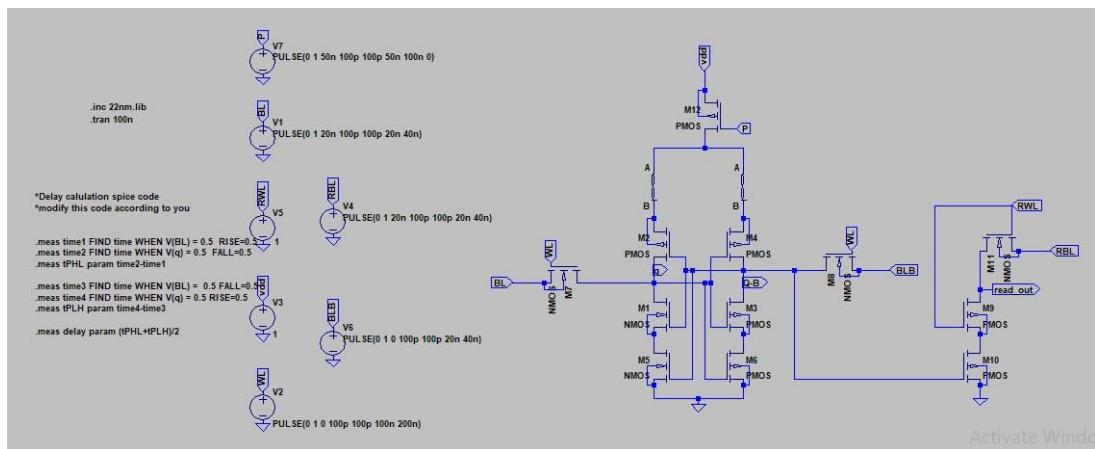


Fig 5.5: Schematic of 2-Memristor based SRAM

The 2-Memristor based SRAM the schematic for the design is shown in the figure 5.5.

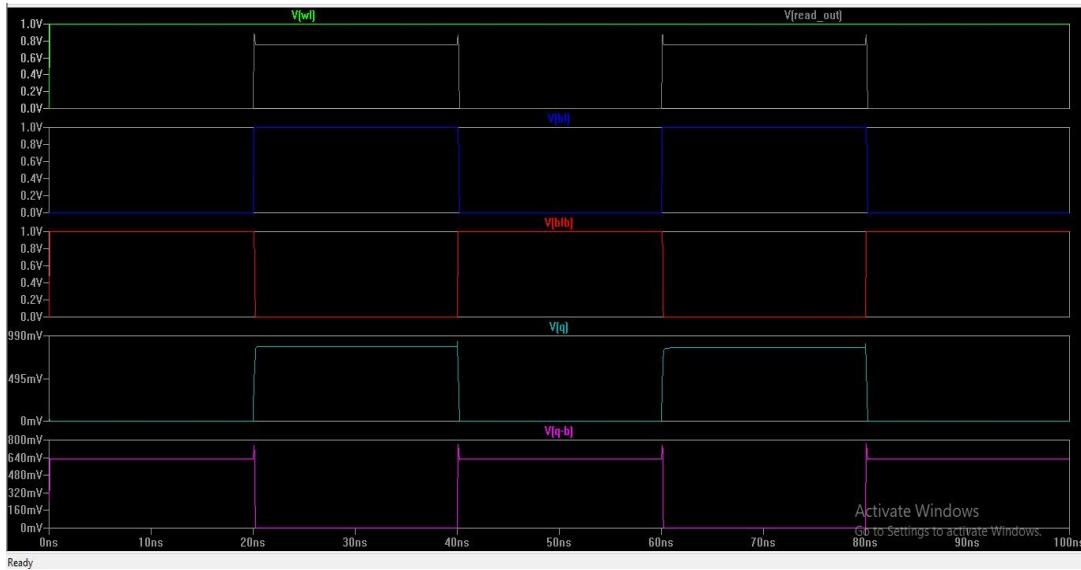


Fig 5.6: Waveform of 2-Memristor based SRAM

Figure 5.6 shows the waveform for the 2 Memristor SRAM cell, illustrating the timing characteristics during read and write operations. In the waveform, key signals such as the word line, bit lines and output

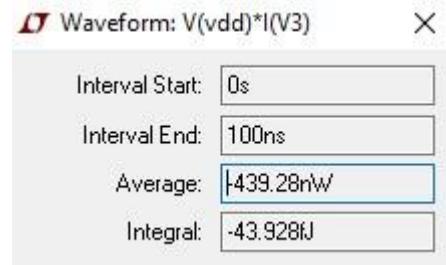


Fig 5.7: Power of 2-Memristor based SRAM

Figure 5.7 shows how much power the 2-memristor cell uses at different operating phases, including read and write cycles. The waveform in the figure presents the power dissipation over time

```

timel: time=2.005e-008 at 2.005e-008
time2: time=4.01091e-008 at 4.01091e-008
tphl: time2-timel=2.00591e-008
time3: time=4.015e-008 at 4.015e-008
time4: time=2.00935e-008 at 2.00935e-008
tplh: time4-time3=-2.00565e-008
delay: (tphl+tplh)/2=1.27666e-012

```

Fig 5.8: Delay of 2-Memristor based SRAM

Figure 5.9 shows the delay values for the 2 Memristor SRAM cell during its read and write operations

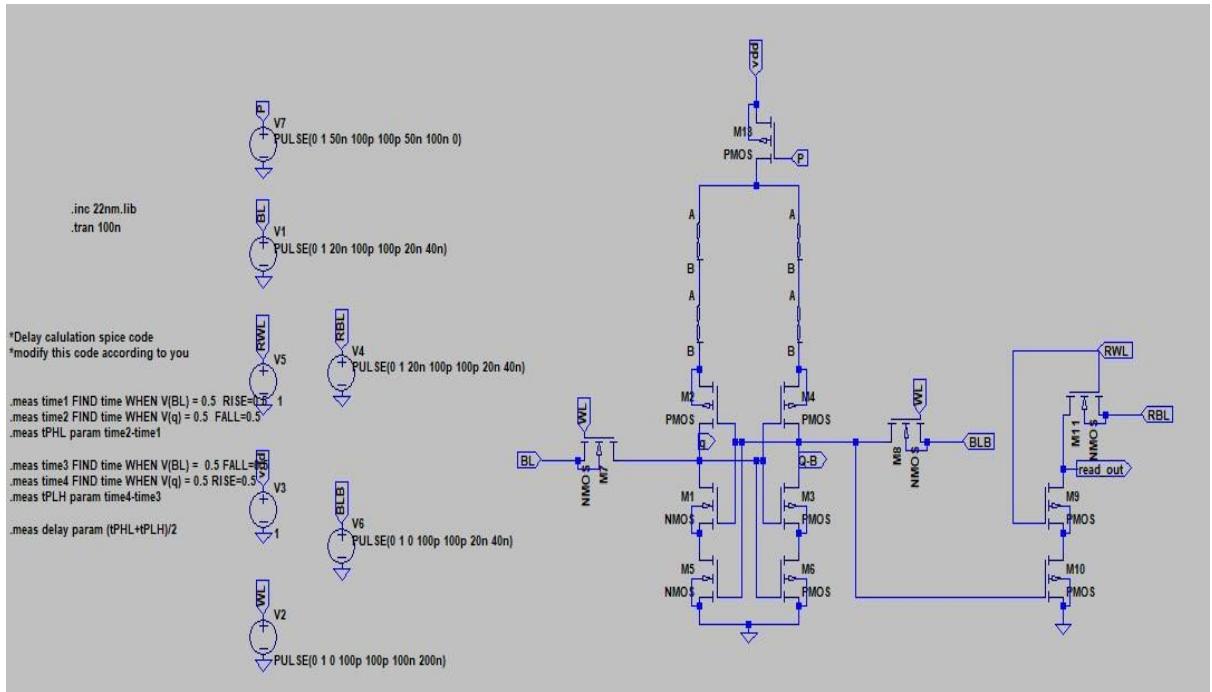


Fig 5.9: Schematic of 4-Memristor based SRAM

Figure 5.9 shows the waveform for the 4-Memristor SRAM cell, illustrating the timing characteristics during read and write operations. In the waveform, key signals such as the word line, bit lines and output.



Fig 5.15: Waveform of 4-Memristor based SRAM

Figure 5.15 shows the waveform for the 4 Memristor SRAM cell, illustrating the timing characteristics during read and write operations. In the waveform, key signals such as the word line, bit lines and output.

```

timel: time=2.005e-008 at 2.005e-008
time2: time=4.01092e-008 at 4.01092e-008
tph1: time2-timel=2.00592e-008
time3: time=4.015e-008 at 4.015e-008
time4: time=2.00935e-008 at 2.00935e-008
tplh: time4-time3=-2.00565e-008
delay: (tph1+tplh)/2=1.31256e-012

```

Fig 5.11: Delay of 4-Memristor based SRAM

Figure 5.11 shows the delay values for the 4 Memristor SRAM cell during its read and write operations

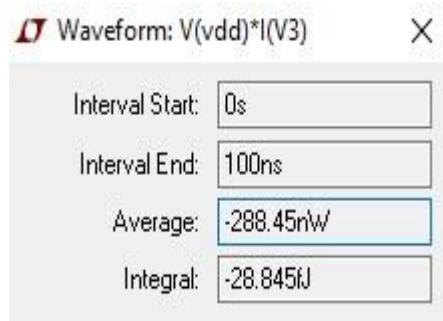


Fig 5.12: Power of 4-Memristor based SRAM

Figure 5.12 shows the power values for the 4 Memristor SRAM cell during its read and write operations

Table 1.1 Comparison Table

DESIGN	POWER	DELAY
11T SRAM	76.74uW	5.519ps
2MEMRISTOR SRAM	439.28nW	1.27 ps
4MEMRISTOR SRAM	288.45nW	1.31 ps

The performance of different SRAM designs is compared based on power consumption and delay. The 11T SRAM consumes $76.74 \mu\text{W}$ with a delay of 5.519 ps. In contrast, the 2-memristor SRAM uses only 439.28nW and has a delay of 1.27 ps, while the 4-memristor SRAM consumes 288.45nW and has a delay of 1.31 ps. These results show a trade-off between power consumption and delay, with memristor-based designs offering better power efficiency and faster delays than the 11T SRAM.

5.1 Summary

The simulation results compare three different SRAM cell designs: the conventional 11T SRAM, the 2-memristor-based 11T SRAM, and the 3-memristor-based 11T SRAM. The analysis focuses on two critical performance parameters: average power consumption and propagation delay. The conventional 11T SRAM exhibits an average power consumption of $76.764 \mu\text{W}$ with a delay of 5.519 ps. While this design is straightforward and widely used, it consumes significantly more power and shows higher delay compared to the memristor-based alternatives.

The 2-memristor 11T SRAM demonstrates a dramatic improvement in both power and speed. With an average power consumption of only 439.28 nW and a delay of 1.276 ps, this design achieves around 99.4% reduction in power consumption and a 76.9% improvement in speed over the conventional version. This makes the 2-memristor 11T SRAM highly suitable for low-power and high-speed memory applications.

Similarly, the 3-memristor 11T SRAM also showcases excellent performance with an even lower average power consumption of 288.45 nW and a slightly higher delay of 1.313 ps compared to its 2-memristor counterpart. While the delay is marginally higher, it still represents a substantial enhancement over the conventional 11T SRAM. The reduced power consumption in this design, about 99.6% lower than the traditional design, offers an even better energy profile.

In conclusion, both memristor-enhanced SRAM designs significantly outperform the conventional 11T SRAM in terms of power efficiency and speed. The 2-memristor variant offers the best overall performance in terms of speed, while the 3-memristor variant excels in power reduction. These results indicate the strong potential of memristor technology in advancing energy-efficient, high-performance SRAM designs.

CHAPTER 6

CONCLUSION

CONCLUSION

In conclusion, the Memristor 11T SRAM cell design, implemented in 22nm LTspice technology, successfully addresses the challenges of stability, power efficiency, and reliable read/write operations. An 11T Memristor-based SRAM cell combines the high speed of SRAM with the non-volatility and power efficiency benefits of memristors. It can lead to lower power consumption and non-volatile storage for SRAM, especially useful for devices requiring both fast access and persistent memory. The integration of memristors enhances the performance and functionality of SRAM, but also adds design complexity. However, it holds significant potential for improving low-power and high-performance memory systems in advanced electronic devices.

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Design and Implementation of 11T-SRAM and Memristor Based SRAM

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Abstract: The design of an 11T SRAM cell aims to enhance stability, power efficiency, and reliable read/write operations compared to traditional SRAM architectures. The core structure consists of six transistors forming a cross-coupled inverter pair for stable data retention, supplemented by five additional transistors that separate read and write operations. This separation ensures non-destructive reads, minimizes disturbances at storage nodes, and improves overall memory cell stability. The write process is managed by two access transistors, controlled by the word line (WL), enabling the bit lines (BL and BLB) and storage nodes to communicate data. The read mechanism operates independently, utilizing transistors linked to the read bit line (RBL) and controlled by a separate read word line (RWL), effectively reducing voltage fluctuations and enhancing read stability by isolating the storage node during read operations. Memristor-based SRAM offers faster switching speeds and lower power consumption while maintaining a compact footprint, positioning it as a strong contender for next-generation memory technologies. Despite challenges such as switching speed limitations, wear-out issues, and integration with existing CMOS circuits, memristor-based memory presents significant advantages, particularly in emerging applications like embedded systems, the Internet of Things (IoT), and neuromorphic computing. This study explores the architectural design, advantages, challenges, and practical applications, highlighting the transformative potential of memristors in the advancement of memory technologies.

Keywords: Efficiency, Memristor-based Memory, Embedded Systems, IoT, Neuromorphic Computing, Power, Stability, 11T-SRAM.

I. INTRODUCTION

Static Random-Access Memory (SRAM): An Overview

One kind of volatile semiconductor memory that stores data using bistable latching circuits is called static random-access memory (SRAM). SRAM retains stored data as long as power is available, in contrast to Dynamic RAM (DRAM), which needs to be refreshed on a regular basis to maintain data. This fundamental difference makes SRAM significantly faster and more efficient in read and write operations, making it a critical component in applications requiring high-speed data access, such as processor cache memory, networking hardware, and AI accelerators. Because of its intricate circuit architecture, SRAM's benefits come at the expense of more silicon area and higher power consumption per bit.

SRAM Cell Design and Configurations

The fundamental building block of SRAM is the memory cell, commonly implemented using six-transistor (6T), eight-transistor (8T), ten-transistor (10T), or twelve-transistor (12T) architectures. Among these, the 6T SRAM cell is the most widely used, consisting of two cross-coupled inverters forming a bistable latch and two access transistors responsible for controlling read and write operations. While 6T SRAM offers efficiency in terms of speed and stability, alternative designs such as 8T, 10T, and 12T configurations enhance noise immunity, minimize leakage power, and improve read/write performance—particularly for ultra-low-power and high-performance applications. Due to its significantly lower latency than DRAM, SRAM is ideal for L1, L2, and L3 cache memory in CPUs and GPUs, where rapid data retrieval is critical. One of the key advantages of SRAM is that it eliminates the need for refresh cycles, simplifying operation and reducing power consumption during active read/write operations. However, this benefit

comes with a trade-off—each SRAM cell requires multiple transistors, making it less dense and more expensive than DRAM. Consequently, SRAM is primarily used for cache memory rather than as main system memory.

Applications and Advancements in SRAM Technology

Despite its higher cost and lower density, SRAM remains a key component in high-speed computing, microcontrollers, networking equipment, biomedical applications, and AI accelerators, where performance and reliability take precedence over cost and space constraints. Researchers in modern semiconductor design focus on optimizing SRAM for power efficiency, stability, and reduced leakage currents especially in deep submicron and nanoscale technologies.

Advantages of SRAM

SRAM's speed is its most obvious benefit. It is a great option for real-time applications as it offers quick data access with little latency and does not require the lengthy refresh cycles like DRAM requires. Additionally, SRAM ensures high data integrity by eliminating the need for capacitors and refresh cycles, reducing the risk of data corruption. Modern advancements in SRAM technology, such as power gating and dynamic voltage scaling, have further enhanced its power efficiency, making it more energy-efficient than earlier generations. However, SRAM is still best suited for scenarios where speed, low latency, and data integrity take precedence over power efficiency. Another advantage of SRAM is its lower heat generation and greater resistance to radiation, making it an optimal choice for high-performance computing, space applications, and critical embedded systems.

II. LITERATURE SURVEY

The performance of SRAM memory circuits is usually measured using industry-standard layouts for traditional SRAM cells, such as the standard S8T cells and the customary C6T cells. These cells do, however, have a number of difficulties, such as half-select problems, write failures, stability degradation, and conflicts between write and read operations. Furthermore, improving read stability by increasing the read static noise margin may have a detrimental effect on the write process. The necessary minimum voltage for both read and write operations may be limited by process fluctuations, according to research forecasts. In response to these challenges, several SRAM topologies have been proposed, offering improved outcomes compared to traditional designs. Using 45nm technology, these include the Schmitt trigger ST9T [1], standard S8T [2], and conventional C6T [3] cells. Their performance is compared to that of the planned E2VR11T cell. The operational specifications of the selected cells, including the proposed E2VR11T cell, are analyzed, with ongoing research confirming that SRAM memory design continues to evolve despite the variety of cells with different

techniques applied. Important features for SRAM memory, especially in low-power applications, include process tolerance and energy efficiency. The chosen cells, such as S8T [2], use two to three bit lines and function in either a differential writing mode or a single-end decoupled read mode. Two transistors are utilized in the S8T [2] cell's read route, and the word line (WL) and read word line (RWL) are frequently employed to facilitate write and read operations. This research suggests the energy-efficient and variability-resilient mersister 11T SRAM memory, which successfully overcomes the concerns raised by the highlighted challenges of current cells.

TRADITIONAL METHOD

The design and development of an 11T SRAM cell [5] are driven by the need for high performance and low power consumption. The process begins with defining functional requirements such as enhanced read stability, write efficiency, and power optimization. These specifications play a crucial role in selecting transistor configurations and layout strategies to ensure a stable and efficient memory cell that operates at low power levels.

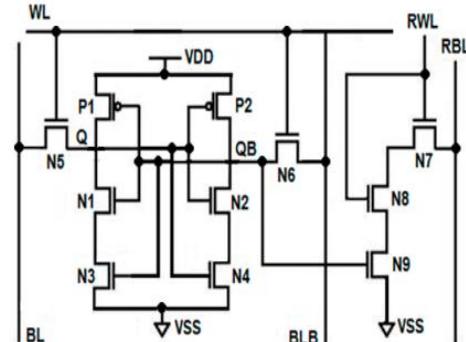
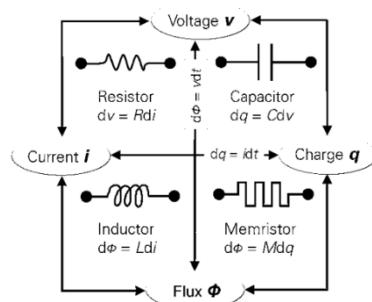


Fig1: 11T SRAM

Core Architecture and Functional Components

At the core of the 11T SRAM [6] cell are six transistors



forming a cross-coupled inverter pair, which provides stable data storage. This fundamental structure is essential for maintaining data integrity within the cell. The additional five transistors serve crucial functions, including improving

read stability, enabling efficient write operations, and managing access control. A key feature of the 1T design is the implementation of dedicated read and write paths, which significantly enhance performance and reduce errors. Write operations are managed by specialized transistors that interact with the word line (WL), enabling data to be written into the cell without disrupting its internal state. Read operations take place through an independent path using separate read bit lines (RBL) and a read word line (RWL).

Read-Write Isolation for Improved Stability

Separating the read and write operations is a critical advancement in the 1T SRAM [6] architecture, as it prevents read disturb errors—a common issue in conventional SRAM designs. By ensuring that read operations do not interfere with the stored data, this design enhances the stability and integrity of the memory cell. Additionally, this isolation mechanism minimizes power consumption during read operations by activating only the necessary transistors, avoiding unnecessary switching of other components.

III. SUGGESTED METHODOLOGY

Memristor-Based SRAM: A Low-Power, High-Efficiency Memory Solution

Introduction to Memristors

Leon O. Chua initially proposed the idea of a memristor, or memory resistor, as the fourth essential passive circuit component, after the resistor, capacitor, and inductor, in 1971. Memristors have variable resistance that varies according on the history of the applied voltage and current, in contrast to conventional resistors that have a set resistance. Memristors are a great option for non-volatile memory applications because of their capacity to "remember" past states even after the power is switched off. A memristor is characterized by its memristance (M), measured in ohms (Ω), which links the charge (q) passing through it to the magnetic flux (Φ) across it. Unlike conventional memory devices such as SRAM and DRAM, which rely on charge storage mechanisms, memristors leverage resistive switching [7], enabling them to store information in a non-volatile manner. This non-volatility, combined with high-speed operation, low power consumption, and CMOS compatibility, makes memristors an excellent candidate for enhancing low-power SRAM designs.

Fig 2. Memristor

Memristor's Advantages in SRAM Design

The integration of memristors with SRAM, opens new possibilities for power-efficient, high-speed memory

architectures. Traditional SRAM is fast but power-hungry, mainly due to leakage currents in CMOS transistors. By incorporating memristors into SRAM, several key benefits can be achieved. Memristor-based SRAM offers several advantages over conventional SRAM, particularly in terms of power efficiency and stability. One key benefit is non-volatility: unlike traditional SRAM [8], which loses data when power is turned off, M-SRAM can retain stored data without requiring a continuous power supply, making it ideal for power-sensitive applications like embedded systems and electronics. Power reduction is another advantage, as memristors dynamically adjust their resistance based on the applied voltage, optimizing the power supply to SRAM cells. Separating the read and write operations is a critical advancement in the 1T SRAM [12] architecture. Memristors help regulate power flow, minimizing unnecessary power wastage. Memristor-based SRAM [13] architectures have gained significant attention due to their potential to enhance power efficiency and speed in various applications. In a hybrid CMOS-memristor SRAM, a memristor is integrated alongside traditional CMOS transistors, where it stores state information, reducing the reliance on volatile charge storage and improving power efficiency while maintaining SRAM-like speed. SRAM's speed is its most obvious benefit. It is a great option for real-time applications as it offers quick data access with little latency and does not require the lengthy refresh cycles like DRAM [15] requires. Non-volatile SRAM with memristors [21] offers instant-on capability, ensuring data retention even after power loss, eliminating the need for boot-up loading. These advancements in memristor-SRAM integration have numerous potential applications, particularly in domains where low power consumption and speed are critical.

Adding 2 Memristors at VDD Power Supply of SRAM

Power Regulation:

The two memristors at the VDD power supply act as dynamic resistors, adjusting their resistance based on the applied voltage. This ensures more stable voltage regulation, reducing unnecessary power dissipation.

Power Consumption Reduction:

By dynamically controlling current flow, leakage power is minimized. This is especially beneficial for low-power applications, such as embedded systems and IoT devices.

Adding 4 Memristors at VDD Power Supply of SRAM

Further Power Optimization: Increasing the number of memristors (from 2 to 4) enhances power efficiency by distributing the load more evenly, reducing overall power wastage. This configuration is particularly useful for large SRAM arrays, where power dissipation scales with size.

IV. RESULTS

Here are the results for the existing design and the proposed design, the proposed design consists of two design one is 2-memristor sram and other is 4-memristor design, the design were simultated in Ltspace tool in 22nm technology.

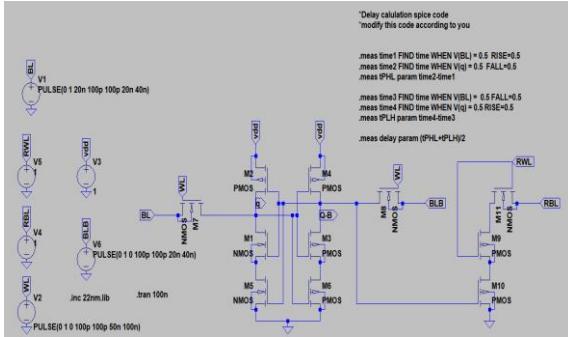


Fig5: Schematic of 11T SRAM Design

Figure 5 represents the schematic of the 11TSRAM Design, which consists of 11 transistors.



Fig6: Waveforms for 11T SRAM

Figure 6 shows the waveform for the 11T SRAM cell, illustrating the timing characteristics during read and write operations. In the waveform, key signals such as the word line, bit lines and output.

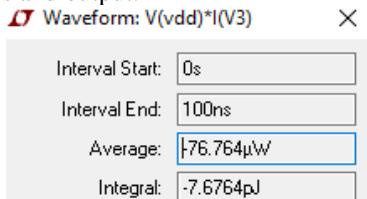


Figure 7: Power for 11T SRAM

Figure 7 shows how much power the 11T SRAM cell uses at different operating phases, including read and write cycles. The waveform in the figure presents the power dissipation over time.

Fig8: Delay for 11T for SRAM

Figure 8 shows the delay values for the 11T SRAM cell during its read and write operations

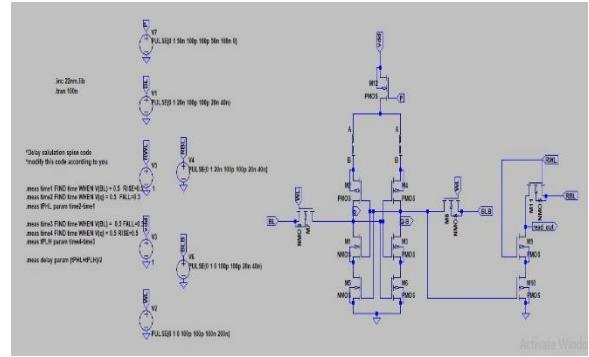


Fig9: Schematic for 2-Memrisotr based SRAM

The 2-Memristor based SRAM the schematic for the design is shown in the figure 9.



Fig10: Waveform for 2-Memrisotr based SRAM

Figure 10 shows the waveform for the 2 Memristor SRAM cell, illustrating the timing characteristics during read and write operations. In the waveform, key signals such as the word line, bit lines and output.

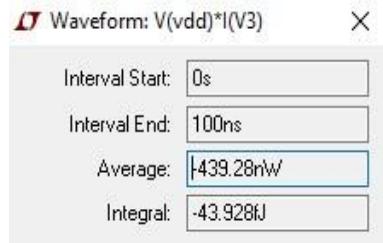


Fig11: Power for 2-Memristor SRAM

Figure 11 shows how much power the 2-memristor cell uses at different operating phases, including read and write cycles. The waveform in the figure presents the power dissipation over time

```

time1: time=2.005e-008 at 2.005e-008
time2: time=4.01091e-008 at 4.01091e-008
tph1: time2-time1=2.00591e-008
time3: time=4.015e-008 at 4.015e-008 -008
time4: time=2.00935e-008 at 2.00935e-008
tplh: time4-time3=-2.00565e-008 -008
delay: (tph1+tplh)/2=1.27666e-012
delay: (tph1+tplh)/2=5.51983e-012

```

Figure 12: Delay for 2-Memrisotr SRAM

Figure 12 shows the delay values for the 2 Memristor SRAM cell during its read and write operations

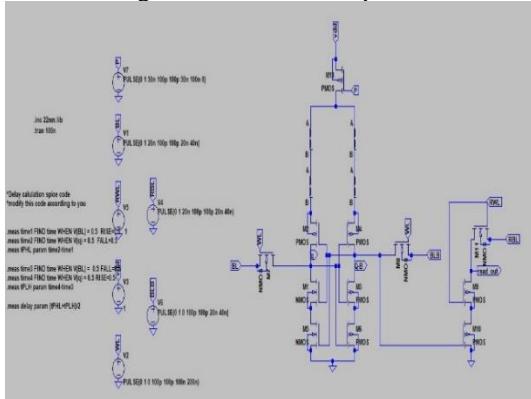


Fig13: Schematic for 4-Memristor based SRAM

The 4-Memristor based SRAM the schematic for the design is shown in the figure 13.

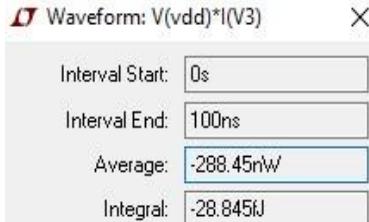


Fig14: Power for 4-Memristor SRAM

Figure 14 shows how much power the 4-memristor cell uses at different operating phases, including read and write cycles. The waveform in the figure presents the power dissipation over time.

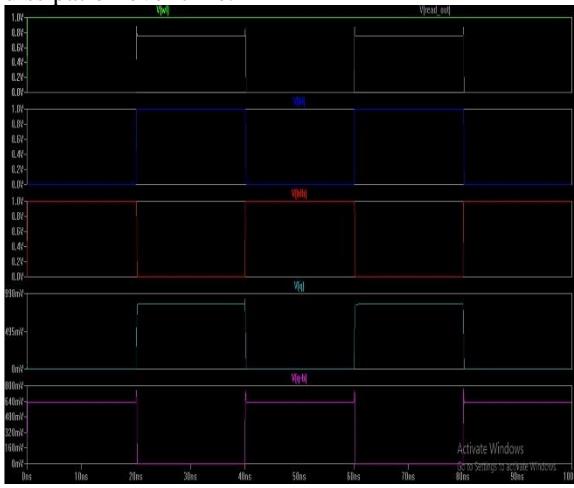


Fig15: Waveform for 4-Memrisotr based SRAM

Figure 15 shows the waveform for the 4 Memristor SRAM cell, illustrating the timing characteristics during read and write operations. In the waveform, key signals such as the word line, bit lines and output.

```
timel: time=2.005e-008 at 2.005e-008  
time2: time=4.01092e-008 at 4.01092e-008  
tphl: time2-timel=2.00592e-008  
time3: time=4.015e-008 at 4.015e-008  
time4: time=2.00935e-008 at 2.00935e-008  
tplh: time4-time3=-2.00565e-008  
delay: (tphl+tplh)/2=1.31256e-012
```

Figure 16: Delay for 4-Memrisotr SRAM

Figure 16 shows the delay values for the 4 Memristor SRAM cell during its read and write operations

Comparison Table

DESIGN	POWER	DELAY
11T SRAM	76.74uW	5.519ps
2-MEMRISTOR SRAM	439.28nW	1.27 ps
4-MEMRISTOR SRAM	288.45nW	1.31 ps

The performance of different SRAM designs is compared based on power consumption and delay. The 11T SRAM consumes 76.74 μ W with a delay of 5.519 ps. In contrast, the 2-memristor SRAM uses only 439.28 nW and has a delay of 1.27 ps, while the 4-memristor SRAM consumes 288.45 nW and has a delay of 1.31 ps. These results show a trade-off between power consumption and delay, with memristor-based designs offering better power efficiency and faster delays than the 11T SRAM.

V. CONCLUSION

In conclusion, the Memristor 11T SRAM cell design, implemented in 22nm LTSpice technology, successfully addresses the challenges of stability, power efficiency, and reliable read/write operations. This innovative design integrates memristors with an 11T SRAM cell, combining the high-speed operation of conventional SRAM with the non-volatility and power efficiency advantages of memristors. By leveraging these characteristics, the proposed design not only reduces power consumption but also enhances data retention, making it particularly beneficial for applications that require both rapid access and persistent memory storage. Furthermore, the incorporation of memristors significantly improves the overall performance and functionality of SRAM, paving the way for advancements in low-power and high-performance memory architectures. This approach is especially valuable for next-generation electronic devices, including IoT systems, edge computing, and AI-driven applications,

where efficient memory solutions are crucial. Despite the promising benefits, further research and optimization can enhance its scalability and adaptability for future semiconductor technologies.

VI. REFERENCES

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