University of Central Florida

Department of Computer Science

CDA 5106: Fall 2022

Machine Problem 1: Cache Design, Memory Hierarchy Design

by

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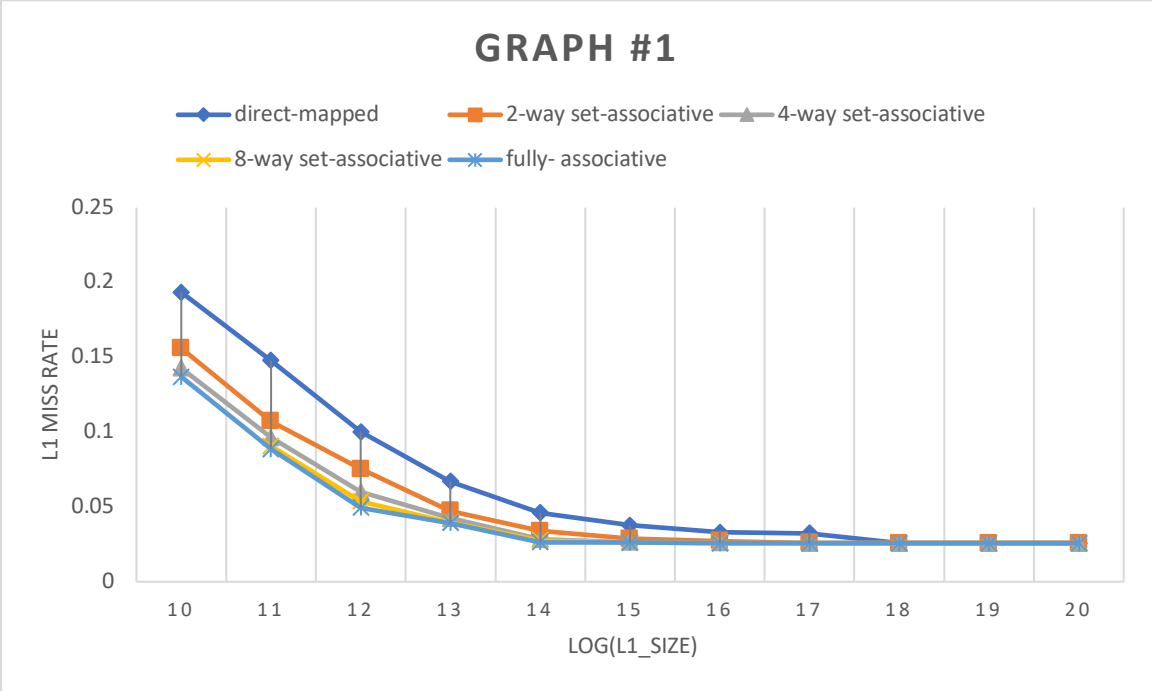
Honor Pledge: "I have neither given nor received unauthorized aid on this test or assignment."

Student's electronic signature: _____Tarun Inakollu_____
(sign by typing your name)

Experiments and Report

1. L1 cache exploration: SIZE and ASSOC

   Graph1:



Discussion:

1) From above Graph, we can observe that increasing cache size decreases the miss rate for given associativity and will become constant as the curves line up. The reason for this is increase in the cache block results in fitting more of blocks in the cache resulting less miss rate. It remains constant after certain cache size because of the compulsory miss which is explained below in (2)

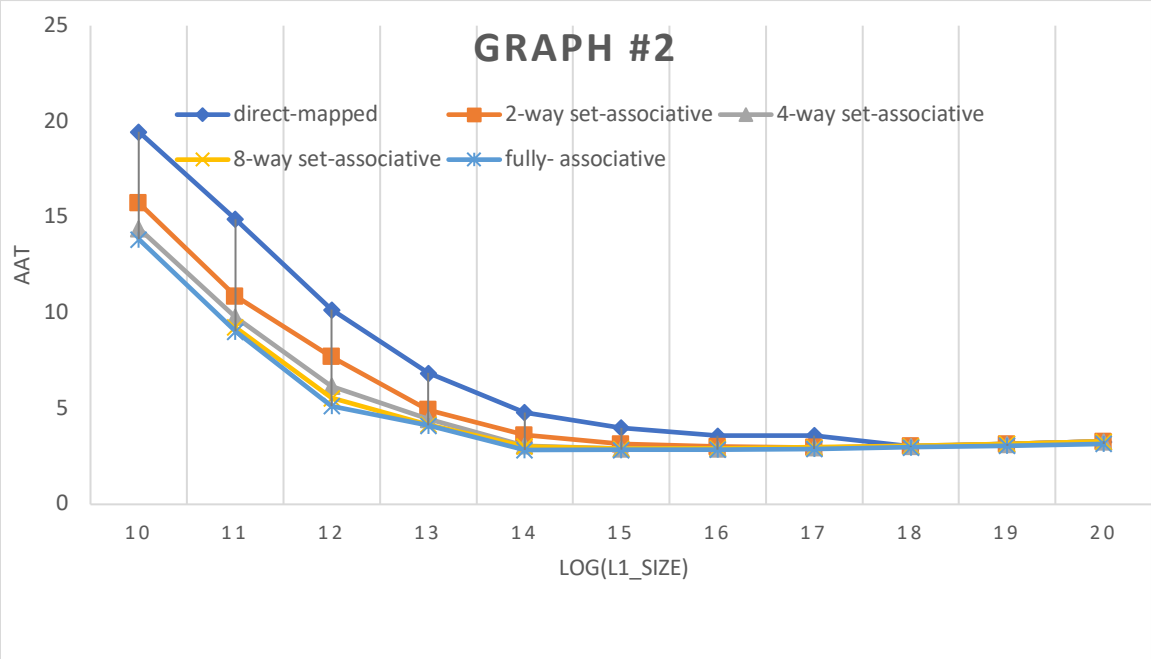
   For given cache size, the effect of increasing associativity initially decreases the miss rate and remains constant after. The reason for this is increasing set associativity fits more blocks in the same set which results in less miss rate.

2) The compulsory is something that occurs when the first access to the block is made. Increasing cache size and increasing set associativity does not affect the compulsory miss rate as it is the default misses. The compulsory miss rate for the above the graph is 0.025820

3) The conflict miss rate for the graph is something that are instances of errors that occur when multiple blocks are mapped to the same frame or set. The estimated values for 2kb cache are

   0.05914 for direct mapping, this is calculated by subtracting direct mapping miss rate and fully associative mapping miss rate i.e (0.14774-0.8860)
   0.01854 for 2-way-associative
   0.00762 for 4-way-associative
   0.00209 for 8-way-associative
   0 for fully associative.

Graph2:

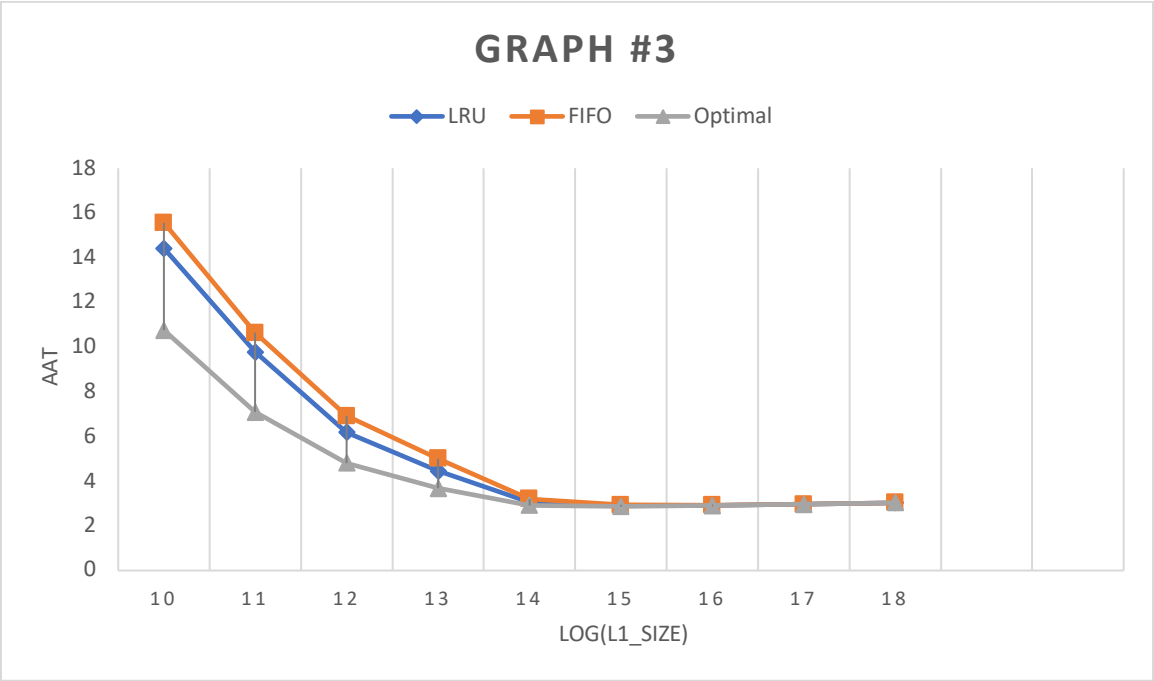


Discussion:

From the above graph, Lowest AAT occurs for fully associative at 14 that is cache 16kb and the value is ~2.8397.

AAT value started increasing from 16KB, this is because miss rate got almost constant but with increase in cache size, access time is increasing. Until 16KB, even though access time increased, Due to heavy decrease in miss rates, the overall AAT value decreased.

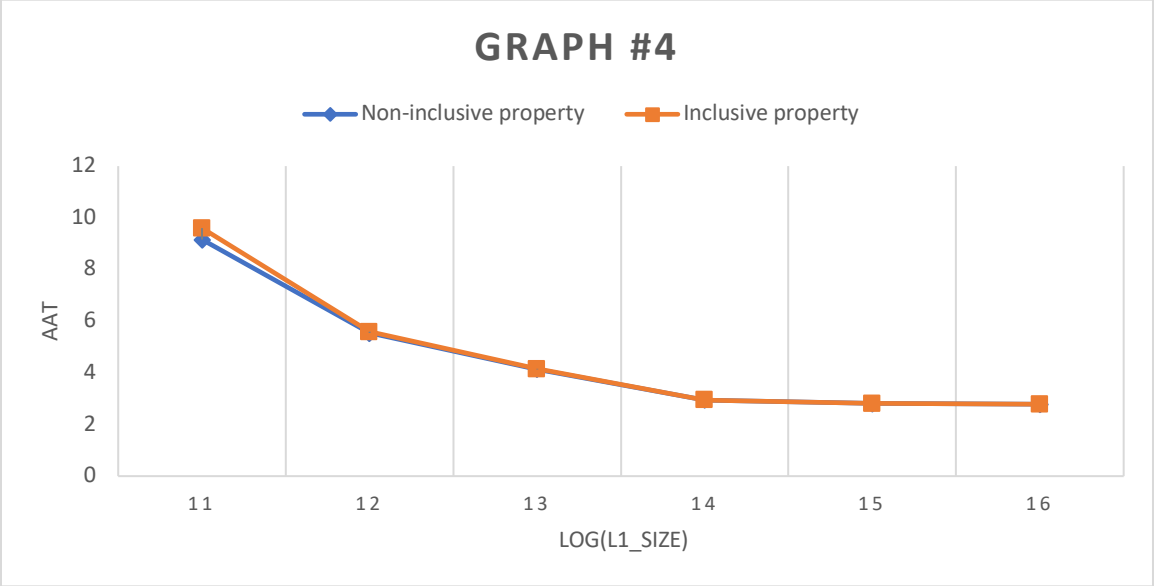
2. Replacement policy study



Discussion:

We can observe that optimal replacement policy results best compared to LRU and FIFO replacement policies as seen from the above graph. But after certain cache size it becomes constant across all the replacement policies. The reason behind this is optimal replacement policy pre-processes the data beforehand such that miss rate will be low initially resulting low Avg Access Time. But the same will be constant after certain cache size because of the compulsory miss rate will be same given higher cache size resulting in constant Avg Access Time for all the replacement policies.

3. Inclusion property study



Discussion:

We can observe that non-inclusive property results in better AAT (Avg Access Time) compared to inclusive as seen from the above graph. This is because Inclusive property involves in block placement in both L1 and L2 caches with respect to any changes with any cache. This results in increased AAT for inclusive due to higher write backs compared to non-inclusive.