Syllabus Handout

Department of Computer Science and Engineering

Course code: DA7020 Credit: 4 (L=3, T=2, P=0)

Course Name: **Advanced Computer Architecture**

Course Coordinator: Dr. Radha Guha , drradha.guha@dituniversity.edu.in, M: 9536769279, Vedanta: 310
Faculty: Samarth Godara, Samarth.godara@gmail.com, M:8114499630, Vedanta: 318

Course Objectives:- The goal is to give students a broad and deep knowledge of contemporary computer architecture issues and techniques. This course gives an overview of computer architecture, with stresses in the underlying design principles and the impact of these principles on computer performance. General topics include design methodology, processor design, control design, memory organization, system organization, and parallel processing. This course gives students knowledge of various architectures and techniques used for building high performance scalable multithreaded and multiprocessor systems.

Lecture Plan:

LecNo	Contents	Text/ Ref. Book	Pages
1.	Review of Fundamentals of CPU, Memory and IO :	KH, HP	1-45, 1-84
2.	Trends in technology, power, energy cost, and dependability.	KH, HP	1-45, 1-84
3.	System attributes to performance. Performance evaluation. Performance metrics, measures and speedup.	KH, HP	1-45, 1-84
4.	Modern computer architecture, architectural classification schemes, Flynn's & Feng's classification.	KH, HP	1-45, 1-84
5.	Multi-tasking, multithreaded architectures.	KH HP	1-45 1-74
6.	Multiprocessor system, shared memory, distributed memory and interconnection networks. Distributed memory multi computers.	KH HP	1-45 1-74
7.	Example solutions	KH HP	1-45 1-74
8.	Example solutions	KH HP	1-45 1-74
9.	Review of pipelining overview, ILP concepts.	HP	172-288
10.	Review of pipelining overview, ILP concepts.	HP	172-288
11.	Speedup, efficiency, throughput. Example solutions.	HP	172-288
12	Speedup, efficiency, throughput. Example solutions.	HP	172-288
13.	Program and network properties. Data and resource dependencies.	KH	51-96
14.	Exploiting more ILP, multiple issue.	HP	172-288
15.	Pipeline and superscalar techniques, nonlinear pipeline processors.	KH	265-322
16.	Reservation table and latency analysis.	KH	265-322
17.	Reservation table and latency analysis. Examples solutions.	KH	265-322
18.	Memory hierarchy principles. Memory technology and optimization.	KH HP	157-205 390-460
19.	Memory cache mapping.	KH HP	157-205 390-460

	Advanced optimization of cache performance. Examples solutions.	KH HP	157-205 390-460
21.	Advanced optimization of cache performance. Examples solutions.	KH HP	157-205 390-460
22.	Virtual memory concepts. paging.	HP	450-500
23.	Virtual memory concepts. paging.	HP	450-500
24.	Techniques for fast address translation.	HP	450-500
25.	Multithreaded architectures. IEEE POSIX threads. creating threads. simultaneous execution of threads.	HP	528-665
26.	Thread synchronization using Semaphore and Mutex. Canceling the threads. VLIW processors.	HP	528-665
27.	Multiprocessors and thread level parallelism	HP	528-665
28.	Symmetric shared memory architecture.	HP	528-665
29.	Distributed shared memory architectures.	HP	528-665
30.	Cache coherence and synchronization mechanisms. snoopy bus protocol.	KH	331-393
31.	Parallel Computing model, Sequential model, need of alternative model.	KH	1-45
32.	Parallel computational models such as PRAM, LMCC, Hypercube, Cube Connected Cycle, Butterfly, Perfect Shuffle Computers, Tree model, Pyramid model. Fully Connected model, PRAM-CREW, EREW Models.	KH	1-45
33.	Parallel computational models such as PRAM, LMCC, Hypercube, Cube Connected Cycle, Butterfly, Perfect Shuffle Computers, Tree model, Pyramid model, Fully Connected model, PRAM-CREW, EREW Models.	KH	1-45
34.	Parallel Algorithms, PRAM Algorithms:	Instructor's notes	
35.	Parallel Reduction, Prefix Sums.	Instructor's notes	
36.	Preorder Tree Traversal, Merging two Sorted lists.	Instructor's notes	
37.	Matrix Multiplication, Row Column Oriented Algorithms, Block Oriented Algorithms	Instructor's notes	
38.	Parallel Quicksort, Hyper Quicksort; Solving Linear Systems: Gaussian Elimination, Jacobi Algorithm; Parallel Algorithm Design Strategies.	Instructor's notes	
39.	Review for end term exam.		
40.	Review for end term exam.		

Course Learning Outcomes:- At the end of the course students should be able to evaluate performance of different computer architecture with respect to various parameters and analyze performance of different ILP techniques. Identify cache and memory related design issues in multi-processor architecture.

Text Books:

1. Kai Hwang. Advance Computer Architecture. TMH. (aka **KH**).

Hennessy and Patterson. Computer Architecture: A Quantitative Approach. Morgan Kaufman Publisher. (aka **HP**).

3.

Reference Books:

1. Harris and Harris Digital Design and Computer Architecture. Second Edition. MK
2. Morris Mano. Computer System Architecture. Third Edition. Pearson

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Signature of Course Coordinator

Signature of HOD

Name: .....

Name: .....

Date: .....