# State Table Diagram:

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Outputs and their meaning:

G1 = Green on first road.

Y1 = Yellow on first road.

R1 =Red on first road.

G2 = Green on second road.

Y2 = Yellow on second road.

R2 =Red on second road.

G3 = Green on third road.

Y3 = Yellow on third road.

R3 =Red on third road.

G4 = Green on fourth road.

Y4 = Yellow on fourth road.

R4 =Red on fourth road.

| State | Time | Next State | G1 | Y1 | R1 | G2 | Y2 | R2 | G3 | Y3 | R3 | G4 | Y4 | R4 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 0-5 | 2 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| 2 | 6-40 | 3 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| 3 | 41-45 | 4 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 4 | 46-80 | 5 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 5 | 81-85 | 6 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 |
| 6 | 86-120 | 7 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |
| 7 | 121-125 | 8 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 |
| 8 | 126-160 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |

In VHDL code we have used array of 12 binary logic bits. Count is incremented with each clock and with the clock we are changing the state after particular count.

When state 8 is reached then count is again set to 0 and State is changed to 1.