DESIGN OF DIGITAL SYSTEMS

Laboratory 1

1.

```
C:\Users\Teo\Desktop\Tasos\Work\Atalanta>atalanta -D 5 c880o.bench -l c880o.log
************************************************************
*                                                          *
*          Welcome to atalanta (version 2.0)               *
*                                                          *
*                 Dong S. Ha (ha@vt.edu)                   *
*      Web: http://www.visc.vt.edu/people/ha               *
*   Virginia Polytechnic Institute & State University      *
*                                                          *
************************************************************

******   SUMMARY OF TEST PATTERN GENERATION RESULTS   ******
1. Circuit structure
   Name of the circuit                      : c880o
   Number of primary inputs                 : 60
   Number of primary outputs                : 26
   Number of gates                          : 409
   Level of the circuit                     : 25

2. ATPG parameters
   Test pattern generation mode             : DTPG + TC
   Backtrack limit                          : 10
   Initial random number generator seed     : 1682069482
   Test pattern compaction mode             : NONE

3. Test pattern generation results
   Number of test patterns                  : 4039
   Fault coverage                           : 100.000 %
   Number of collapsed faults               : 942
   Number of identified redundant faults    : 0
   Number of aborted faults                 : 0
   Total number of backtrackings            : 1066

4. Memory used                              : 168058 Kbytes

5. CPU time
   Initialization                           : 0.000 secs
   Fault simulation                         : 0.000 secs
   FAN                                      : 1.567 secs
   Total                                    : 1.567 secs
```

The response of the circuit for each fault in each of the 5 cases above is shown in the c880o.log file, which details each fault detected, the 5 test vectors that detect it and their response.

2.

```
C:\Users\Teo\Desktop\Tasos\Work\Atalanta>atalanta -r 48 s9234.bench -l s9234.log
*************************************************************
*                                                           *
*          Welcome to atalanta (version 2.0)                *
*                                                           *
*                  Dong S. Ha (ha@vt.edu)                   *
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*                                                           *
*************************************************************

******   SUMMARY OF TEST PATTERN GENERATION RESULTS   ******
1. Circuit structure
   Name of the circuit                          : s9234
   Number of primary inputs                     : 247
   Number of primary outputs                    : 250
   Number of gates                              : 5597
   Level of the circuit                         : 58

2. ATPG parameters
   Test pattern generation mode                 : RPT + DTPG + TC
   Limit of random patterns (packets)           : 48
   Backtrack limit                              : 10
   Initial random number generator seed         : 1682069935
   Test pattern compaction mode                 : REVERSE + SHUFFLE
   Limit of suffling compaction                 : 2
   Number of shuffles                           : 12

3. Test pattern generation results
   Number of test patterns before compaction : 714
   Number of test patterns after compaction  : 376
   Fault coverage                               : 93.475 %
   Number of collapsed faults                   : 6927
   Number of identified redundant faults        : 404
   Number of aborted faults                     : 48
   Total number of backtrackings                : 731

4. Memory used                                  : 169877 Kbytes

5. CPU time
   Initialization                               : 0.267 secs
   Fault simulation                             : 4.167 secs
   FAN                                          : 3.650 secs
   Total                                        : 8.083 secs
```

3.

```
C:\Users\Teo\Desktop\Tasos\Work\Atalanta>atalanta -D 2 -b 4 -u s9234.bench
************************************************************
*                                                          *
*          Welcome to atalanta (version 2.0)               *
*                                                          *
*                  Dong S. Ha (ha@vt.edu)                  *
*      Web: http://www.visc.vt.edu/people/ha               *
*   Virginia Polytechnic Institute & State University      *
*                                                          *
************************************************************

******   SUMMARY OF TEST PATTERN GENERATION RESULTS   ******
1. Circuit structure
   Name of the circuit                        : s9234
   Number of primary inputs                   : 247
   Number of primary outputs                  : 250
   Number of gates                            : 5597
   Level of the circuit                       : 58

2. ATPG parameters
   Test pattern generation mode               : DTPG + TC
   Backtrack limit                            : 4
   Initial random number generator seed       : 1681982916
   Test pattern compaction mode               : NONE

3. Test pattern generation results
   Number of test patterns                    : 11632
   Fault coverage                             : 93.359 %
   Number of collapsed faults                 : 6927
   Number of identified redundant faults      : 392
   Number of aborted faults                   : 68
   Total number of backtrackings              : 4534

4. Memory used                                : 169713 Kbytes

5. CPU time
   Initialization                             : 0.267 secs
   Fault simulation                           : 0.250 secs
   FAN                                        : 50.517 secs
   Total                                      : 51.033 secs
```

11,632 control vectors were calculated. 6,927 errors were returned. The program found 392 redundant errors.

4.

a. sw3-> gt1 /1

b. gt2 -> sb2 /0

c. f8 /1

d. gh6 -> gt1 /0

5.

```
C:\Users\Teo\Desktop\Tasos\Work\Atalanta>atalanta c1355o.bench -l c1355o.log
*************************************************************
*                                                           *
*          Welcome to atalanta (version 2.0)                *
*                                                           *
*                  Dong S. Ha (ha@vt.edu)                   *
*      Web: http://www.visc.vt.edu/people/ha                *
*   Virginia Polytechnic Institute & State University       *
*                                                           *
*************************************************************

******   SUMMARY OF TEST PATTERN GENERATION RESULTS   ******
1. Circuit structure
   Name of the circuit                      : c1355o
   Number of primary inputs                 : 41
   Number of primary outputs                : 32
   Number of gates                          : 578
   Level of the circuit                     : 25

2. ATPG parameters
   Test pattern generation mode             : RPT + DTPG + TC
   Limit of random patterns (packets)       : 16
   Backtrack limit                          : 10
   Initial random number generator seed     : 1681986265
   Test pattern compaction mode             : REVERSE + SHUFFLE
   Limit of suffling compaction             : 2
   Number of shuffles                       : 6

3. Test pattern generation results
   Number of test patterns before compaction : 108
   Number of test patterns after compaction  : 85
   Fault coverage                           : 99.492 %
   Number of collapsed faults               : 1574
   Number of identified redundant faults    : 8
   Number of aborted faults                 : 0
   Total number of backtrackings            : 0

4. Memory used                              : 168161 Kbytes

5. CPU time
   Initialization                           : 0.000 secs
   Fault simulation                         : 0.000 secs
   FAN                                      : 0.000 secs
   Total                                    : 0.000 secs
```

The last control vectors detect minimal errors (1 to 5). This is because in data compression, the algorithm extracts test vectors that each detect as many errors as possible. Thus, because the first will detect the most, subsequent vectors will

detect fewer and fewer errors. This is why there are fewer vectors than in the simulation without data compression.

6.

```
C:\Users\Teo\Desktop\Tasos\Work\Atalanta>atalanta -N c1355o.bench -l c1355o.log
*************************************************************
*                                                           *
*          Welcome to atalanta (version 2.0)                *
*                                                           *
*                  Dong S. Ha (ha@vt.edu)                   *
*      Web: http://www.visc.vt.edu/people/ha                *
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*************************************************************

******   SUMMARY OF TEST PATTERN GENERATION RESULTS   ******
1. Circuit structure
   Name of the circuit                      : c1355o
   Number of primary inputs                 : 41
   Number of primary outputs                : 32
   Number of gates                          : 578
   Level of the circuit                     : 25

2. ATPG parameters
   Test pattern generation mode             : RPT + DTPG + TC
   Limit of random patterns (packets)       : 16
   Backtrack limit                          : 10
   Initial random number generator seed     : 1681986867
   Test pattern compaction mode             : NONE

3. Test pattern generation results
   Number of test patterns                  : 113
   Fault coverage                           : 99.492 %
   Number of collapsed faults               : 1574
   Number of identified redundant faults    : 8
   Number of aborted faults                 : 0
   Total number of backtrackings            : 0

4. Memory used                              : 168161 Kbytes

5. CPU time
   Initialization                           : 0.000 secs
   Fault simulation                         : 0.000 secs
   FAN                                      : 0.000 secs
   Total                                    : 0.000 secs
```

The difference is that there is no more data compression.

7.

The circuit requested is described below:

#circuit_7

INPUT (A)

INPUT (B)

INPUT (C)

INPUT (D)

INPUT (E)

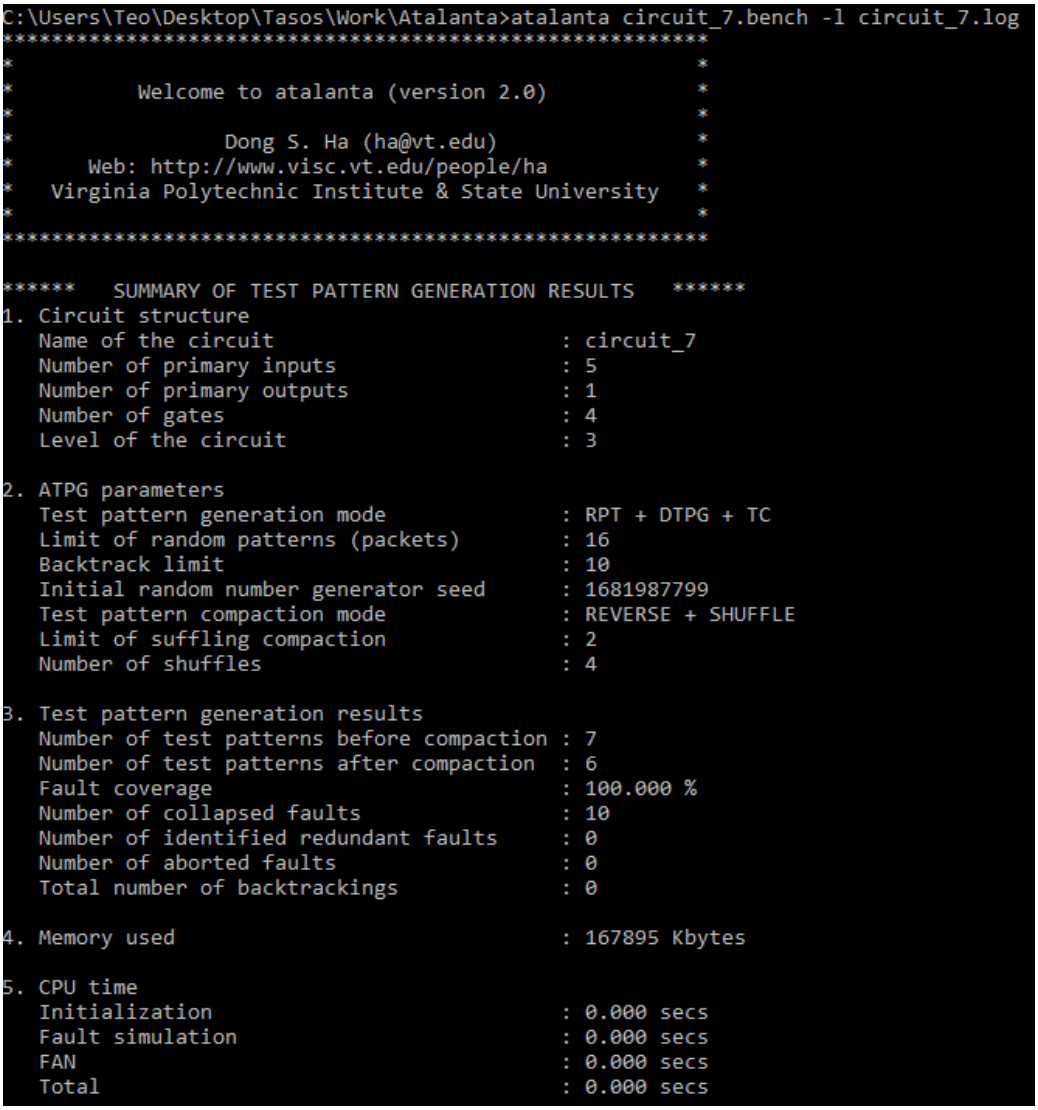
OUTPUT (F)

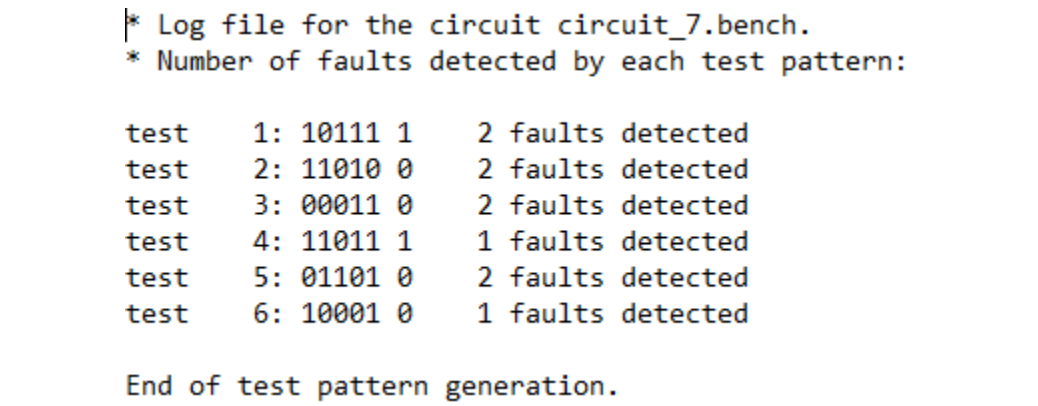
G = AND (A, B)

H = AND (C, D)

I = OR (G, H)

F = AND (E, I)





6 test vectors are generated. The response in each case is shown in the photo above.