DESIGN OF DIGITAL SYSTEMS

Laboratory 1

1.

```
:\Users\Teo\Desktop\Tasos\Work\Atalanta>atalanta -D 5 c880o.bench -l c880o.log
Welcome to atalanta (version 2.0)
               Dong S. Ha (ha@vt.edu)
      Web: http://www.visc.vt.edu/people/ha
   Virginia Polytechnic Institute & State University
******************
       SUMMARY OF TEST PATTERN GENERATION RESULTS
. Circuit structure
  Name of the circuit
  Number of primary inputs
Number of primary outputs
                                       : 60
                                       : 26
  Number of gates
                                        : 409
  Level of the circuit
                                        : 25
2. ATPG parameters
  Test pattern generation mode
                                       : DTPG + TC
  Initial random number generator seed : 1682069482
Test pattern compaction mode
Test pattern generation results
  Number of test patterns
                                       : 4039
  Fault coverage
                                       : 100.000 %
  Number of collapsed faults
                                       : 942
  Number of identified redundant faults
                                       : 0
  Number of aborted faults
                                       : 0
  Total number of backtrackings
                                        : 1066
4. Memory used
                                        : 168058 Kbytes
5. CPU time
  Initialization
                                        : 0.000 secs
  Fault simulation
                                        : 0.000 secs
  FAN
                                        : 1.567 secs
  Total
                                        : 1.567 secs
```

The response of the circuit for each fault in each of the 5 cases above is shown in the c880o.log file, which details each fault detected, the 5 test vectors that detect it and their response.

```
C:\Users\Teo\Desktop\Tasos\Work\Atalanta>atalanta -r 48 s9234.bench -l s9234.log
  .............
           Welcome to atalanta (version 2.0)
                   Dong S. Ha (ha@vt.edu)
       Web: http://www.visc.vt.edu/people/ha
    Virginia Polytechnic Institute & State University
 ************************************
****** SUMMARY OF TEST PATTERN GENERATION RESULTS ******
1. Circuit structure
   Name of the circuit
                                               : 59234
  Number of primary inputs
Number of primary outputs
Number of gates
                                               : 247
                                               : 250
   Number of gates
                                               : 5597
   Level of the circuit
                                                : 58
ATPG parameters
  Test pattern generation mode : RPT + DTPG + TC
Limit of random patterns (packets) : 48
  Initial random number generator seed : 1682069935

Test pattern compaction mode : REVERSE + S

Limit of suffling compaction : 2

Number of shuffles
                                               : REVERSE + SHUFFLE
Test pattern generation results
   Number of test patterns before compaction : 714
   Number of test patterns after compaction : 376
   Fault coverage
                                               : 93.475 %
   Number of collapsed faults : 6927
Number of identified redundant faults : 404
   Number of aborted faults
                                               : 48
   Total number of backtrackings
                                               : 731
Memory used
                                               : 169877 Kbytes
5. CPU time
   Initialization
                                                : 0.267 secs
   Fault simulation
                                               : 4.167 secs
   FAN
                                               : 3.650 secs
   Total
                                                : 8.083 secs
```

```
C:\Users\Teo\Desktop\Tasos\Work\Atalanta>atalanta -D 2 -b 4 -u s9234.bench
*****************
          Welcome to atalanta (version 2.0)
                Dong S. Ha (ha@vt.edu)
      Web: http://www.visc.vt.edu/people/ha
   Virginia Polytechnic Institute & State University *
*******************
        SUMMARY OF TEST PATTERN GENERATION RESULTS
1. Circuit structure
  Name of the circuit
  Name of the circuit
Number of primary inputs
Number of primary outputs
                                         : 59234
                                         : 247
                                         : 250
  Number of gates
                                         : 5597
  Number of gates
Level of the circuit
                                          : 58
ATPG parameters
  Test pattern generation mode : DTPG + TC
  Backtrack limit
  Backtrack limit : 4
Initial random number generator seed : 1681982916
  Test pattern compaction mode
                                         : NONE
Test pattern generation results
  Number of test patterns
                                         : 11632
                                         : 93.359 %
  Fault coverage
  Number of collapsed faults
                                         : 6927
  Number of identified redundant faults : 392
Number of aborted faults : 68
  Total number of backtrackings
                                          : 4534
Memory used
                                          : 169713 Kbytes
5. CPU time
  Initialization
                                          : 0.267 secs
  Fault simulation
                                          : 0.250 secs
  FAN
                                         : 50.517 secs
  Total
                                          : 51.033 secs
```

11,632 control vectors were calculated. 6,927 errors were returned. The program found 392 redundant errors.

4.

- **a.** sw3-> gt1 /1
- **b.** gt2 -> sb2 /0
- **c.** f8 /1
- **d.** gh6 -> gt1 /0

```
C:\Users\Teo\Desktop\Tasos\Work\Atalanta>atalanta c1355o.bench -l c1355o.log
 Welcome to atalanta (version 2.0)
                  Dong S. Ha (ha@vt.edu)
      Web: http://www.visc.vt.edu/people/ha
    Virginia Polytechnic Institute & State University *
 ***********************************
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         SUMMARY OF TEST PATTERN GENERATION RESULTS

    Circuit structure

  Name of the circuit
                                              : c13550
  Number of primary inputs
Number of primary outputs
                                              : 41
                                              : 32
  Number of gates
                                              : 578
   Level of the circuit
                                               : 25
ATPG parameters
  Test pattern generation mode
Limit of random patterns (packets)
                                              : RPT + DTPG + TC
                                           : 16
   Backtrack limit
                                              : 10
  Initial random number generator seed : 1681986265
Test pattern compaction mode : REVERSE + S
Limit of suffling compaction : 2
                                              : REVERSE + SHUFFLE
  Number of shuffles
                                              : 6
Test pattern generation results
   Number of test patterns before compaction: 108
  Number of test patterns after compaction : 85
  Fault coverage : 99
Number of collapsed faults : 15
Number of identified redundant faults : 8
   Fault coverage
                                              : 99.492 %
                                              : 1574
  Number of aborted faults
                                              : 0
   Total number of backtrackings
                                              : 0
Memory used
                                               : 168161 Kbytes
5. CPU time
   Initialization
                                               : 0.000 secs
   Fault simulation
                                              : 0.000 secs
   FAN
                                               : 0.000 secs
   Total
                                               : 0.000 secs
```

The last control vectors detect minimal errors (1 to 5). This is because in data compression, the algorithm extracts test vectors that each detect as many errors as possible. Thus, because the first will detect the most, subsequent vectors will

detect fewer and fewer errors. This is why there are fewer vectors than in the simulation without data compression.

6.

```
C:\Users\Teo\Desktop\Tasos\Work\Atalanta>atalanta -N c1355o.bench -l c1355o.log
           Welcome to atalanta (version 2.0)
                  Dong S. Ha (ha@vt.edu)
      Web: http://www.visc.vt.edu/people/ha
    Virginia Polytechnic Institute & State University *
 ************************
****** SUMMARY OF TEST PATTERN GENERATION RESULTS ******

    Circuit structure

  Name of the circuit
                                             : c13550
  Name of the circuit
Number of primary inputs
Number of primary outputs
                                             : 41
                                              : 32
  Number of gates
Level of the circuit
                                              : 578
  ATPG parameters
Test pattern generation mode : RPT + DTPG + TC
Limit of random patterns (packets) : 16
Packtrack limit : 10
ATPG parameters
  Initial random number generator seed : 1681986867
  Test pattern compaction mode
                                              : NONE
3. Test pattern generation results
  Number of test patterns
                                             : 113
  Number of collapsed faults
                                             : 99.492 %
  Number of identified redundant faults : 8

Number of aborted faults
  Total number of backtrackings
                                              : 0

    Memory used

                                              : 168161 Kbytes
5. CPU time
   Initialization
                                              : 0.000 secs
   Fault simulation
                                              : 0.000 secs
   FAN
                                              : 0.000 secs
   Total
                                              : 0.000 secs
```

The difference is that there is no more data compression.

7.

The circuit requested is described below:

#circuit_7

INPUT (A)

INPUT (B)

INPUT (C)

INPUT (D)

INPUT (E)

OUTPUT (F)

G = AND(A, B)

H = AND(C, D)

I = OR(G, H)

F = AND (E, I)

```
:\Users\Teo\Desktop\Tasos\Work\Atalanta>atalanta circuit_7.bench -l circuit_7.log
          Welcome to atalanta (version 2.0)
                  Dong S. Ha (ha@vt.edu)
      Web: http://www.visc.vt.edu/people/ha
   Virginia Polytechnic Institute & State University
        SUMMARY OF TEST PATTERN GENERATION RESULTS ******
1. Circuit structure
  Name of the circuit
  Number of primary inputs
Number of primary outputs
Number of gates
                                              : 1
  Level of the circuit
 . ATPG parameters
  Test pattern generation mode
                                              : RPT + DTPG + TC
  Limit of random patterns (packets)
                                              : 16
  Backtrack limit
                                             : 10
  Initial random number generator seed
                                              : 1681987799
  Test pattern compaction mode
Limit of suffling compaction
                                              : REVERSE + SHUFFLE
  Number of shuffles
  Test pattern generation results
  Number of test patterns before compaction: 7
  Number of test patterns after compaction : 6
  Fault coverage
                                             : 100.000 %
  Number of collapsed faults
                                              : 10
  Number of identified redundant faults
  Number of aborted faults
                                              : 0
  Total number of backtrackings
  Memory used
                                              : 167895 Kbytes
  CPU time
  Initialization
                                              : 0.000 secs
   Fault simulation
                                              : 0.000 secs
  FAN
                                              : 0.000 secs
   Total
                                              : 0.000 secs
```

- * Log file for the circuit circuit_7.bench.
- * Number of faults detected by each test pattern:

```
1: 10111 1
                    2 faults detected
test
test
       2: 11010 0
                    2 faults detected
      3: 00011 0
                  2 faults detected
test
test
       4: 11011 1
                    1 faults detected
       5: 01101 0
test
                    2 faults detected
       6: 10001 0
                    1 faults detected
test
```

End of test pattern generation.

6 test vectors are generated. The response in each case is shown in the photo above.