DESIGN OF DIGITAL SYSTEMS

Laboratory 2

LABORATORY EXERCISE 1

1.

Error classification:

Detected: 1639

Possibly detected: 0

Undetectable: 0

ATPG untestable: 0

Not detected: 3

2.

After the fault collapsing process, we had a 99.82% coverage rate. So, of the 1642 faults added, 1639 faults were detected and 3 remained undetected.

3.

The test coverage rate decreased from 99.45% to 99.43%. This was because the faults that were removed were detected in the first place, so now that the detected faults have been reduced, the test coverage has also been reduced.

4.

Detected: 1019

Possibly detected: 0

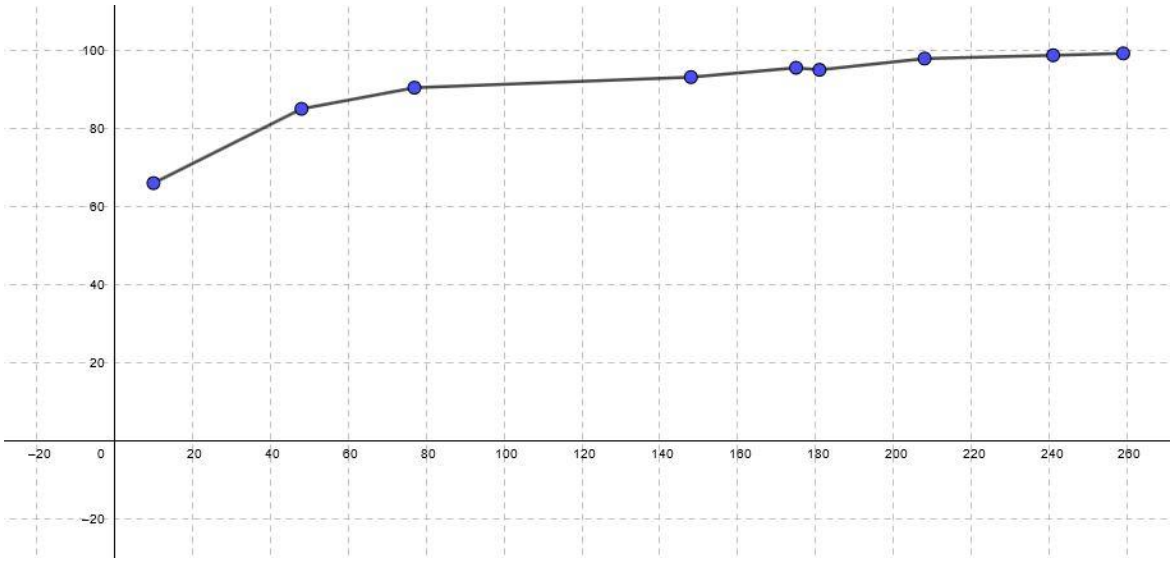
Undetectable: 0

ATPG untestable: 0

Not detected: 1

Of the 1020 new bugs added, only 1 was not detected. This is a 99.9% rate.

5.



In the figure, on the x-axis I have placed the number of test vectors indicating the files rather than what the files are named. On the y-axis is the error coverage rate.

Errors that are not detected are called "Not Detected" and are 43. We did not achieve 100% fault coverage because we only checked the circuit for permanent value faults. The remaining faults are likely to belong to another fault model, for which we did not produce test vectors.

LABORATORY EXERCISE 2

1.

The rule that is violated is C2 (unstable nonscan DFF when clocks off), which is violated 74 times. Of the 2734 bugs added, only 8 are detected, 7 are undetectable and 2719 are ATPG untestable. Test coverage is only at 0.29%.

2.

For all 3 pseudorandom vectors, there is the same test coverage rate (100%) and the same error categorization. So, there are no Random Pattern Resistant errors in the circuit, since with pseudorandom vectors, there was 100% coverage rate.

LABORATORY EXERCISE 3

1.

During the control phase, the operation is correct. There are no violations in any of the 179 cells.

LABORATORY EXERCISE 4

1.

During the control phase, the operation is correct. There are no violations in any of the 74 cells.