LABORATORY EXERCISE 5 VLSI

EXERCISE 1 :

For α)

G	$\frac{4}{3} * 1 = \frac{4}{3}$
H	$\frac{12}{4} = 3$
B	1
F	$\frac{4}{3} * 1 * 3 = 4$
f	$\sqrt[2]{4} = 2$
P	$2 + 1 = 3$
D	$2\sqrt[2]{4} + 3 = 4 + 3 = 7$
x	$\frac{12*1}{2} = 6C$

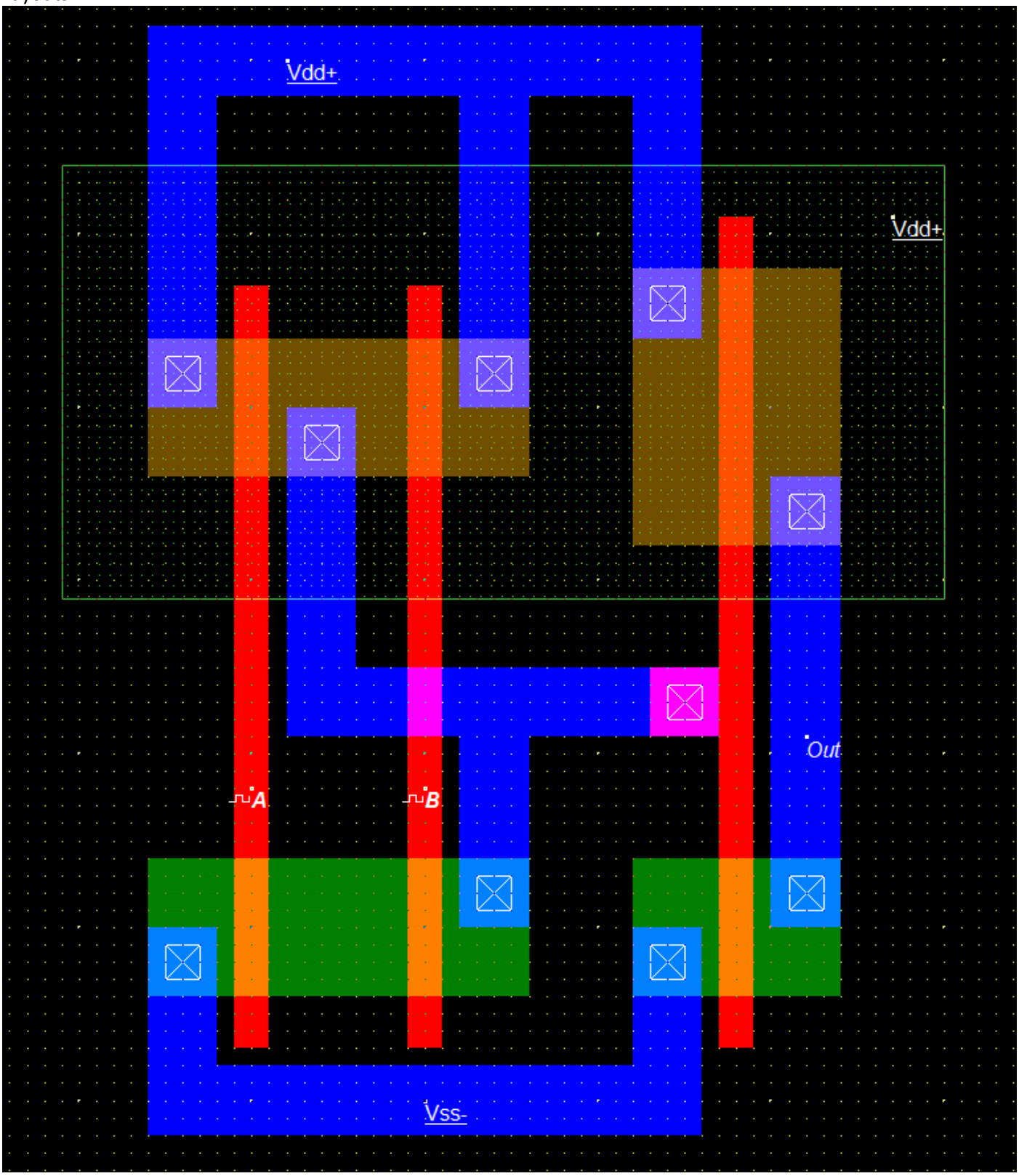
Για το β)

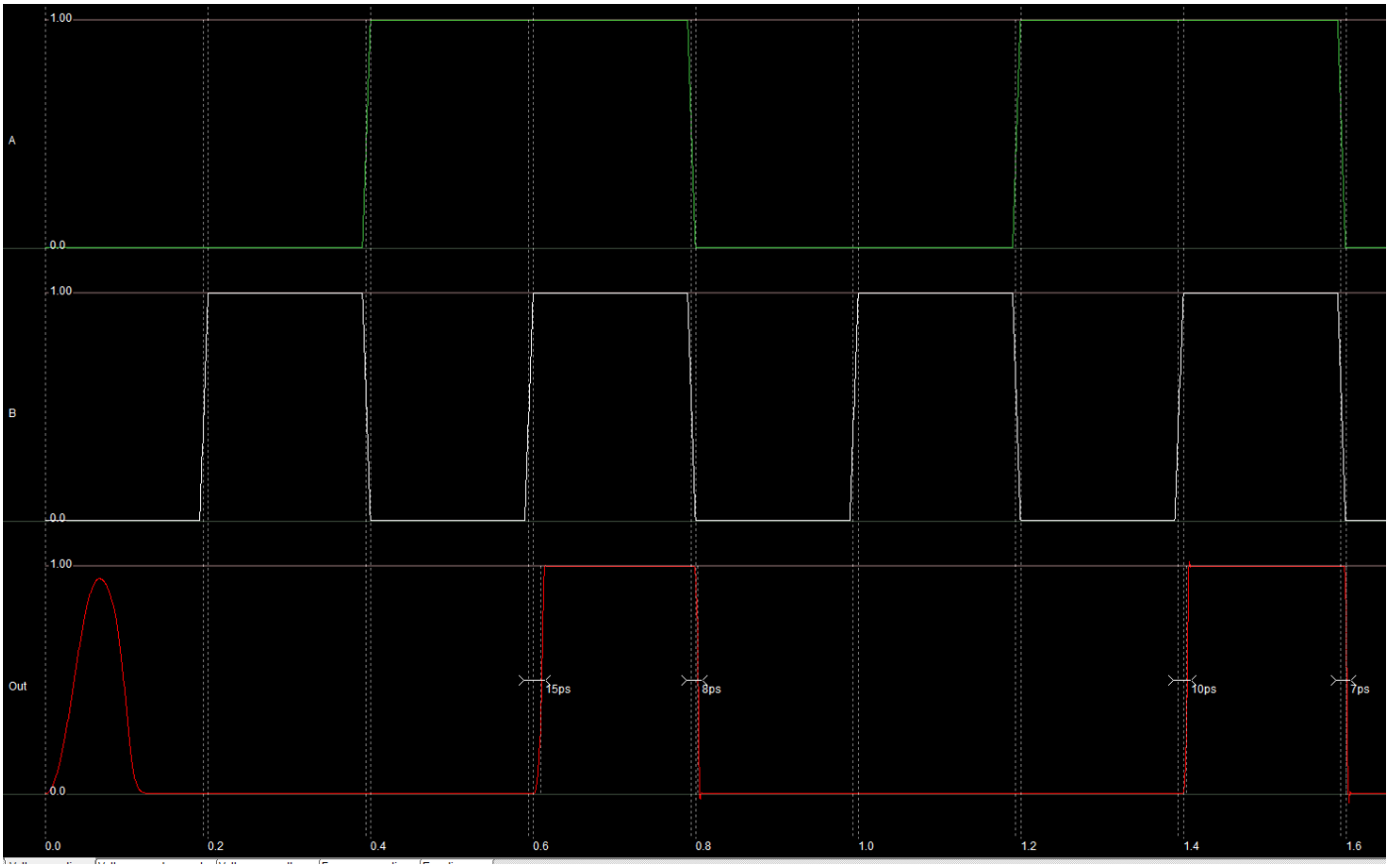
G	$\frac{5}{3}$
H	$\frac{12}{3} = 4$
B	1
F	$\frac{5}{3} * 1 * 4$
f	$\sqrt[2]{\frac{20}{3}} = 2.58$
P	$2 * 1 = 2$
D	$2 * \sqrt[2]{\frac{20}{3}} + 2 = 7.16$
y	$\frac{12 * \frac{5}{3}}{2.58} = 7.7C$

From the theoretical calculations we observe that the first circuit is faster.

MICROWIND :

Layouts :





Εργαστηριακή Άσκηση 4

Αναλογίες στις διατάξεις:

NOT => $W_p = 2\kappa \cdot W_{min}$, $W_n = \kappa \cdot W_{min}$ (1)

NAND => $W_p = 2n \cdot W_{min}$, $W_n = 2n \cdot W_{min}$ (2)

NOR => $W_p = 4q \cdot W_{min}$, $W_n = q \cdot W_{min}$ (3)

Στην πρώτη άσκηση, βρήκαμε ότι $X = 6\lambda$ (για την NOT)

Άρα, έχουμε την εξίσωση από το (1) => $2p_{mos} + 1n_{mos} = 6\lambda$ =>

=> $p_{mos} = 2\lambda = n_{mos}$

(Πρέπει $p_{mos} = n_{mos}$)

Ισχύει ότι $(=4\lambda)$

Άρα, για την NOT έχω: $W_p = 2 \cdot 2\lambda = 16\lambda$ και $W_n = 2\lambda = 8\lambda$

~~Επίσης, το γ το βρήκαμε~~

Επίσης, η NAND ίση με 4λ, άρα: $2p_{mos} + 2n_{mos} = 4\lambda$ => $p_{mos} = n_{mos} = \lambda$

Άρα, $W_p = 2 \cdot \lambda = 8\lambda$ και $W_n = 2 \cdot \lambda = 8\lambda$

EXERCISE 2 :

(i)

(a) 1 NAND of 6 inputs and 1 NOT:

G	$\frac{8}{3} * 1 = \frac{8}{3}$
H	H
B	$1 + 1 = 1$
F	$\frac{8}{3} * H$
P	$6 + 1 = 7$

(b) 2 NAND of 3 inputs and 1 NOR of 2 inputs:

G	$\frac{5}{3} * \frac{5}{3} = \frac{25}{9}$
H	H
B	$2 * 1 = 2$
F	$\frac{50}{9} * H$
P	$3 + 2 = 5$

(c) 3 NAND of 2 inputs and 1 NOR of 3 inputs:

G	$\frac{4}{3} * \frac{7}{3} = \frac{28}{9}$
H	H
B	$3 * 1 = 3$
F	$\frac{84}{9} * H$
P	$2 + 3 = 5$

(d) 2 NAND of 3 inputs and 2 NOT and 1 NAND of 2 inputs and 1 NOT:

G	$\frac{5}{3} * 1 * \frac{4}{3} * 1 = \frac{20}{9}$
H	H
B	$2 * 2 * 1 * 1 = 4$
F	$\frac{80}{9} * H$
P	$3 + 1 + 2 + 1 = 7$

(ii)

For H=5:

(a)

F	$\frac{40}{3}$
f	3.65
Dmin	$2 * 3.65 + 7 = 14.3$

(b)

F	$\frac{250}{9}$
f	5.3
Dmin	$2 * 5.3 + 5 = 15.6$

(c)

F	$\frac{420}{9}$
f	6.8
Dmin	$2 * 6.8 + 5 = 18.6$

(d)

F	$\frac{400}{9}$
f	2.6
Dmin	$4 * 2.6 + 7 = 17.4$

So, the fastest design is (a).

For H=18:

(a)

F	48
f	6.9
Dmin	$2 * 6.9 + 7 = 20.8$

(b)

F	100
f	10
Dmin	$2 * 10 + 5 = 25$

(c)

F	168
f	13
Dmin	$2 * 13 + 5 = 31$

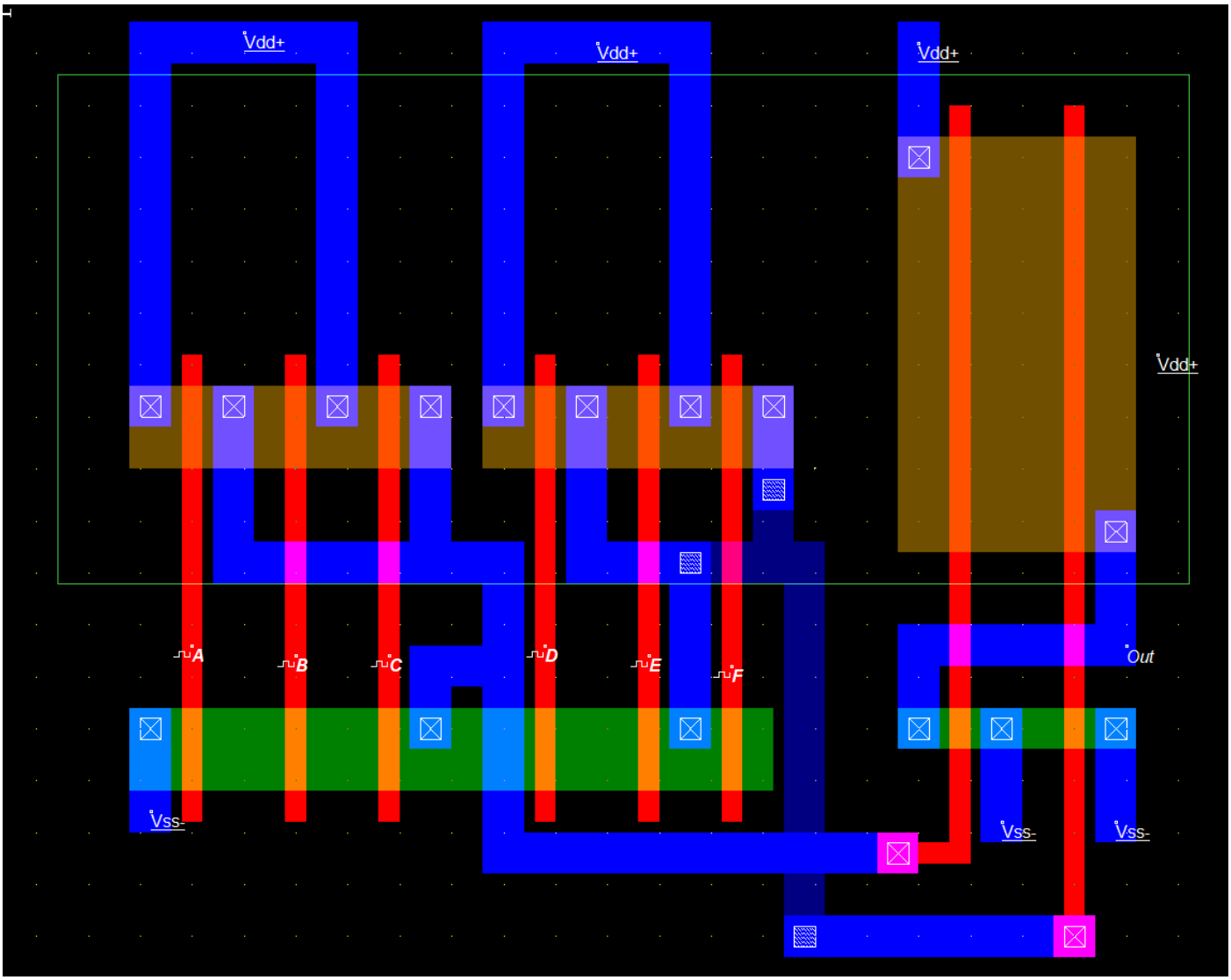
(d)

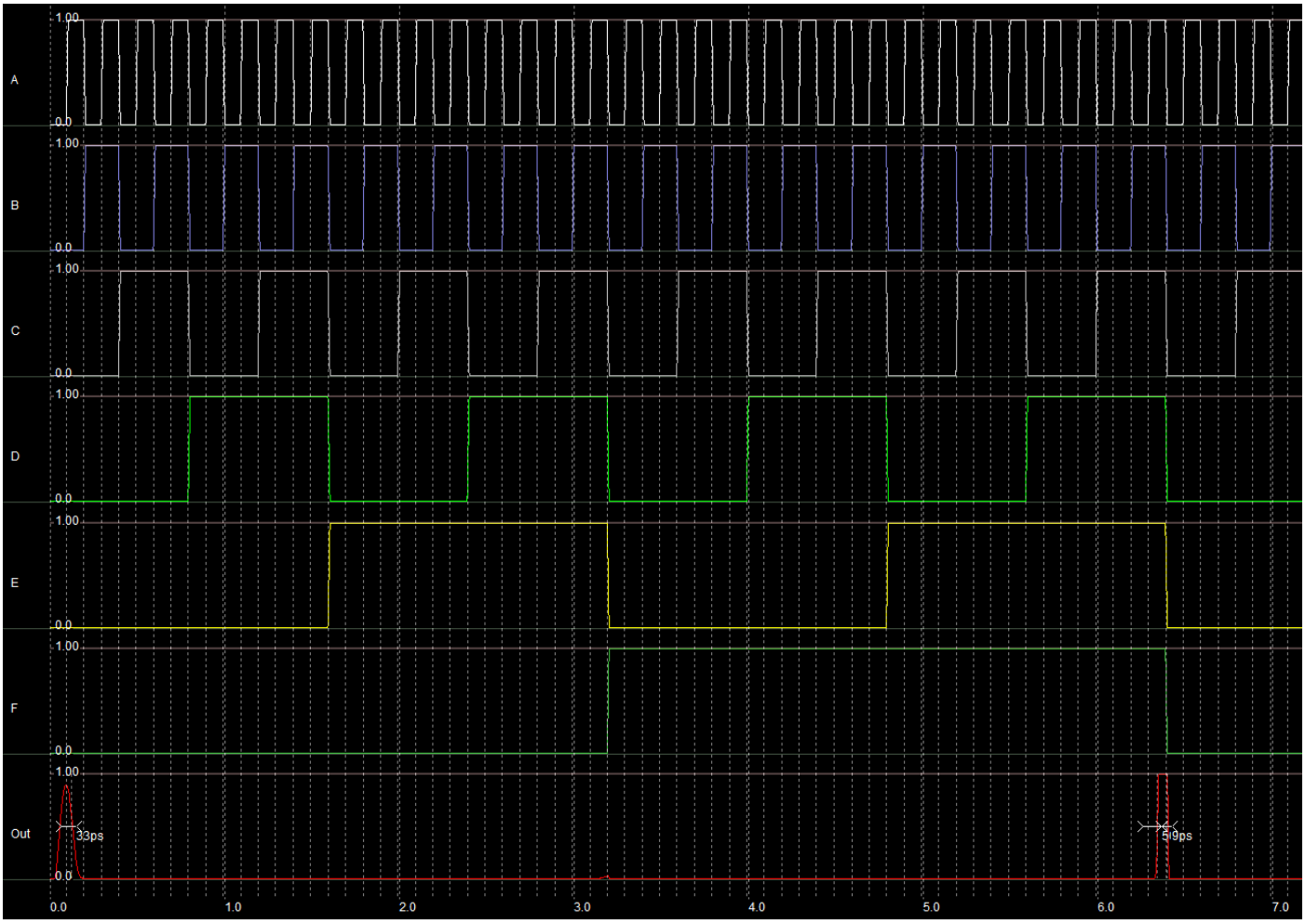
F	160
f	3.5
Dmin	$4 * 3.5 + 7 = 21$

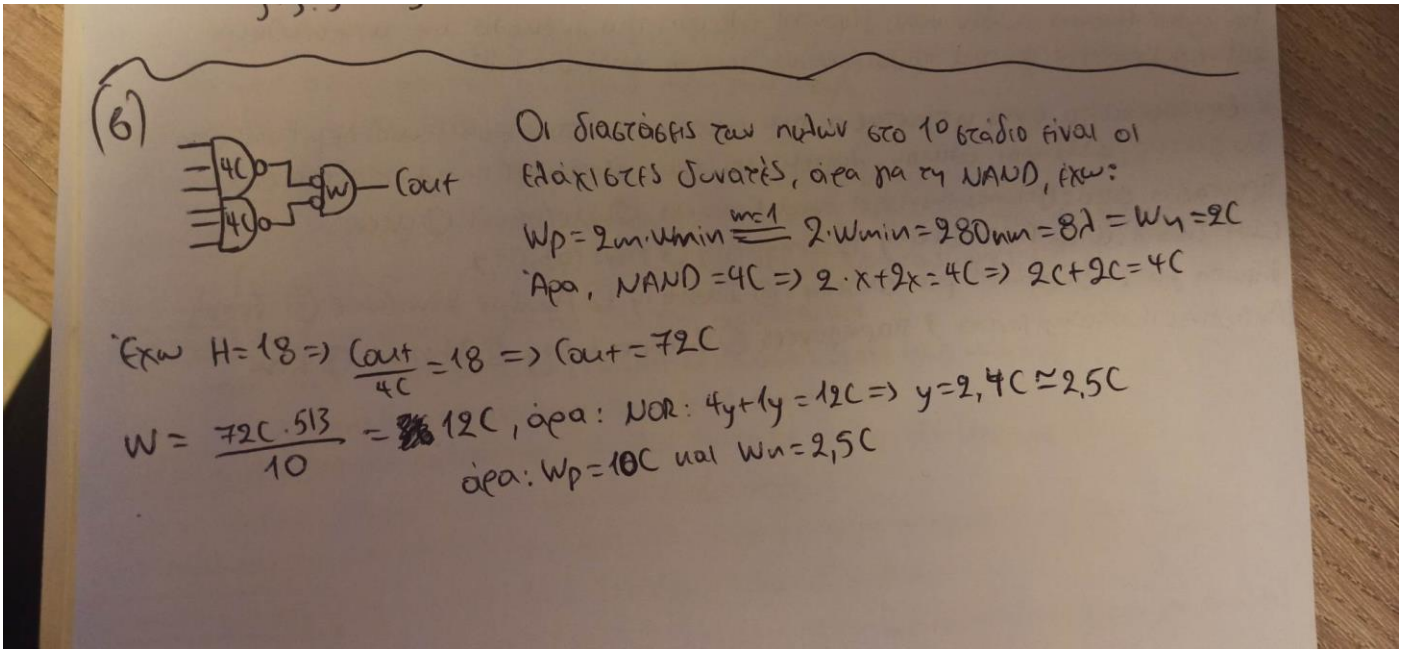
So, the fastest design is (a), with very little difference from (d).

(iii) We use cmos65n technology

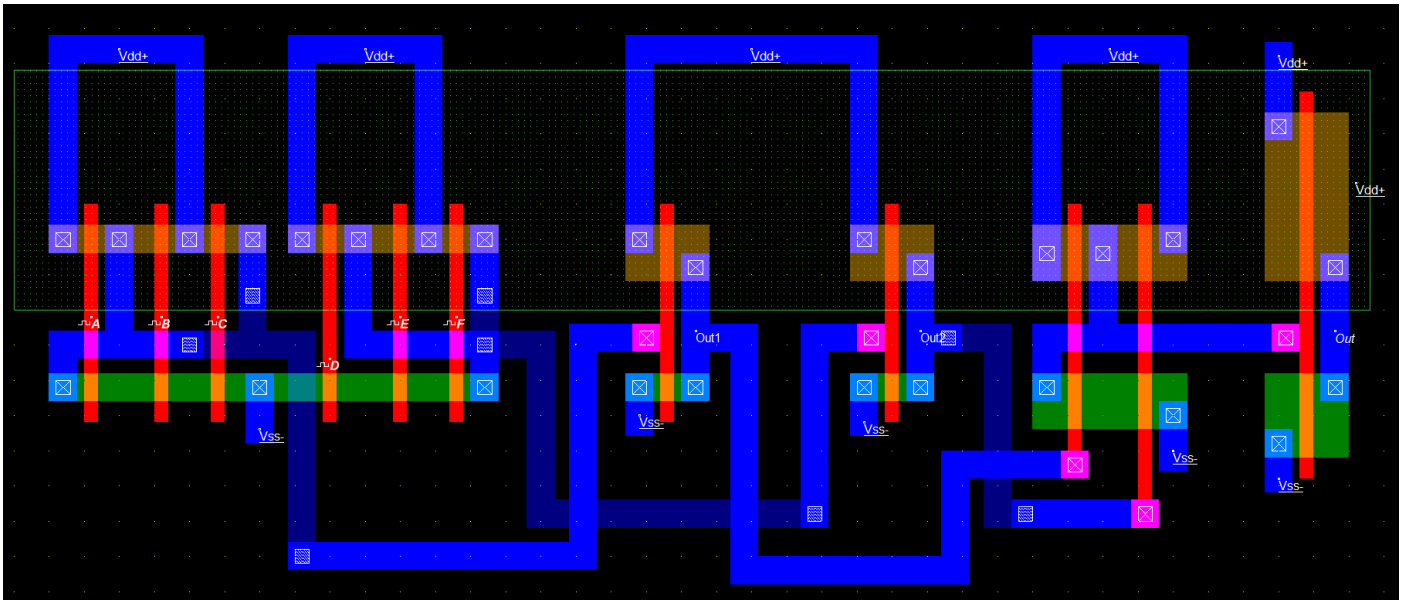
(b)

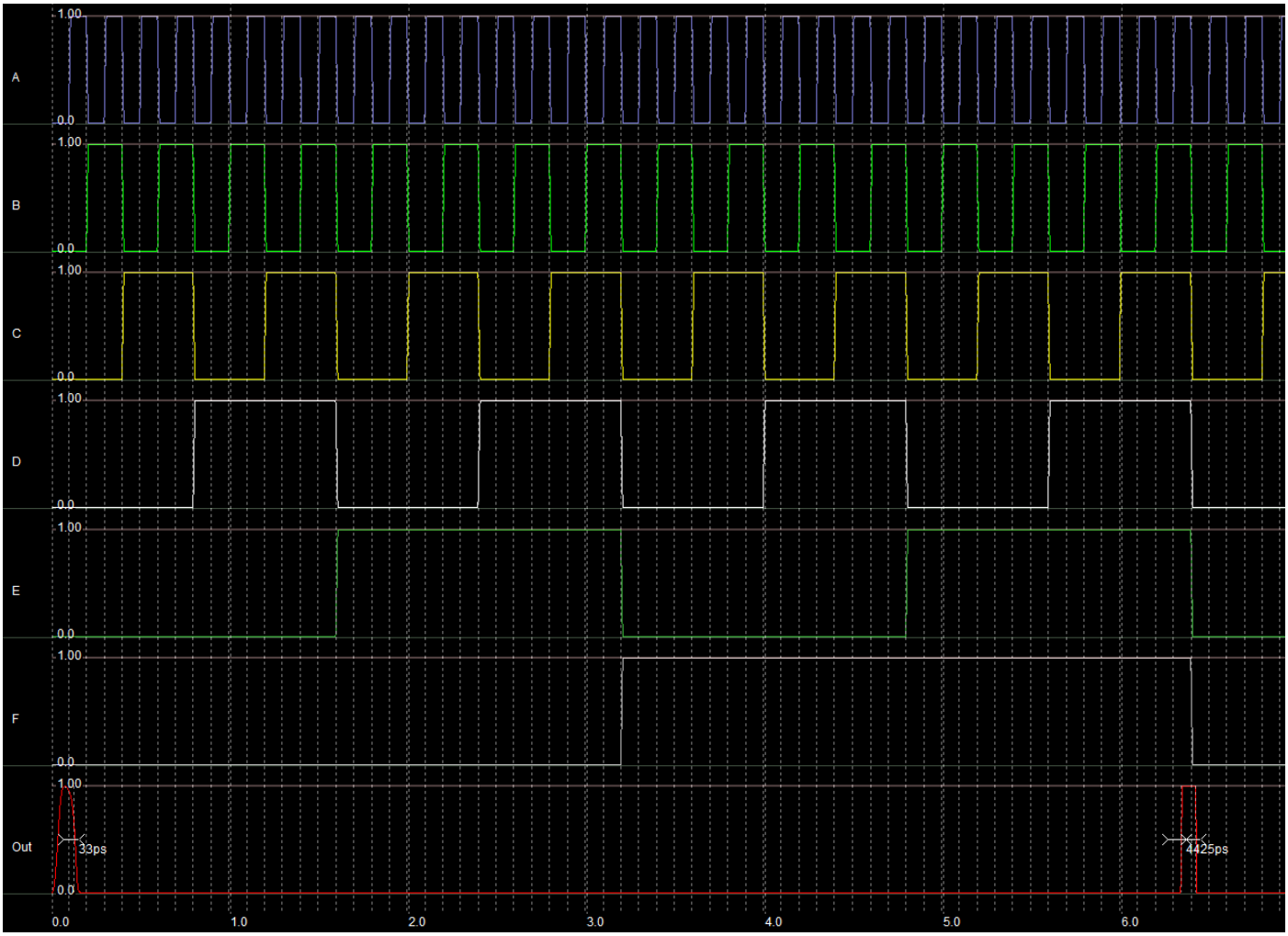



A
B
C
D
E
F
Out
1.00
0.0
33ps
5.9ps
0.0
1.0
2.0
3.0
4.0
5.0
6.0
7.0

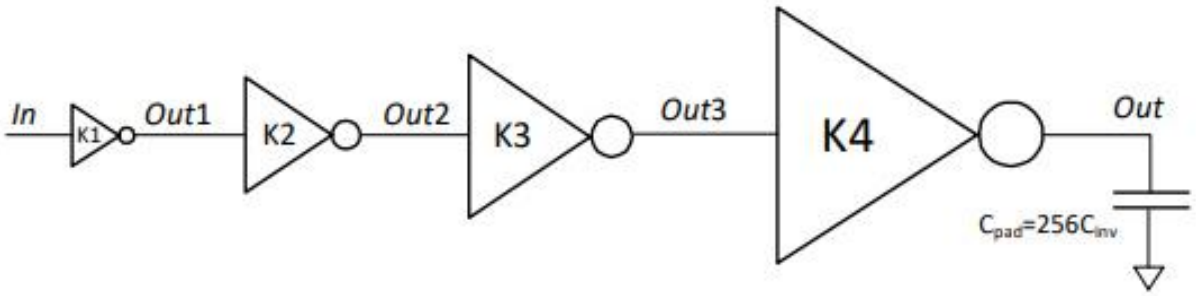

(6)
4C
4C
W
Cout
Οι διαστάσεις των πυλών στο 1ο στάδιο είναι οι ελάχιστες δυνατές, άρα για τη NAND, έχω:
Wp = 2m · Wmin (m=1) 2 · Wmin = 280nm = 8λ = W4 = 2C
Άρα, NAND = 4C ⇒ 2 · x + 2x = 4C ⇒ 2C + 2C = 4C
Έχω H = 18 ⇒ Cout / 4C = 18 ⇒ Cout = 72C
W = 72C · 513 / 10 = 12C, άρα: NOR: 4y + 1y = 12C ⇒ y = 2,4C ≃ 2,5C
άρα: Wp = 10C και Wn = 2,5C

(d)


Vdd+
Vdd+
Vdd+
Vdd+
Vdd+
Vdd+
A
B
C
D
E
F
Out1
Out2
Out
Vss-
Vss-
Vss-
Vss-
Vss-


A
B
C
D
E
F
Out
1.00
0.0
33ps
4425ps
0.0
1.0
2.0
3.0
4.0
5.0
6.0

EXERCISE 3 :



G	1
H	256
B	1
F	256
f	4
P	4
D	20

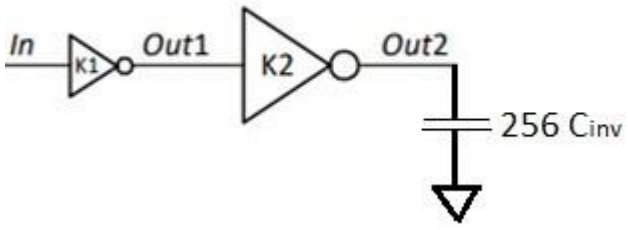
From the above it follows that:

$$\mathrm{K4} = \frac{256}{4} = 64$$

$$\mathrm{K3} = \frac{64}{4} = 16$$

$$\mathrm{K2} = \frac{16}{4} = 4$$

$$\mathrm{K1} = \frac{4}{4} = 1$$



G	1
H	256
B	1
F	256
f	16
P	2
D	34

From the above it follows that:

$$\mathrm{K2} = \frac{256}{16} = 16$$

$$\mathrm{K1} = \frac{16}{16} = 1$$