

1st Laboratory Exercise

Familiarizing yourself with Microwind

1 General introduction

The process of designing digital integrated circuits (digital design), especially at large scales of integration (VLSI) is a complex sequence of steps aimed at the optimal transition from specification to implementation. These steps can be arranged in different subtractive levels, in the form of a pyramid. Higher abstraction levels are characterized by high abstraction and concise descriptions. The opposite occurs at lower abstraction levels. In the laboratory part of the course we will deal with the lowest abstract level of design, called *the physical design level*, and deals with the construction and control of the geometric masks required to create after a series of processes semiconductor devices on a thin slice of silicon.

2 Subject of the first laboratory exercise

The purpose of the first laboratory exercise is to get to know the software package MICROWIND for designing, testing and simulating VLSI circuits. The MICROWIND project (<http://www.microwind.org>) was initiated at the University Institut National des Sciences Appliquées (INSA) in Toulouse, France as an academic aid for the respective course. Its initial versions had several shortcomings and followed simplified design methodology. However, in recent years and in collaboration with the semiconductor and digital circuit manufacturing company STMicroelectronics (<http://www.st.com>), the MICROWIND program has been commercialized and significantly improved. Its main advantage over other competing tools is its compact operation, that is, all the basic functions of physical design are covered by a main program with a menu of command selections and a toolbar.

Version 3.1 of the MICROWIND program is available at the laboratory, which you can obtain and install. Of course, your presence in the laboratory is mandatory, where the introduction to each laboratory exercise, the solving of questions, the examination and presentation of special topics and techniques will take place. You can find useful information on the laboratory course page <https://eclass.upatras.gr/> as well as submit the group reports for each laboratory exercise electronically.

With the MICROWIND program you can:

- Construction of a physical design (layout) of an integrated circuit in detail (full custom), transistor by transistor.
- Hierarchical physical design construction from ready-made physical blueprints of subunits, the generator physical MOS transistor designs, or Verilog language descriptions.
- Control of physical design and control of compliance with the design rules (minimum required dimensions or distances between different shapes) of the implementation technology.
- Measurements to derive characteristic sizes and operational parameters of CMOS circuits.
- SPICE level simulation of the circuit corresponding to the physical design.

In the first lab exercise, which is introductory, you will complete the design and testing of a CMOS inverter and a transmission gate. You will become familiar with the basic geometric characteristics of a MOS transistor and the interactions between them as well as their connection to create CMOS circuits. You will be able to measure both in the physical design and in the simulation some characteristic sizes.

3 Introduction to the MICROWIND program

The main screen of the MICROWIND program is shown in Figure 1.1 below.

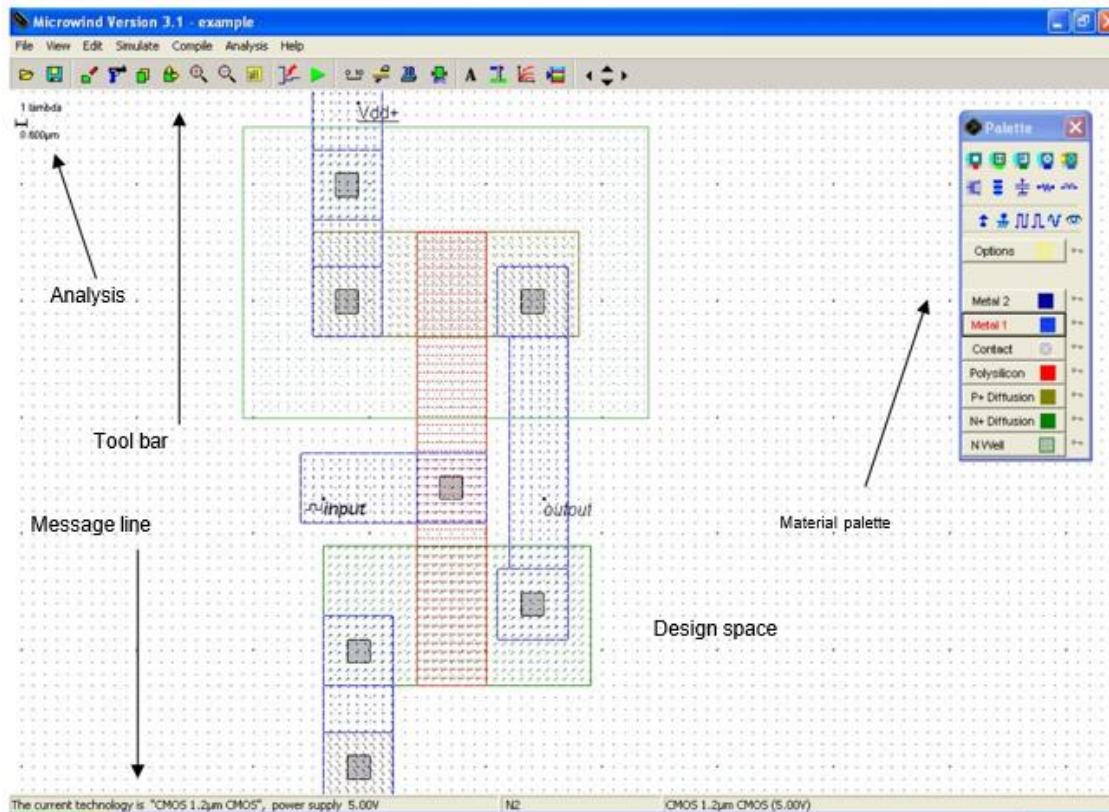






















Figure 1.1: The main screen of MICROWIND

The central and main screen includes all the elements that help build the physical design of a CMOS circuit. The largest part of it constitutes the drawing space on which the required geometric shapes of a physical design must be drawn. The drawing space can also have the drawing frame visible, whose resolution is indicated in its upper left corner and changes according to changes in focus (zoom) of the physical drawing. As with most programs, so does MICROWIND includes a command menu, a toolbar, and a message bar. It also includes a material palette, which changes depending on the implementation technology (each implementation technology has different materials, like for example more layers of metal). This palette also includes some complex design tools such as contact generators, MOS transistor generator, passive element generators (resistances, capacitances, inductances) and tools for defining the inputs and outputs of a circuit. Next, the toolbar and material palette will be briefly introduced.

For more details you can refer to the user guide of the program MICROWIND.

The basic design and control functions of the MICROWIND program can be executed by pressing the toolbar buttons. The table below gives a brief description of each.

Button Function

	Physical design file retrieval.
	Save physical design file.
	Draw a rectangle with the material selected from the material palette.
	Delete elements from the physical drawing that are selected either by simply pressing the left mouse button or by enclosing them in a rectangle with the help of the mouse.
	Copy elements from the physical drawing selected by enclosing them in a rectangle with the help of the mouse.
	Extension of a side to a rectangular element of the physical design. The side is selected by simply pressing the left mouse button.
	Increased focus on physical design.
	Decrease focus on physical design.
	Change the focus to the physical design so that all constructed elements are visible.
	Illumination of physical design elements that are on a common conductive path with a point selected by pressing the left mouse button. Very useful for locating short circuits.
	Start simulation.
	Draw a horizontal and/or vertical measurement ruler.
	Cross-sectional view of physical plan.
	Showing the physical design in 3 dimensions step by step, in relation to the various processes of creating semiconductor elements in silicon.
	Check design rules of the selected implementation technology.
	Placing text in the physical design.
	Creating vias between different layers of materials in the physical design.
	Study and variation of the characteristic sizes of a MOS transistor from the physical design.
	Show the material palette.
	Move the physical pattern opposite the selected direction.

The material palette is the second basic design tool of the program MICROWIND. Its form (for implementation technology with two metal layers) is given in Figure 1.2.



Figure 1.2: The material palette

The lower part of the material palette includes buttons with all available materials for each implementation technology. By selecting one of them and the draw parallelogram button from the toolbar, we draw a parallelogram with the corresponding material (eg polysilicon, n-type diffusion, etc.). The keys next to each material disable all objects designed with that material, making it easier to change the rest. The upper part of the palette includes some complex design tools such as contact generators between layers of different materials, MOS transistor generator, passive element generators (resistances, capacitances, inductances) and tools for defining the inputs and outputs of a circuit. The most commonly used are the buttons on the first row that make contacts between levels and from the buttons on the last row, the first one sets the *Vdd supply point*, the second one sets the *Vss supply point*, the third one sets the pulse input point and the latter defining an exit point. For example, pressing the set pulse train input button displays the window of Figure 1.3 with fields and buttons from which all parameters of the pulse train are defined.

Accordingly, pressing the output definition button displays the window of figure 1.4. Notice in both windows the bottom right button that says “*Visible in simu*”. In case it says “*Not in simu*”, the corresponding input or output will not appear in the simulation waveforms. Switching between the two states is done by successive button presses.

Add a Clock

Label name :

DC Supply | **Clock** | Pulse | Sinus | Variable | Ground | PWL | Math

Parameters

Level 1 (V):

Level 0 (V):

Time low (tl): ns

Rise time (tr): ns

Time high (th): ns

Fall time (tf): ns

Slower Faster ~Last Clock

☒ Assign ☒ Cancel ☒ Visible in simu

Figure 1.3: Input definition with pulse train

Add simple text

Label name :

DC Supply | Clock | **Pulse** | Sinus | Variable | Ground | PWL | Math

Parameters

"Not in Simu": signal invisible at the next simulation
 "Visible in simu": signal waveform visible at the next simulation

☒ Assign ☒ Cancel ☒ Visible in simu

Figure 1.4: Output definition

Finally, Figure 1.5 shows the simulation window for the circuit of an inverter, displayed by pressing the corresponding button from the toolbar. The window displays all input or output waveforms that have the "Visible in simu" and on the far right has a series of buttons and option fields. Of these, the "Time Scale" field is very useful, which defines the visible part of the waveforms as well as the direction buttons below it that time shift the waveforms. The time intervals indicated on the output waveform are the rise and fall delay times between the input and output waveforms and their display is selected from the fields on the top right.

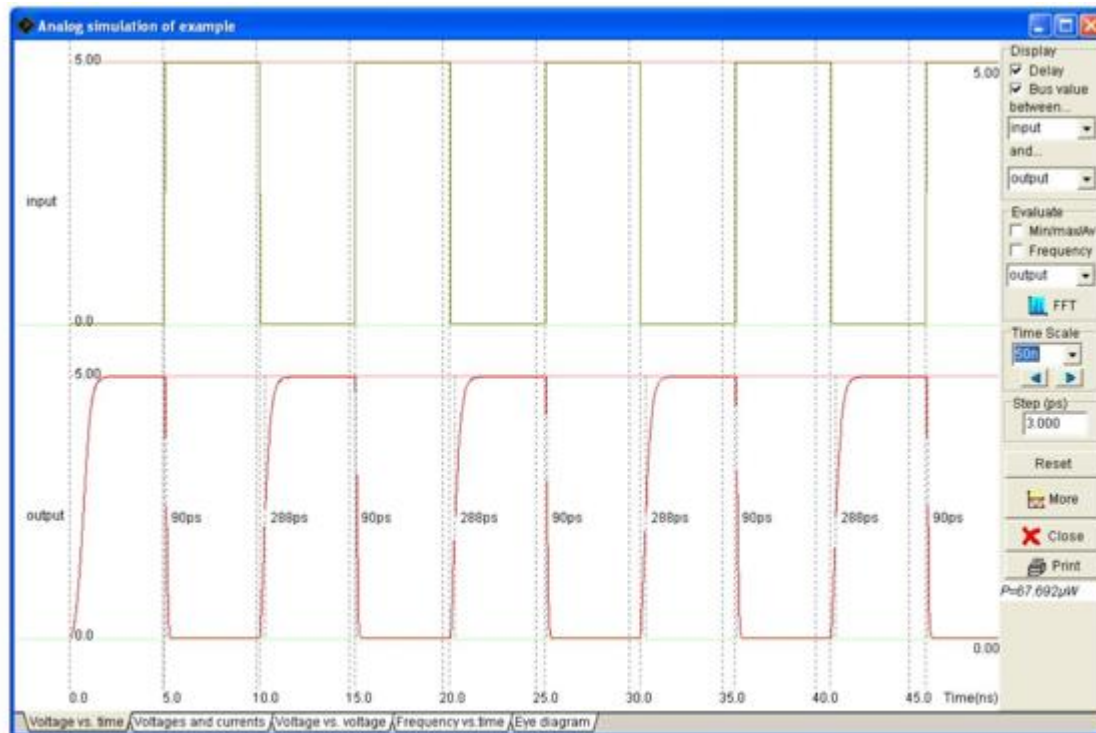


Figure 1.5: Simulation

EXERCISES

- 1 Design a CMOS inverter in detail, that is to use only the pallet materials (*Full Custom*), in *cmos65n* technology (65nm *technology*, $\gamma=35\text{nm}$) with the following dimensions: $W_p=280\text{nm}$, $W_n=140\text{nm}$, $L_p=L_n=70\text{nm}$, where W is the transistor channel width and L is the transistor channel length. Then simulate the circuit with a square wave input (0 - 1V).
- 2 Design CMOS *transmission gate* in detail (Fig. 1.7), in *cmos65n* technology (65nm *technology*, $\gamma=35\text{nm}$) and dimensions: $W_p=280\text{nm}$, $W_n=140\text{nm}$, $L_p=L_n=70\text{nm}$, where W is the width of the transistor channel and L the length of the transistor channel. Use the previous circuit as an inverter (Subject 1). Also simulate the circuit with a square wave input (0 – 1V) with the gate open ($C=1$) and closed ($C=0$).

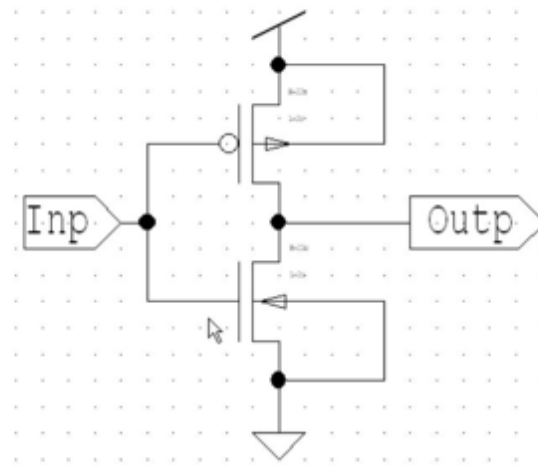


Fig. 1.6: CMOS inverter schematic diagram

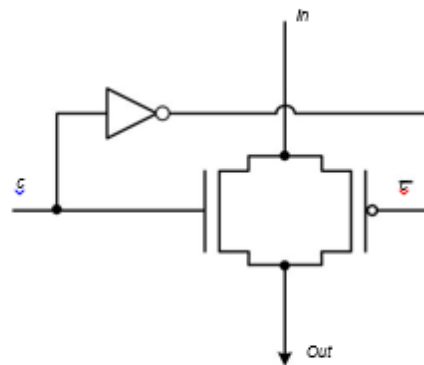


Fig. 1.7: Schematic diagram of CMOS transmission gate

