4th Laboratory Exercise

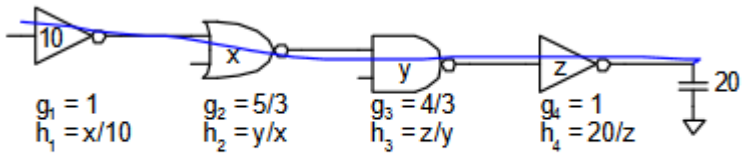
Theoretical/ practical calculation of delays in multistage logic networks

1 Theory In
the previous exercise, the linear model for calculating logic gate delays was used, specificallythe formula:

$$d = gh + p$$

where *d* is the calculated gate propagation delay, *g* is the logic load, *h* is the electrical load and
p is the intrinsic parasitic delay. These parameters are calculated from the physical characteristicsof the transistor.

The logic load *(g)* is generalized to the case of multistage logic networks. For example, Figure
4.1 shows a 4-stage logic network with different gates at each stage. Let each gate exhibit input capacitance as listed inside the gate. Then, the logic *(g)* and electrical load *(h)* are calculated aslisted below each gate. Notice that the logic load is independent of the gate dimensions and is the one calculated for the case of unit active resistors (see previous exercise). Instead, the electrical load depends on the input resistances and therefore on the gate dimensions.



Σχήμα 4.1: Λογικό δίκτυο πολλών σταδίων

For the entire network, logical load G, electrical load *H* and load *F* are defined by the followingformulas:

$$G = \prod g_i$$

$$H = \frac{C_{out-path}}{C_{in-path}}$$

$$F = \prod f_i = \prod g_i h_i$$

In the case of the network in Figure 4.1, relation (4) can also be written as *F* ÿ *GH* , but it

is not general and specifically does not apply in cases where there are branches in some stages. For example, in figure 4.2 for the path defined by the dashed line it is calculated G=1*1=1, H=90/5=18, GH=1*18=18, h1=(15+15)/5= 6, h2=90/15=6, *F=g1*h1*g2*h2=36=2GH.*

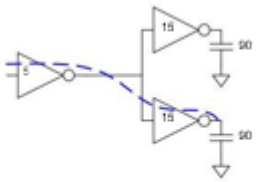


Figure 4.2: Multistage logic network with branches

For the case of networks with alternative paths, a new quantity is defined, the branching load, which for each stage thatincludes *n* alternative paths of which we are interested in path 1, is defined:

$$b = \frac{C_{path_1} + C_{path_2} + \cdots + C_{path_n}}{C_{path_1}}$$

For a multi-stage network the total branch load is defined as:

$$B = \prod\prod b_i$$

Finally, the load of a network of multiple stages and alternative paths is given by the formula

$$F = GBH$$

The load of a network *F* is a quantity that depends only on the network topology and the input and output capacities. Itis used to calculate the propagation delay of the network, derived from the formulas

$$P = \sum p_i$$
$$D_F = \sum f_i$$
$$D = D_F + P$$

where the parasitic delays *pi* are calculated as is the logic load without considering the dimensions of the transistors,but referring to the case of unit active resistors (see previous exercise). For example, in the circuit of Figure 4.1:

$$P = \sum_{i=1}^{4} p_i = 1 + 2 + 2 + 1 = 6$$
$$D_F = \sum_{i=1}^{4} g_i h_i = \frac{x}{10} + \frac{5}{3} \cdot \frac{y}{x} + \frac{4}{3} \cdot \frac{z}{y} + \frac{20}{x}$$

$$\hat{f} = \sqrt[n]{F}$$

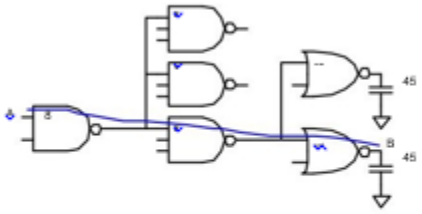
From this relation the central relation in all logical load theory is derived, that the minimum network delay is given by the formula:

$$D_{\min} = n\sqrt[n]{F} + P$$

for the calculation of which the dimensions of the transistors are not required. These are calculated a posteriori for each stage, starting from the output capacitance and successively using the formula:

$$\hat{f} = gh = g\frac{C_{out}}{C_{in}} \Rightarrow C_{in} = \frac{gC_{out}}{\hat{f}}$$

For example, in figure 4.3 we can calculate all the values on the right.



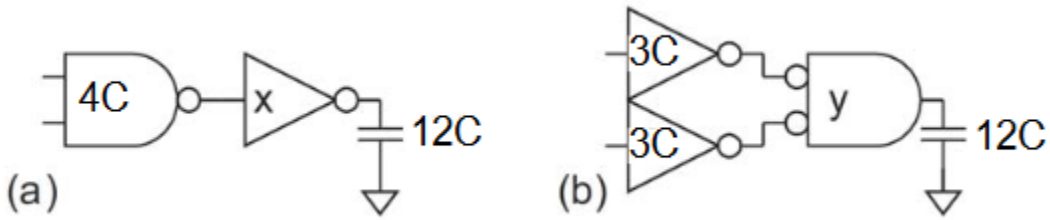
G=4/3*5/3*5/3=100/27
H=45/8
B=1*3*2=6
F=125
f=5
P=2+3+2=7
D=3*5+7=22
y=(45*5/3)/5=15
x=((15+15)*5/3)/5=10

Figure 4.3: Example calculations

From *x* and *y* we can choose the appropriate dimensions of the transistors and construct the optimal layout of the circuit.

1 The requirements of the laboratory exercise

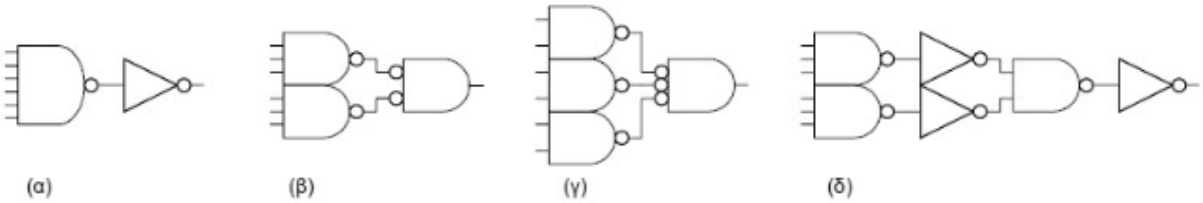
1. Consider the two designs of a two-input AND gate shown in the figure below (the 2nd figure uses a NOR gate). Calculate the total path load, delay, and input capacitances *x* and *y* for each case. Which circuit is faster? Design the corresponding layout and do experimental verification with simulation.


4C
x
12C
(a)
3C
3C
y
12C
(b)

Note: For the theoretical calculation start from formula (11), as in the example in figure 4.3. For the layout designs, use any integration technology you wish (between *120nm, 90nm, 65nm, 45nm* and *22nm)* round the theoretical results to the nearest integer (where needed) and calculate the dimensions of the gates that will be needed taking into account and respecting theproportions : *Wp=2kÿWmin, Wn=kÿWmin* for the inverter, Wp=2mÿWmin, Wn=2mÿWmin for the 2-input NAND and Wp=4qÿWmin, *Wn=qÿWmin* for the 2-input NOR

of inputs, where k, m, *q* are integers and *Wmin* the nmos transistor width of the minimum inverter for the selected technology (eg for cmos65n, Wmin=140nm while Lp=Ln=70nm). Finally,the capacitance C corresponds to the gate capacitance of nmos, the minimum inverter.

2. Consider four designs of a 6-input AND gate as shown infigure below.



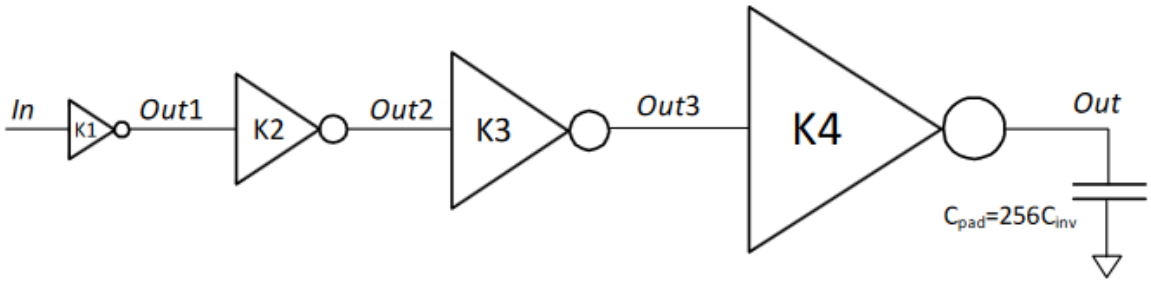
(i) Develop an expression for the delay of each path, if the electrical path effort is H.

(ii) What is the fastest design for *H* = 5 and for *H* = 18? For your convenience, create a calculation table of these delays (spreadsheet) with columns for the values of G, P, N and for the four cases a-d, which make up the lines of the table. Explain your conclusions.

(iii) For H=18 draw the layout in cases b and d and do experimental verification by simulation.

Note: You can use any technology you want (between *120nm, 90nm, 65nm, 45nm* and *22nm).* Calculate the dimensions of the gates that will be needed in the design of the optimal layouts starting again from the formula (11). Simulate different H, just change the output load. The dimensions of the transistors should be as defined in the previous exercise. Consider the 1st stage gates in all cases to be the minimum possible.

2. Design in any technology you want (between *120nm, 90nm, 65nm, 45nm* and *22nm)* a minimum CMOS K1 inverter with the following dimensions: Wn=4ÿ, Ln=2ÿ and Wp=8ÿ, Lp=2ÿ. Calculate the delay introduced by a series of inverters K1, K2, K3, K4 when driving a load Cpad 256 times the input capacitance Cinv of inverter K1. Calculate the minimum-optimal total delay from *In* to *Out* for 4 stages of inverters theoretically and experimentally as well as the dimensionsof the transistors. If the tiers are two (K1, K2) what are the corresponding (optimal) results? Draw conclusions.



Hint: Plan the layout of the powerful inverters so that they do not occupy a large area vertically. Such alimitation comes in the case of standard cells where the cells are all the same height.