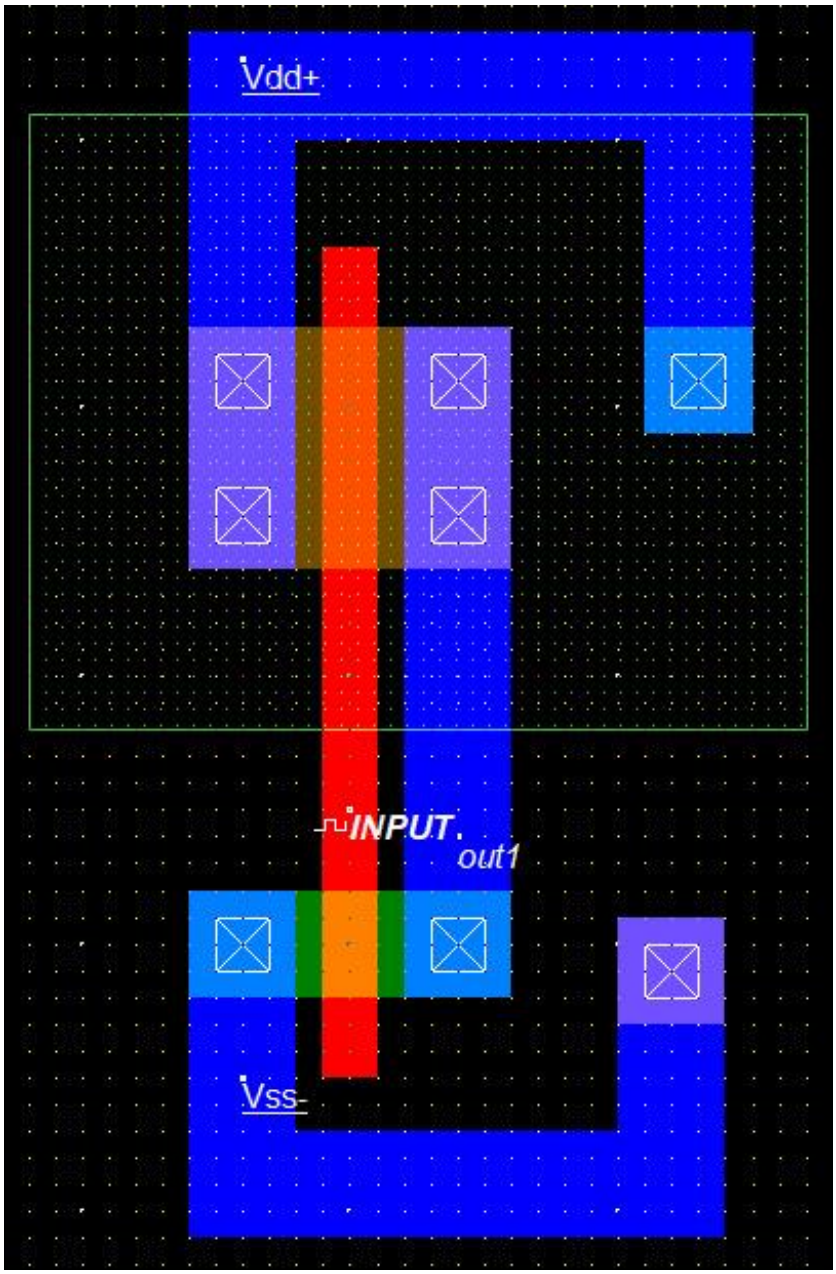
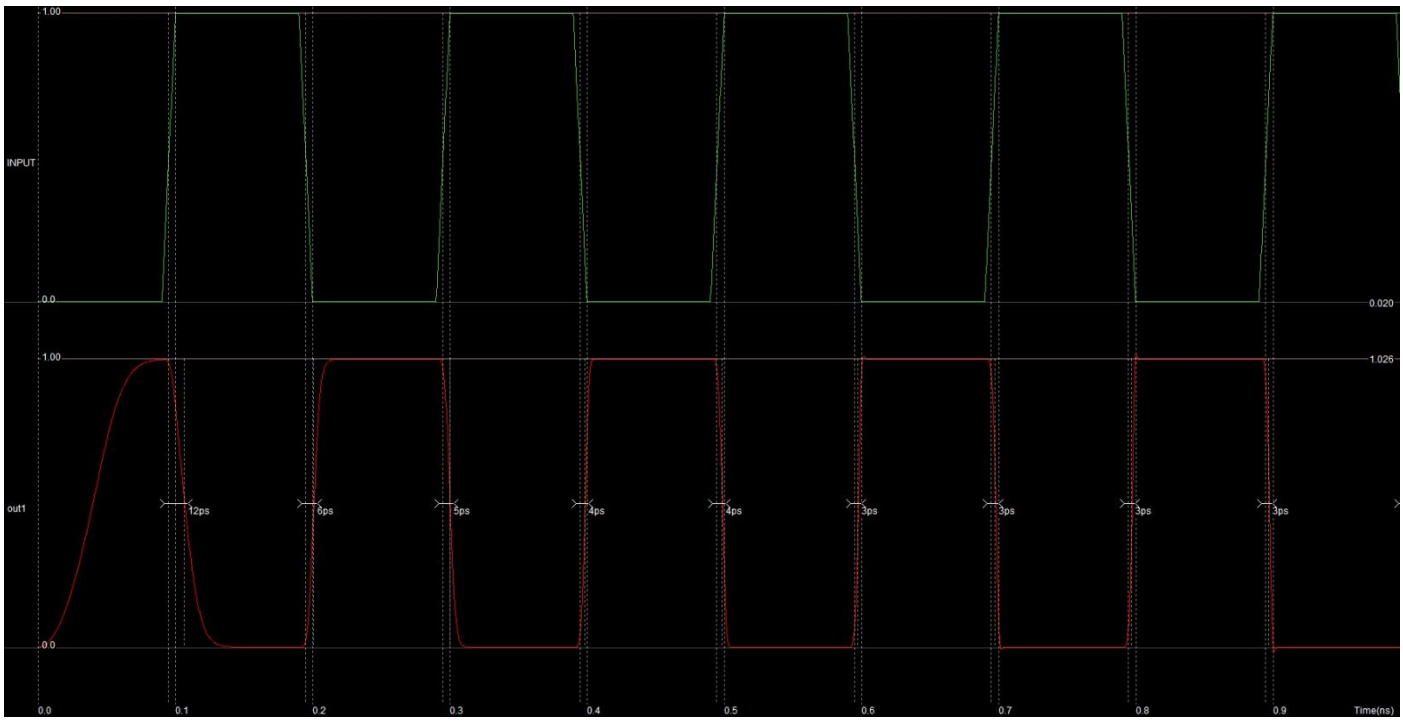
1st VLSI Laboratory Exercise

EXERCISE 1:

a)



b)

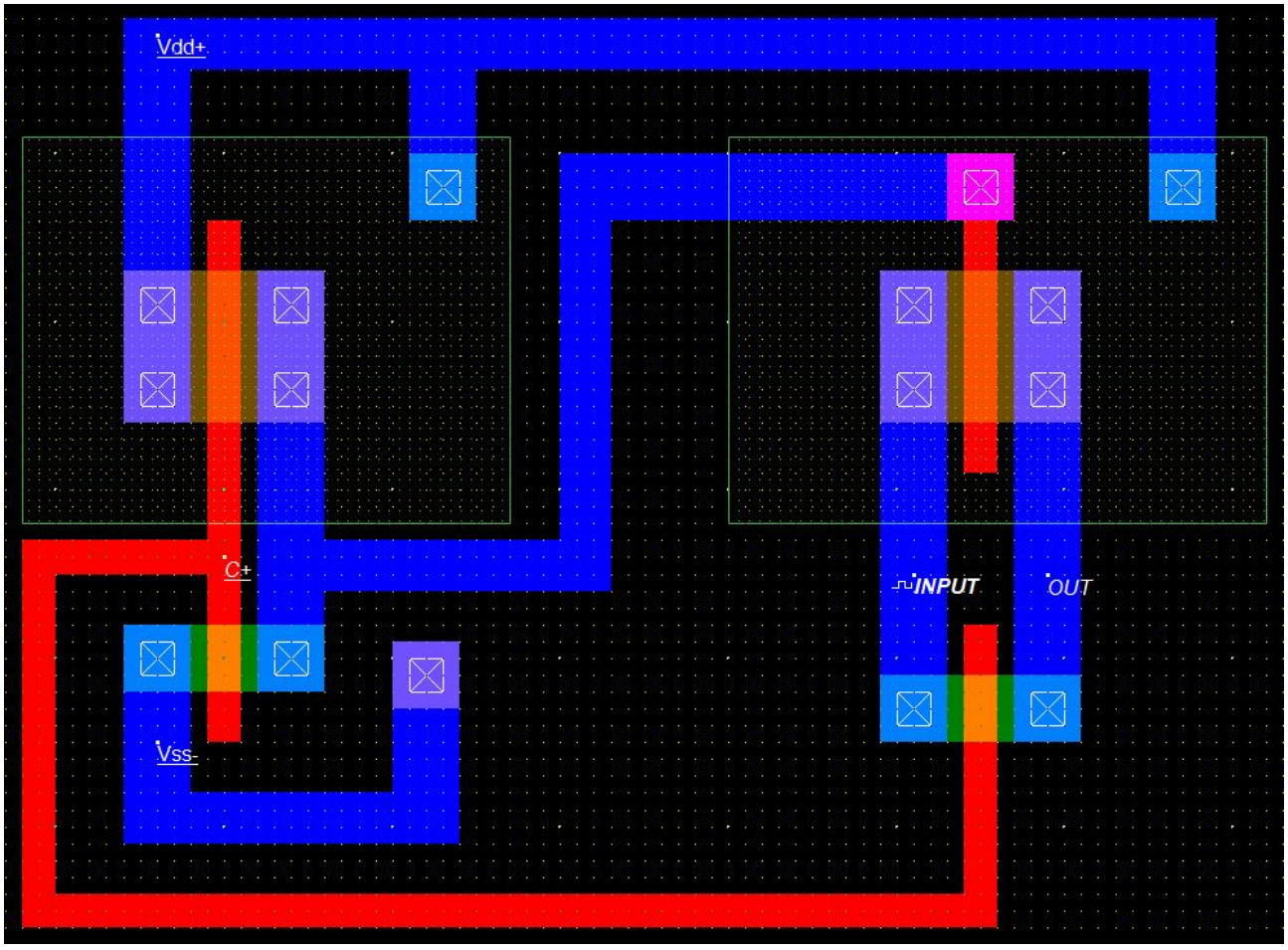


c)

As we can see in the simulation, the CMOS inverter works correctly. For the input of the circuit we have placed a fixed pulse train. The output of the circuit should be the opposite of the input. So, whenever the input has the value 1, the output will have the value 0 and correspondingly the opposite. The delay observed in the output of the circuit is due to the fact that it takes time for the capacitances of the logic circuit to charge and discharge.

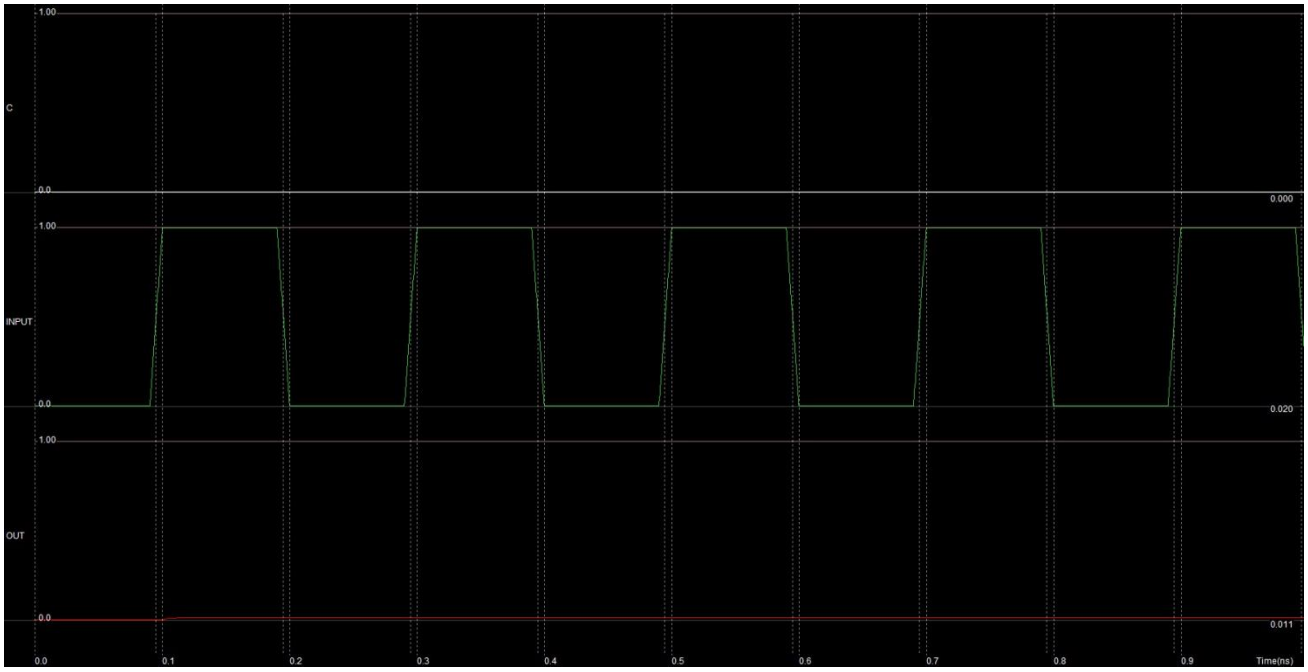
EXERCISE 2:

a)

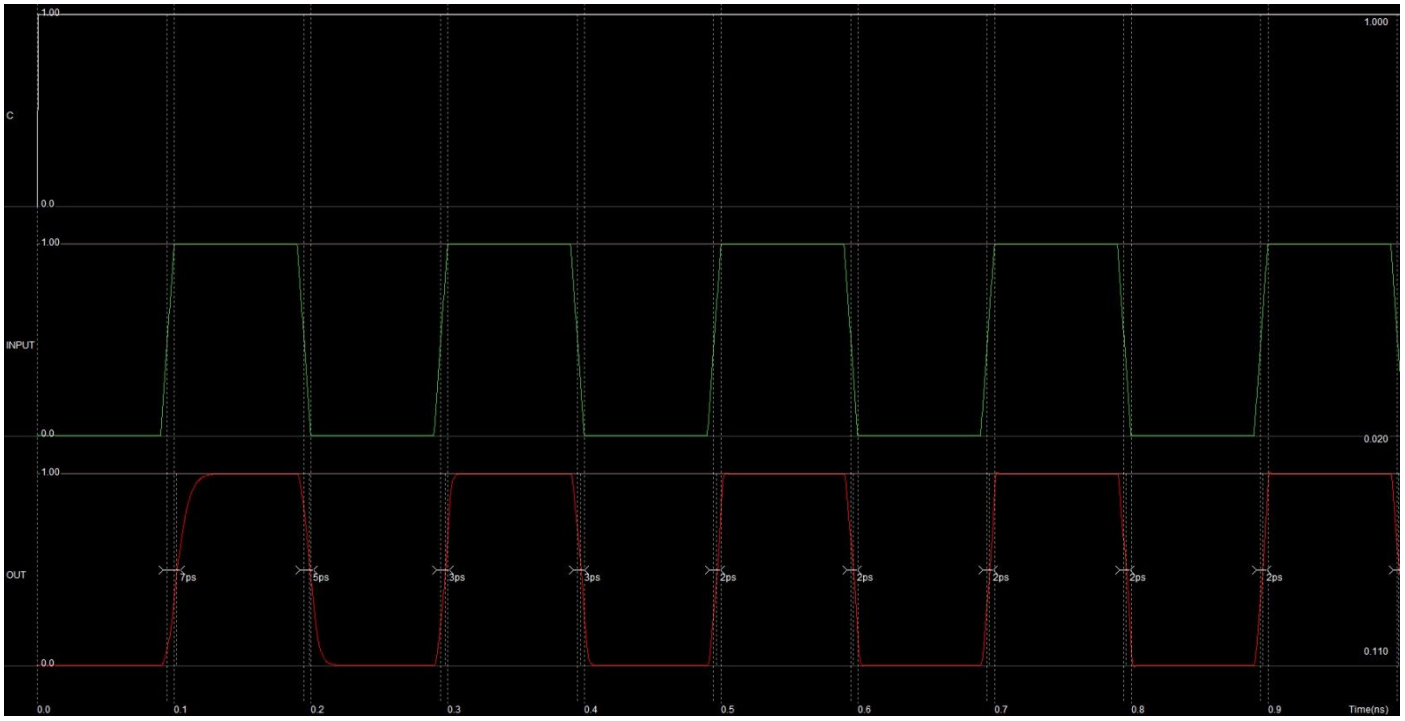


b)

i) For C=0:



ii) For C=1:



c)

As we can see above the transmission gate works correctly as when the inverter is set to 1 the gate transmits 0 and 1 equally well. We have placed a constant pulse train at the input (INPUT) and at C a constant voltage (0 or 1V). When C is not at voltage as we can see in the first diagram the inverter does not turn on any transistor and we do not have the same input and output. When C has a voltage of 1V then the output "copies" the input. The delays we observe are due to the charging and discharging time of the capacitors of the logic circuit.