3rd Laboratory Exercise – Part B

Theoretical & practical calculation of delays in CMOS VLSI inverters

1 The requirements of the laboratory exercise

1. Make the Datasheets as given in (next) *Table* 3.1, using MICROWIND, for three (3) of your own inverters in *cmos018* technology with dimensions: Wn=(0.6ÿ)×k, Ln=0.2 μ and Wp=(1.2μ)×k, Lp=0.2μ for k=1, 3 and 8. In particular calculate the *input capacitance,* the *intrinsic* or *parasitic delay* and the *slope* Kload of the curve representing the delay as a function of the load capacitance . Compare them with the values in *Table* 3.1 and draw conclusions.

Cell Description

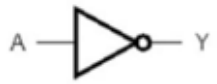
The INV cell provides the logical inversion of a single input (A). The output (Y) is represented by the logic equation:

$Y = \overline{A}$

Functions

A	Y
0	1
1	0

Logic Symbol



Cell Size

Drive Strength	Height (μm)	Width (μm)
INVXL	5.04	1.32
INVX1	5.04	1.32
INVX2	5.04	1.98
INVX3	5.04	2.64
INVX4	5.04	2.64
INVX8	5.04	3.96
INVX12	5.04	8.58
INVX16	5.04	11.22
INVX20	5.04	12.54

AC Power

Pin	Power (μW/MHz)								
	XL	X1	X2	X3	X4	X8	X12	X16	X20
A	0.0087	0.0117	0.0218	0.0329	0.0394	0.0773	0.1706	0.2260	0.2820

Pin Capacitance

Pin	Capacitance (pF)								
	XL	X1	X2	X3	X4	X8	X12	X16	X20
A	0.0027	0.0036	0.0071	0.0104	0.0136	0.0271	0.0068	0.0090	0.0110

Delays at 25°C, 1.8 V, Typical Process

Description	Intrinsic Delay (ns)								
	XL	X1	X2	X3	X4	X8	X12	X16	X20
A → Y↑	0.0261	0.0253	0.0228	0.0243	0.0206	0.0198	0.1303	0.1276	0.1265
A → Y↓	0.0154	0.0146	0.0140	0.0146	0.0125	0.0125	0.1235	0.1232	0.1183

Description	K_{load} (ns/pF)								
	XL	X1	X2	X3	X4	X8	X12	X16	X20
A → Y↑	6.2539	4.5257	2.2629	1.5216	1.1447	0.5513	0.3680	0.2760	0.2209
A → Y↓	3.3414	2.3675	1.2661	0.8247	0.6333	0.3211	0.2194	0.1647	0.1316

Table 3.1: Artisan Components INV cell library datasheet