CMOS-VLSI

CDA 4213L

Lab 1 Report

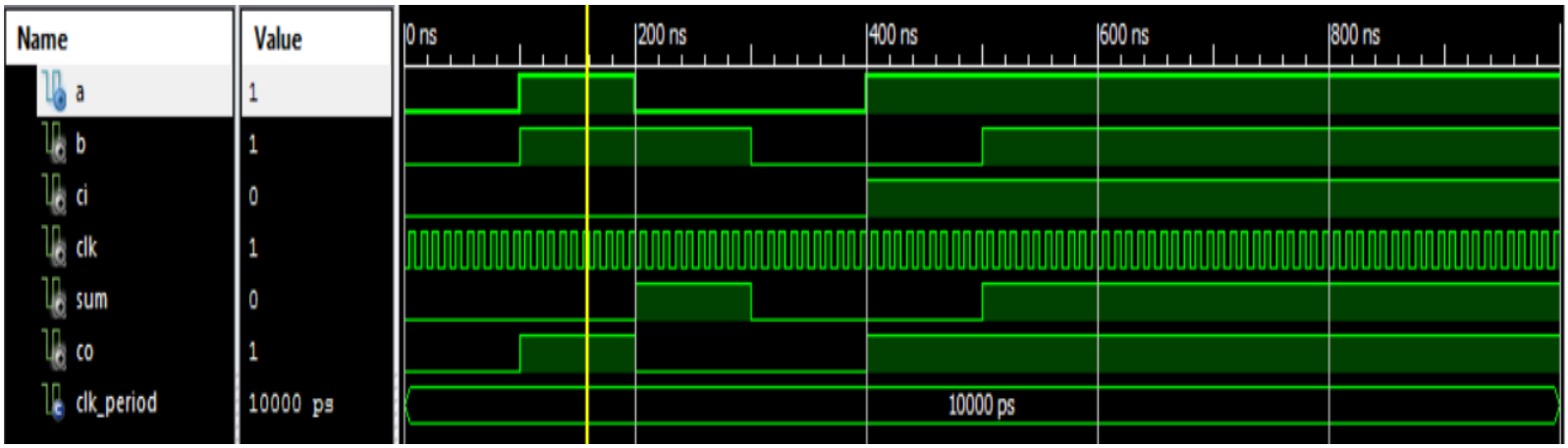
Name: Tashane Daley

Date: 09/06/2016

This lab showed how to make a structural architecture using VHDL. The main file had different components using which had no entities (definitions) of the components used. Each component that was used was created with its own entity. Entities that was created for this lab are xnor_2 and and_4.

Simulation and Results

Below is the simulation for the full adder. It shows that different inputs were given to ‘a’, ‘b’ and ‘ci’ then showing the outputs as sum and co. This is a positive edge trigger which checks the inputs and gives the correct outputs every 100ns. The first inputs are a = 1, b = 1, ci = 0 which gave an output of sum = 0 and co = 1. Comparing the results with the truth table for a full adder showed the exact outputs.



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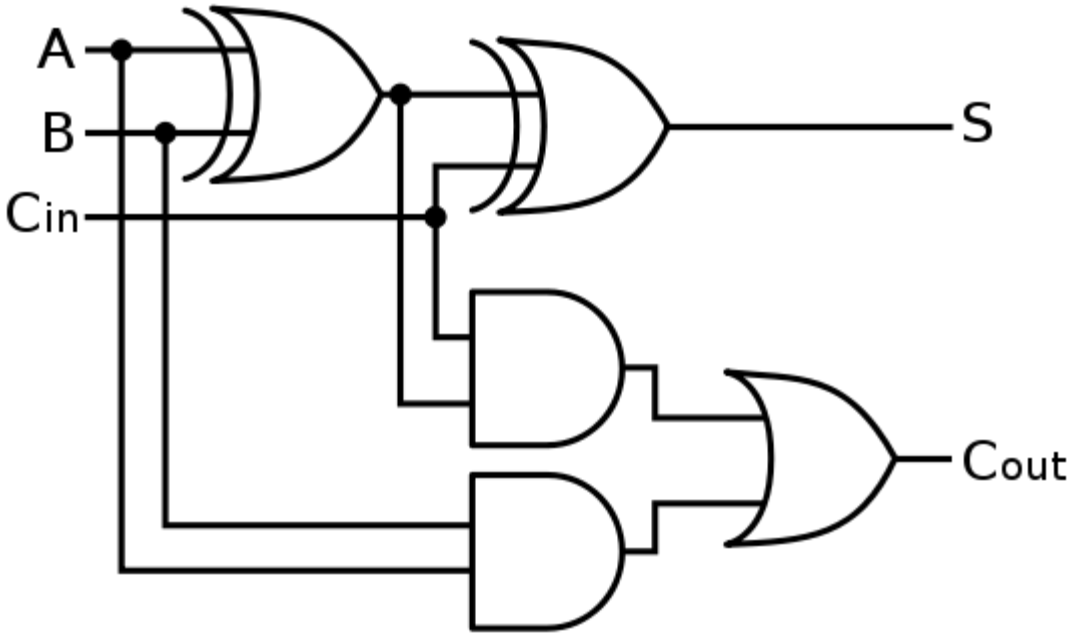

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Below shows the simulation of a 4-bit comparator. If inputs ‘a’ and ‘b’ are the same then the comparator will output ‘equal’ to be 1 else the output will be 0. Inputs were compared every 100ns that will give an output to equal. It shows that when inputs a = 0000 and b = 0000, equals goes high (1). On the next clock cycle the inputs are a = 1111 and b =1000 making the output equal = 0. Other inputs were compared and it gave the correct result.