Lab Report: EEE 466
Group No 15
Lab No 01

LAB TITLE: Study of Single Stage Common Source CMOS Amplifier Design

Prepared by:

Student Name: Himel Kundu Utsha

Student ID:1906014

Name of Group Member and Student ID: Tasmin Khan -1906055

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Course Title: Analog Integrated Circuits and Design Laboratory
Instructor Name: Dr. Muhammad Abdullah Arafat

ABSTRACT

In this experiment, we plotted and observed the current-voltage characteristics of P-channel MOSFET and N_channel MOSFET. We used gpdk090 and analoglib library of Cadence Virtuoso for all the simulations. We also determined the threshold voltage of the MOSFETs. Furthermore, we obtained the plot of transconductance and transconductance per unit current against gate voltage of the N-channel MOSFET. For the report section, we compared the mobility of P and N channel MOSFETs. We also plotted the output resistance againts gate voltage for N channel MOSFET.At the end, we compared the parameters of TT, SS and FF models of N-MOSFET.

KEYWORDS:

1.gpdk090

2.Cadence-Virtuoso

3.Transconductance

4.Threshold-Voltage

5.analoglib

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INTRODUCTION

- Overview of the lab experiment: We got familiar with the Cadence Virtuoso environment and performed some basic simulations with technology libraries like gpdk090 and analoglib.
- What did you expect to learn from the experiment: We learnt how to analyze the I-V characteristics plot of NMOS and PMOS. We got introduced with some simulation corners like FF, TT and SS. We learnt how to obtain threshold voltage and compare other parameters like mobility, output resistence of the MOSFETs.
- What information was analyzed in the lab: I-V characteristics on NMOS and PMOS, threshold voltage and transconductance , output resistance of NMOS, comparison of mobility of NMOS and PMOS
- Explain how this experiment result can relate to real world problems: The results of this experiment can help us to gain more insights of the MOSFETs' various parameters which are vital for an electronic engineer.

THEORY

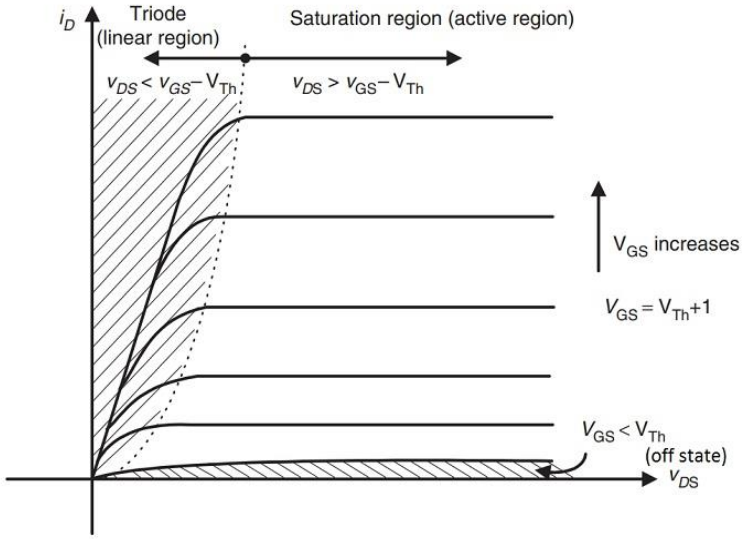

Figure 1: Typical I-V curve of a NMOS, neglecting Early effect

MOS operation can be classified into three region, cut-off, triode, and saturation. NMOS only turned on when $VGS > VTH$. When $VDS < VGS - VTH$, the NMOS transistor is said to be in triode region and the drain current is given by

$$I_D = \frac{\mu_n C_{ox} W}{L}[(V_{GS} - V_{TH})V_{DS} - \frac{1}{2}V_{DS}^2]$$

For $VDS > VGS - VTH$, NMOS is in saturation region of operation, and channel is pinched off. Including Early effect, drain current in this region is given by

$$I_D = \frac{\mu_n C_{ox} W}{2L}(V_{GS} - V_{TH})^2(1 + \lambda V_{Ds})$$

Where transistor output resistance in saturation region is defined by

$$r_o = \frac{\delta V_{DS}}{\delta I_D} = \frac{1}{\lambda I_D}$$

An important parameter transconductance gm is defined as

$$g_m = \frac{\delta I_D}{\delta V_{GS}} | at\ V_{DS}\ constant$$

TOOLSUSED

List all the tools that are used in the lab:
Cadence Virtuoso Software

PROCEDURE

1. Creation of a Design Project and adding Library to the design by adding gpdk090, analogLib, basic the libraries in the Library Path Editor. Then open a new 'Library' from File menu, select 'gpdk090' as the technology library and set a 'Cell' name for Schematics.

2. A blank schematic window will appear, and desired circuit was drawn.

3. By Launching Analog Design Environment (ADE), we started the process of netlist creation and simulation using Spectre. After setting Model Libraries, Design variables, Analysis, and Output plots, we run the simulations.

4. The resultant plots were analyzed for verification.

RESULTS

I-V characteristics of NMOS

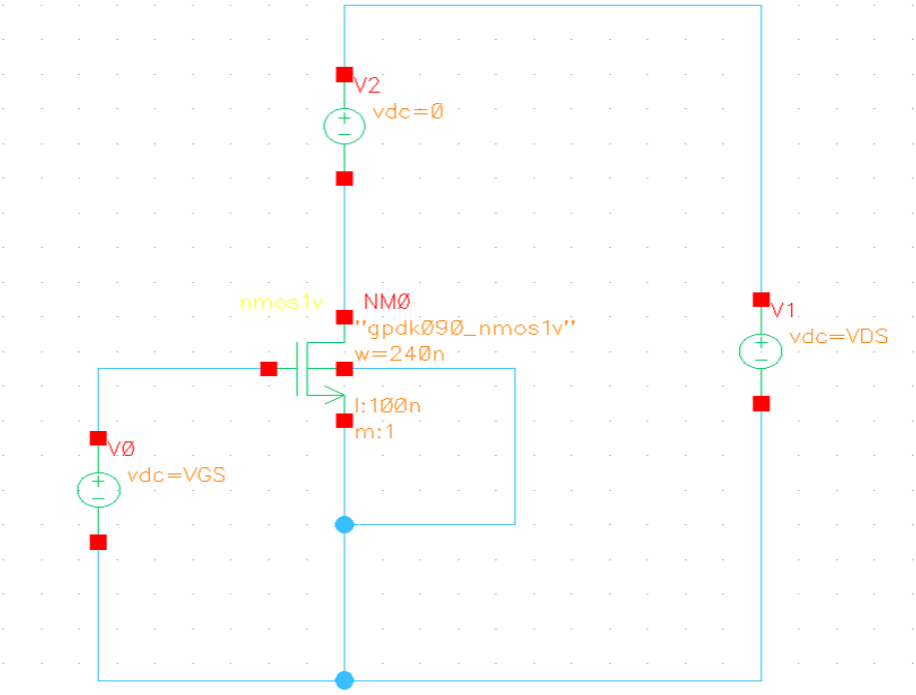

Figure 2: Schematic for I-V characteristic of NMOS

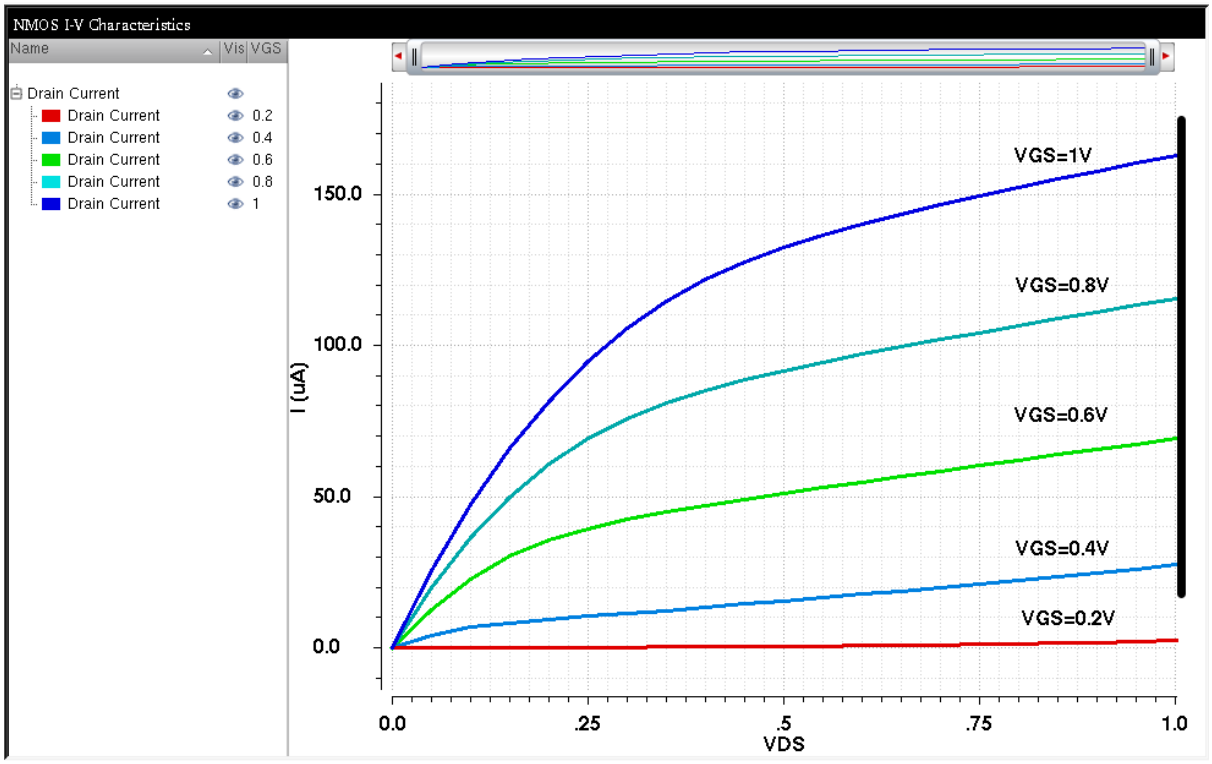

Figure 3: I-V characteristic of NMOS

I-V characteristics of PMOS

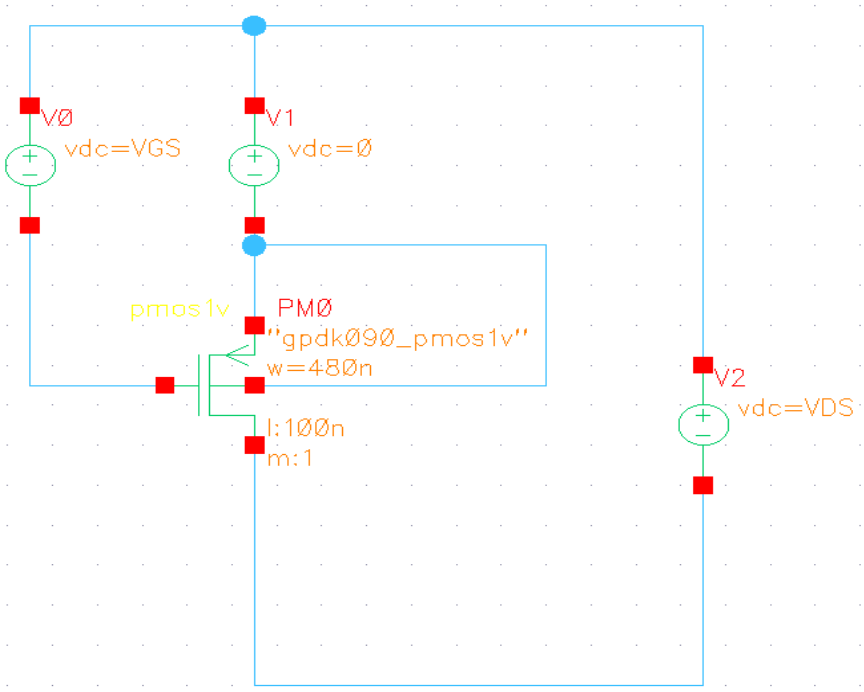

Figure 4: Schematic for I-V characteristic of PMOS

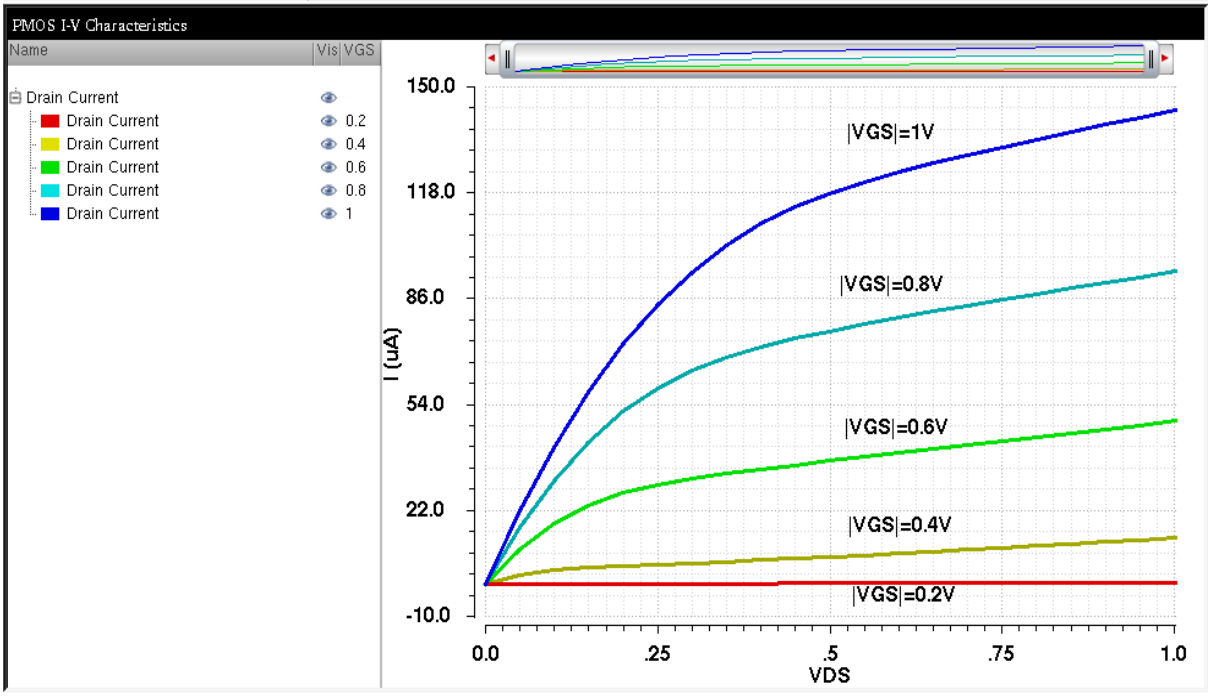

Figure 5: I-V characteristic of PMOS

Measuring the threshold voltage of MOS transistor

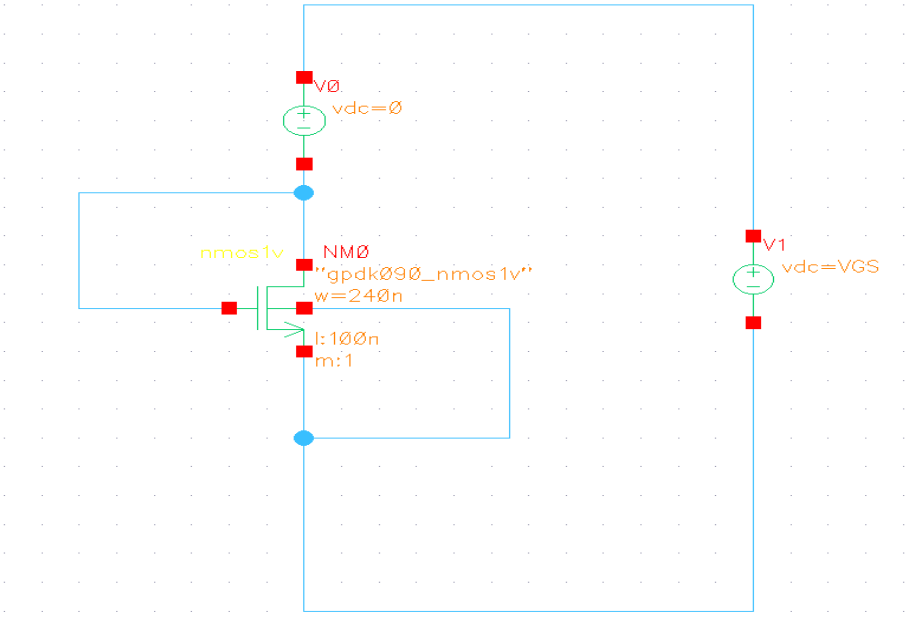

Figure 6: Schematic for Threshold Voltage of NMOS

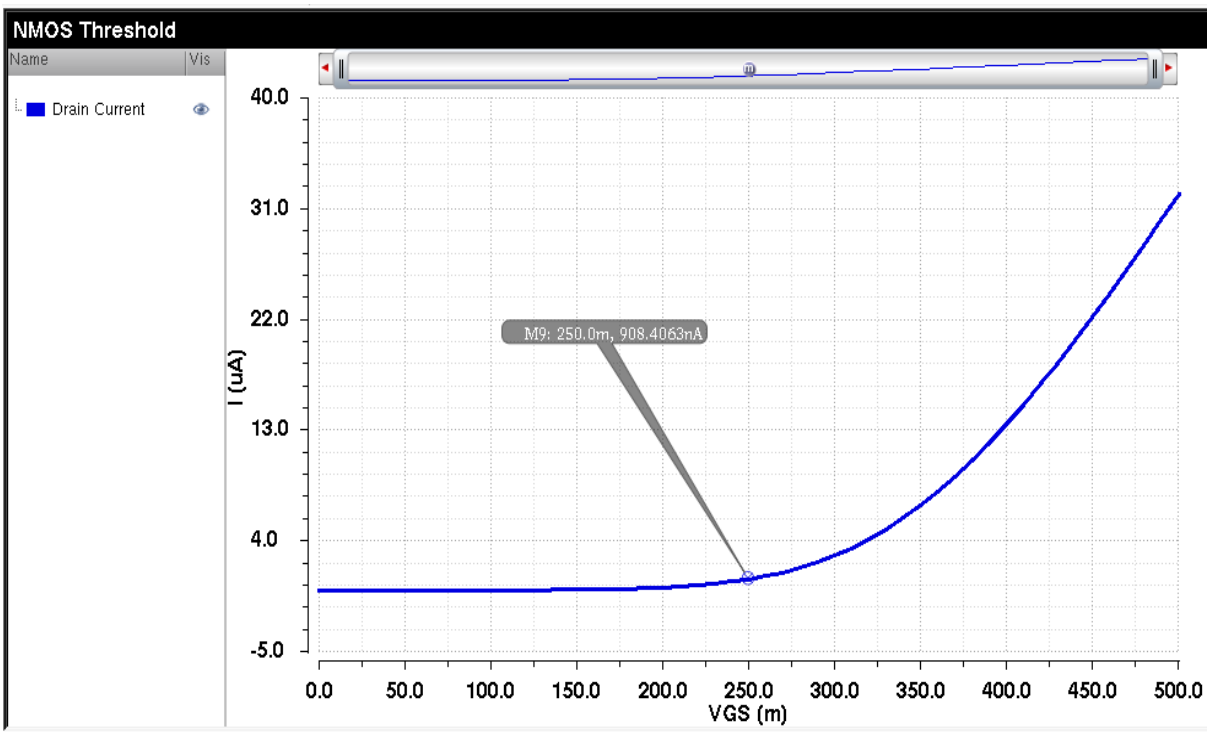

Figure 7: Threshold Voltage of NMOS

Threshold voltage was found to be $VGS = 0.25V$ for drain current $ID = 0.908$ nA.

Measuring the Figure of Merit of MOS transistor

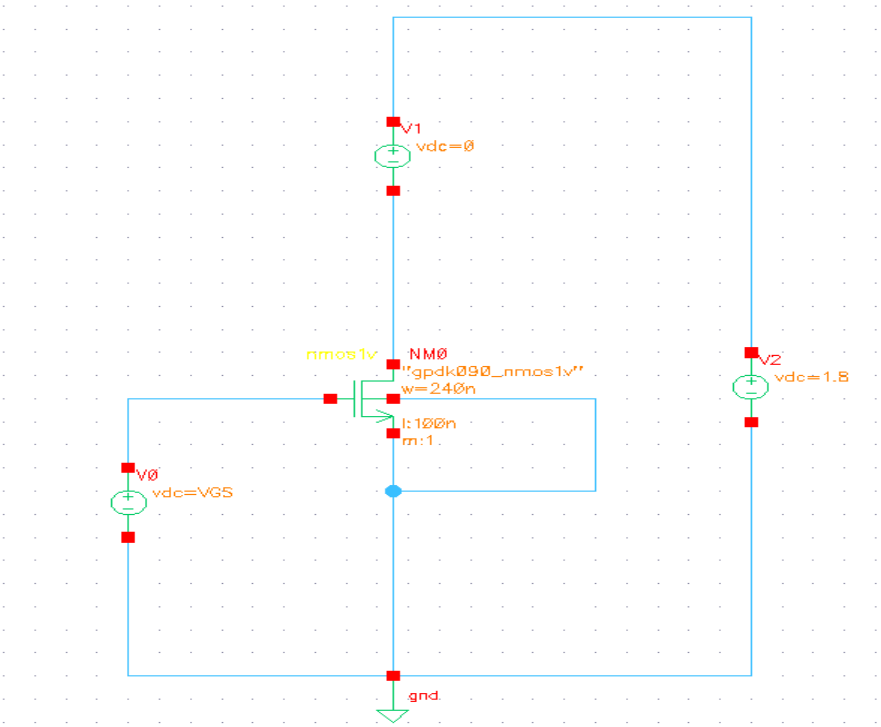

Figure 8: Schematic for transconductance of NMOS

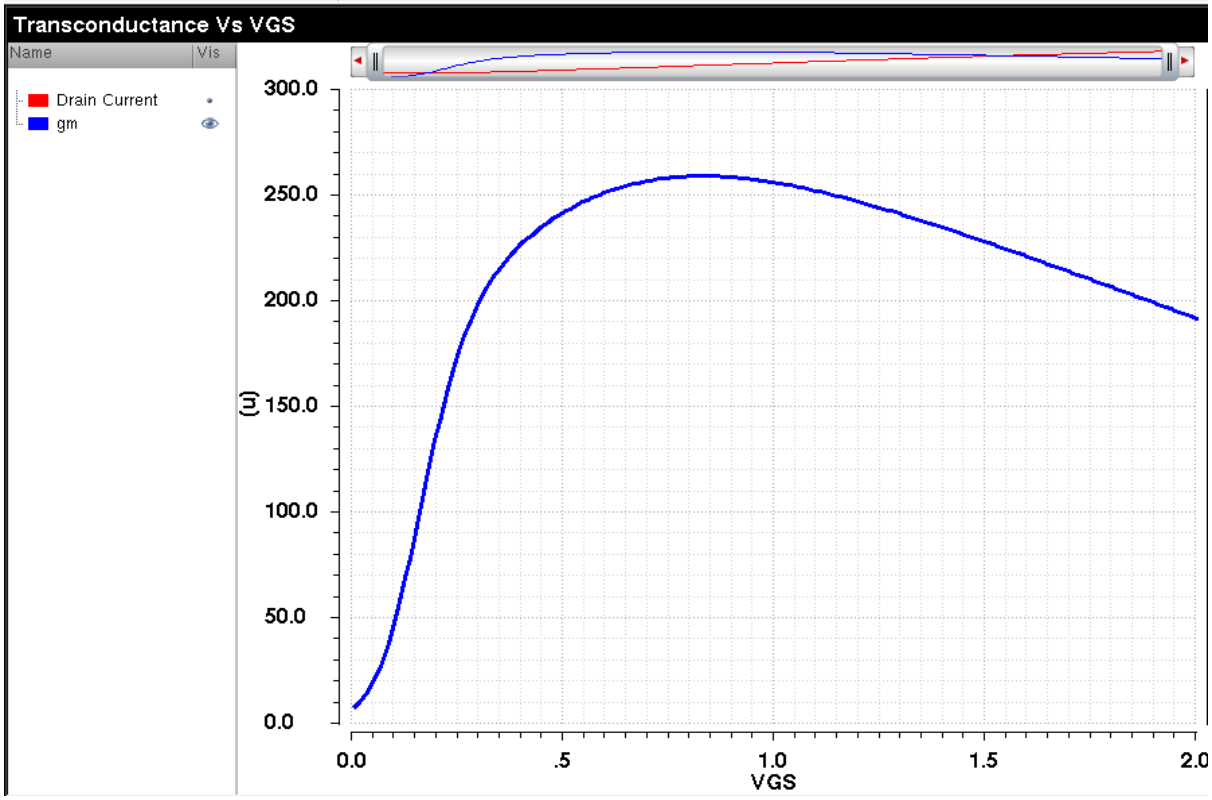

Figure 9: transconductance(gm) Vs VGS of NMOS

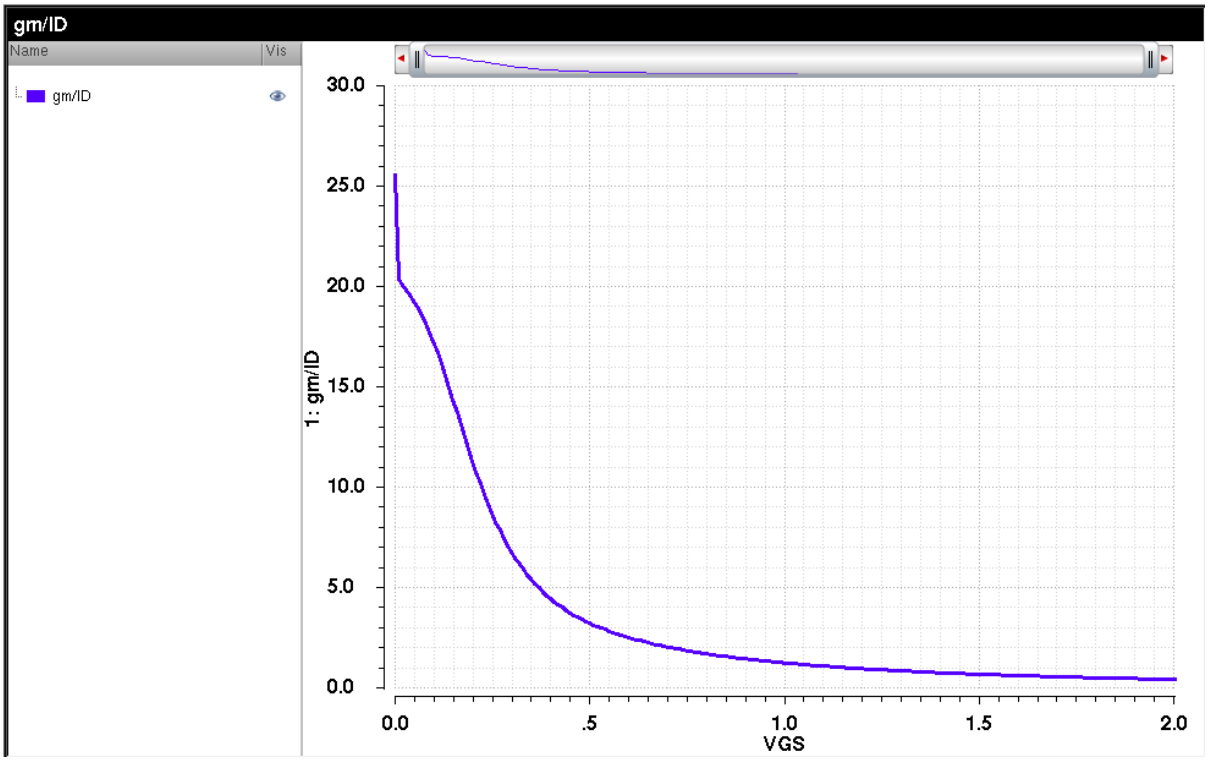

Figure 10: gm/ID Vs VGS of NMOS

Report 1

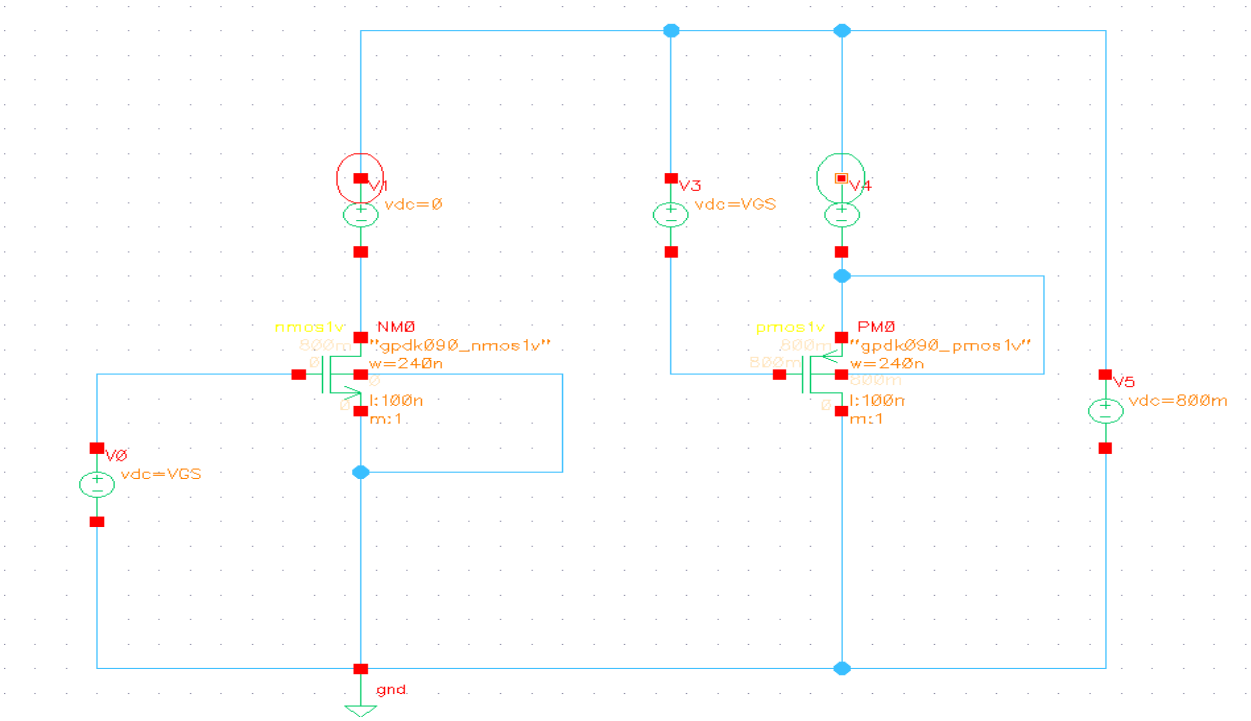

Figure 11: Schematic for mobility comparison

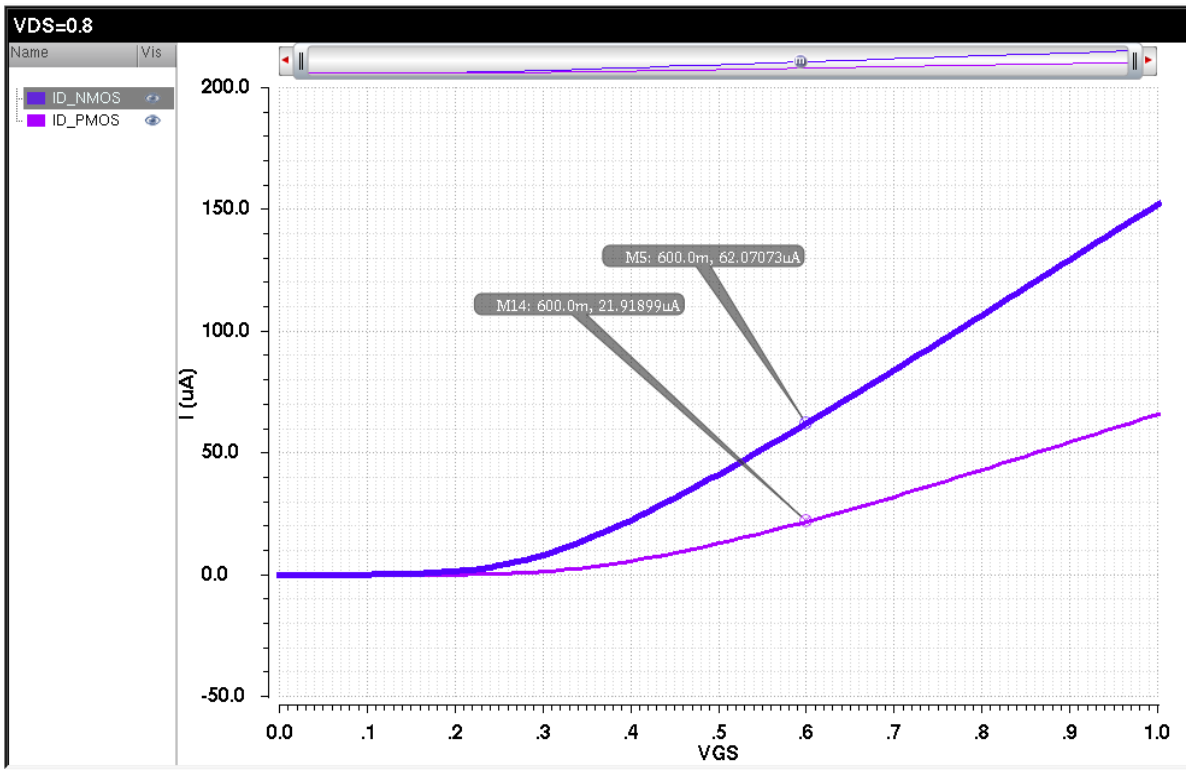

Figure 12: ID vs Vgs for NMOS and PMOS with VDS = 0.8V

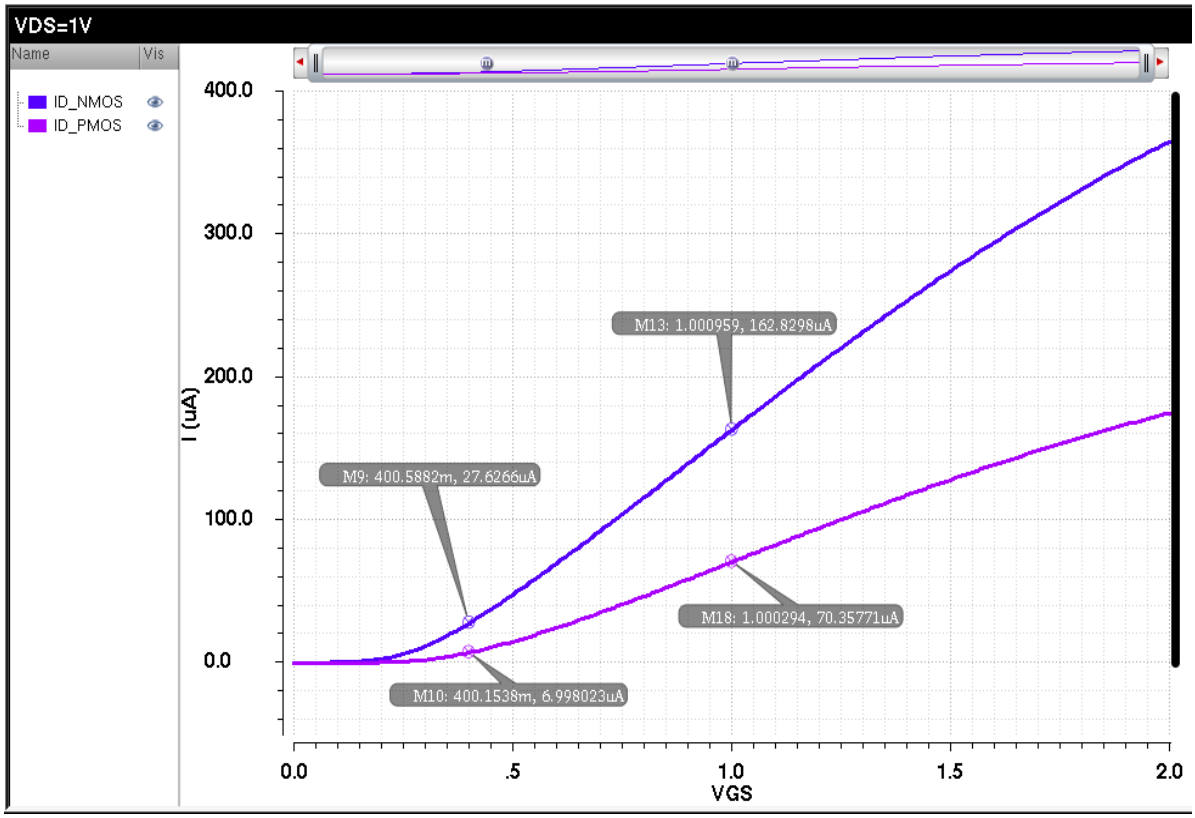

Figure 13: ID vs Vgs for NMOS and PMOS with VDS = 1V

Mobility of a transistor is proportional to its drain current. Thus, mobility ratio for two MOS can be written as $\mu n / \mu p = Idn/Idp$.

$VGS = 0.6V$, $VDS = 0.8V$, mobility ratio = 62.07 / 21.99 =2.8
$VGS = 0.4V$, $VDS = 1V$, mobility ratio = 27.63 / 7 =3.9
$VGS = 1V$, $VDS = 1V$, mobility ratio = 162.83 / 70.36 = 2.3

The mobility of NMOS is higher than PMOS in each case. NMOS has electrons as majority carrier and PMOS has holes as majority carrier. Electrons are faster than holes. Hence, we get higher mobility for NMOS.

Report 2

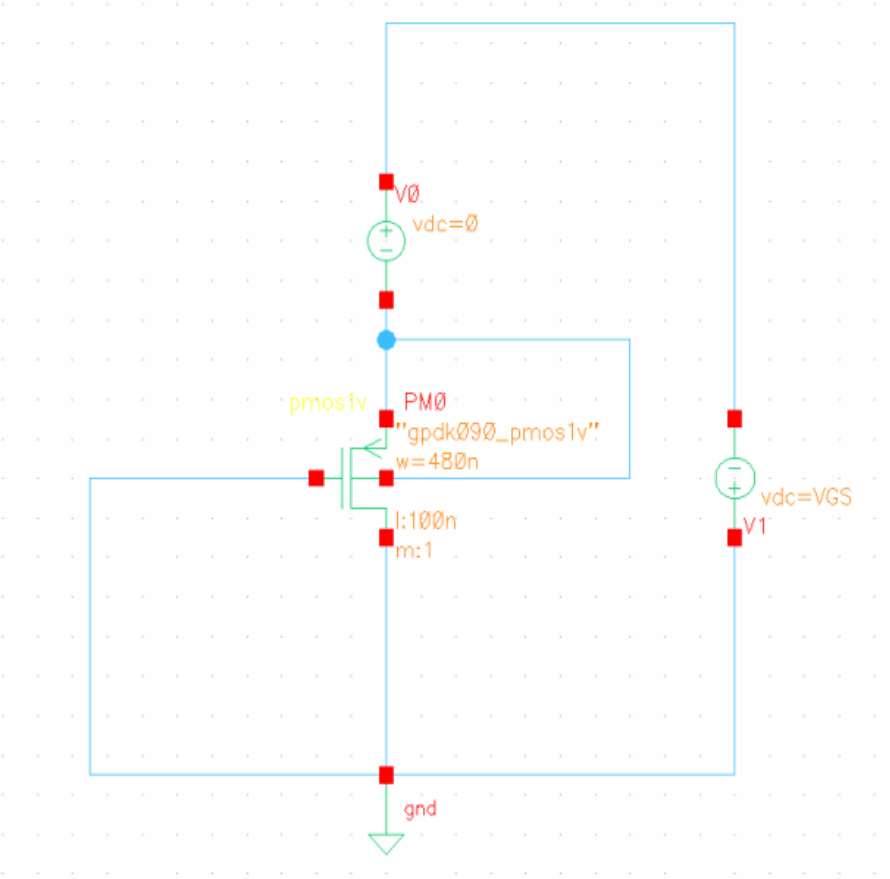

Figure 14: Threshold voltage calculation schematic for PMOS

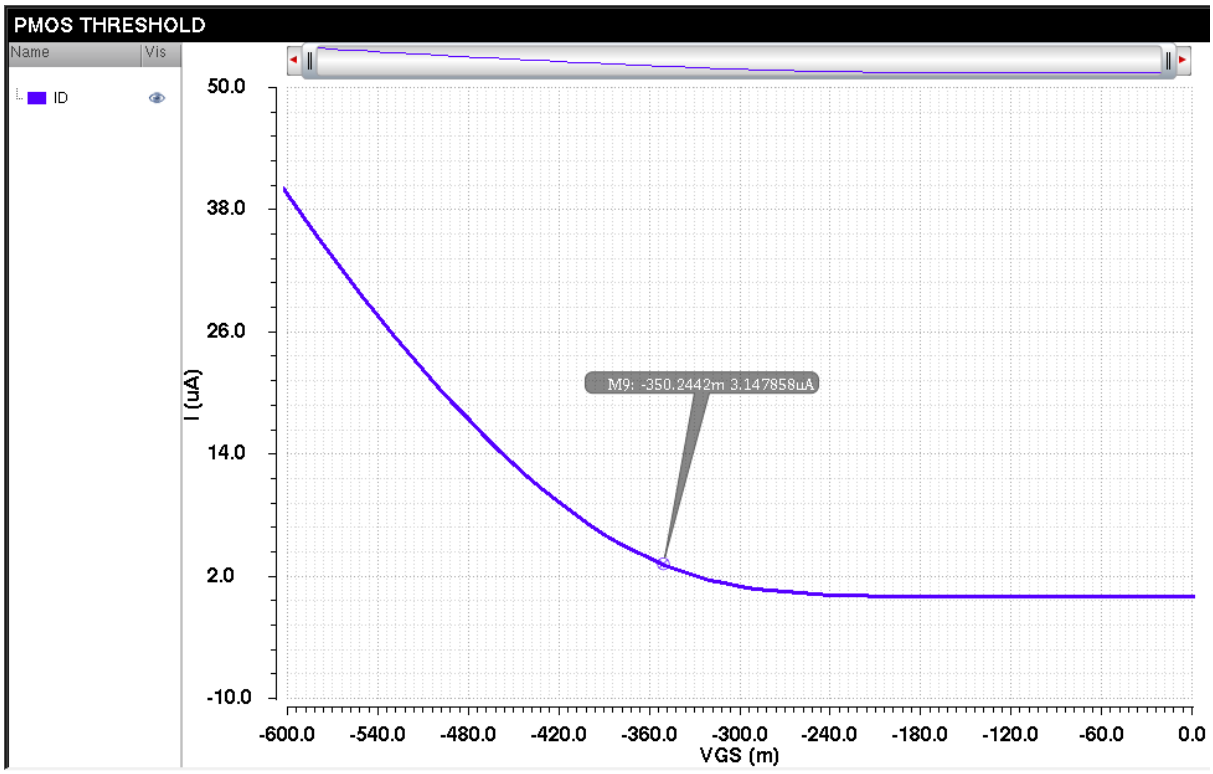

Figure 15: Threshold voltage calculation plot for PMOS

Threshold voltage was found to be $VGS = -350mV$ for drain current $ID = 3.15\mu A$.

For PMOS, the threshold voltage is negative because we have to apply a negative gate voltage to accumulate sufficient amount of holes to form p channel.

Report 3

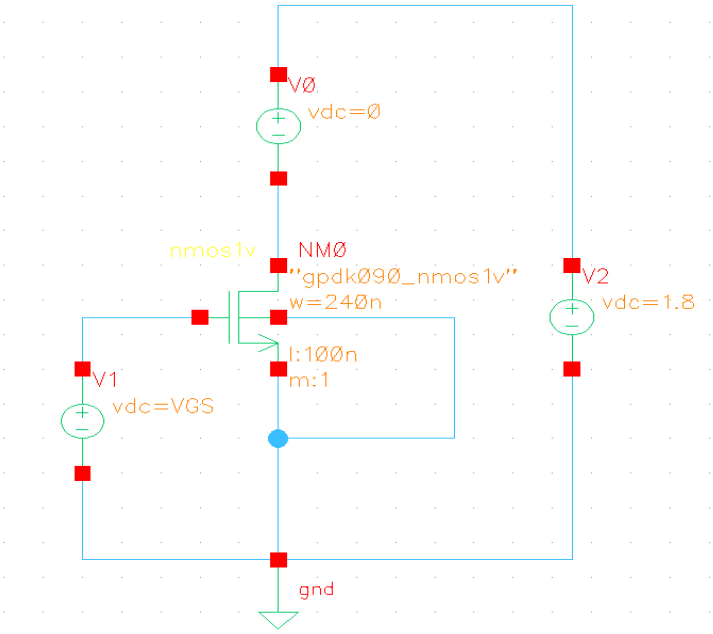

Figure 16: Output Resistance calculation schematic for NMOS

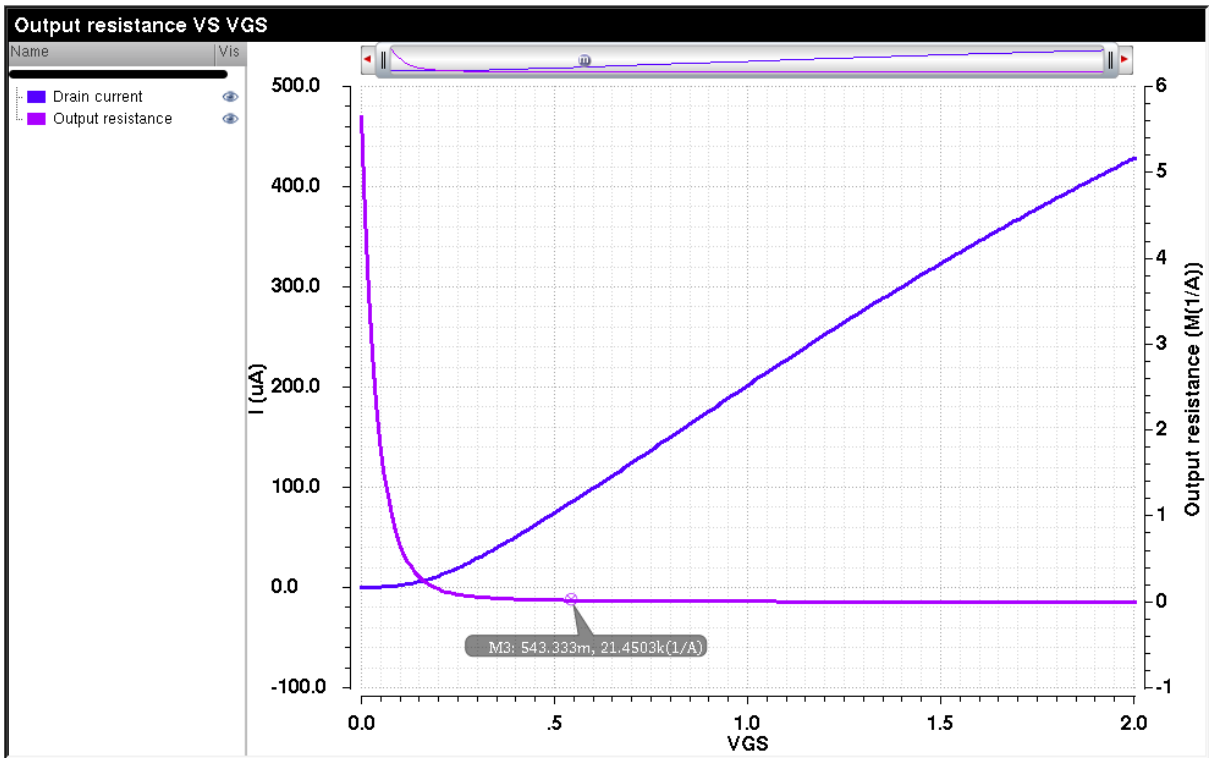

Figure 17: Output Resistance plot for NMOS

• For $Vgs < Vth$ in cut off operating condition, $r0$ was effectively infinity
• For Vgs - $Vth > VDS$ in triode operating condition, $r0$ rapidly deceases.
• For Vgs - $Vth < VDS$ in saturation condition, $r0$ saturates to 21.5 $k\ \Omega$.

Report 4

In gm vs VGS plot, gm remains effectively constant up to 0.1V gate voltage which can be denoted as weak inversion region, and then in moderate inversion region, gm linearly increases up to 0.8V with peak value of 260. Finally, it starts to steadily decline in the strong inversion region.

For the particular schematic, we always had $VGS = VDS$, thus immediately after crossing the threshold voltage VTH, the NMOS enters into saturation, where we have,

$$g_m = \frac{\delta I_D}{\delta V_{GS}} = \frac{\mu_n C_{ox} W}{L}(V_{GS} - V_{TH})$$

With increasing VGS, drain current also rises. But at high very gate voltage, the drain current cannot increase that much. Thus,

$$g_m = \frac{\mu_n C_{ox} W}{L}(V_{GS} - V_{TH}) = \sqrt{(\frac{2\mu C_{ox} W}{L} I_D)} = \frac{2I_D}{V_{GS} - V_{TH}}$$

Report 5

The maximum gm/ID ratio was discovered in the weak inversion region. However, as the operating point approaches strong inversion, the gm/ID ratio falls. Weak inversion operation would be the most efficient in terms of minimum power consumption and high transconductance gain. However, too low drain current in the weak inversion may not provide enough noise margin, so shifting to moderate inversion may be a good compromise in some cases.

Report 7

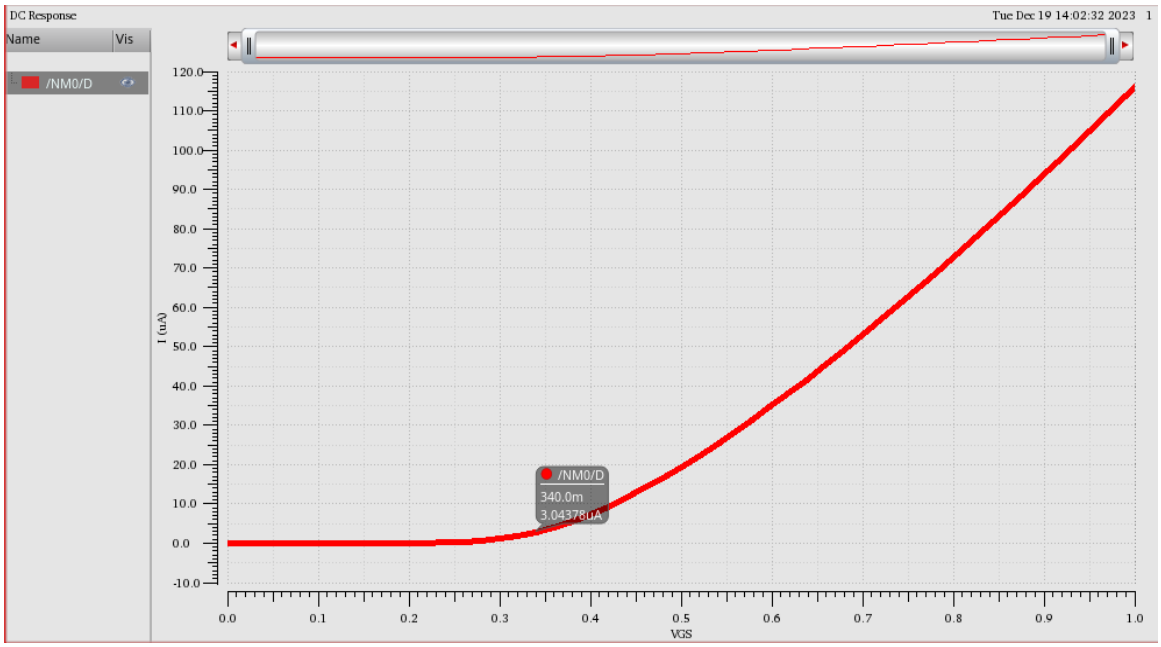

Figure 18: IV curve of NMOS with SS model corner

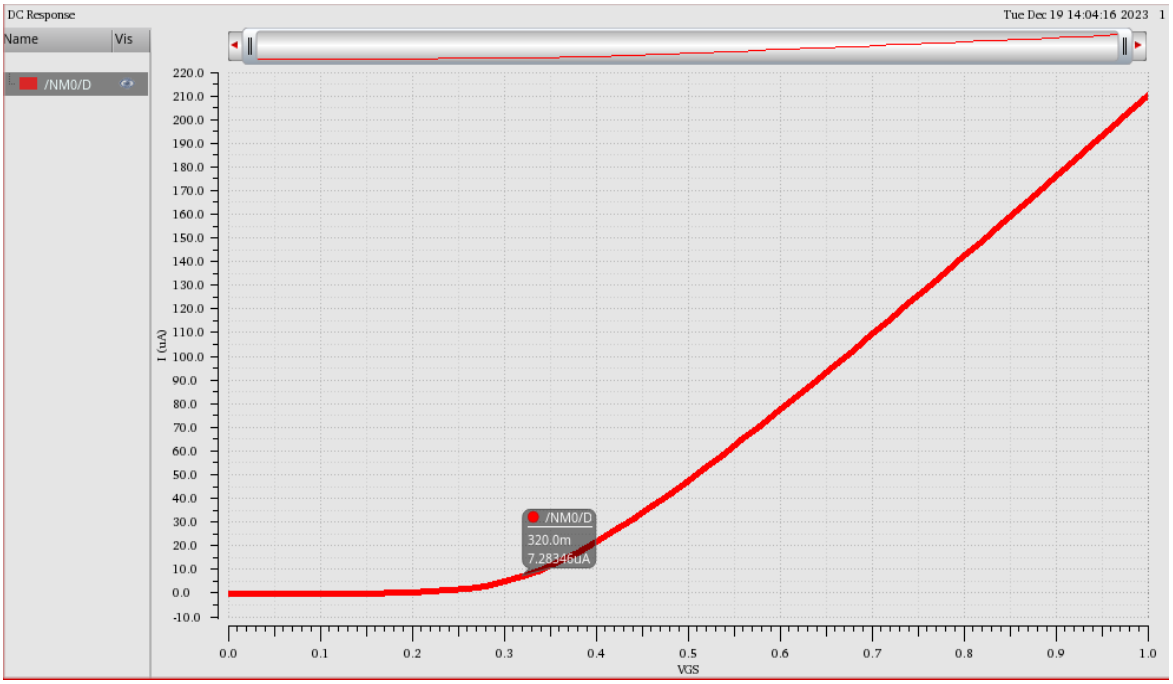

Figure 19: IV curve of NMOS with FF model corner

Threshold for SS model corner : 0.34V
Threshold for FF model corner : 0.32V

CONCLUSION

We plotted and observed the current-voltage characteristics of P-channel MOSFETs and N_channel MOSFETs in this experiment. For all simulations, we used Cadence Virtuoso's gpdk090 and analoglib libraries. We also determined the MOSFETs' threshold voltage. Furthermore, we obtained a plot of the N-channel MOSFET's transconductance and transconductance per unit current against gate voltage. We compared the mobility of P and N channel MOSFETs for the report section. For N channel MOSFETs, we also plotted the output resistance versus gate voltage.Finally, we compared the parameters of N-MOSFET models TT, SS, and FF.

REFERENCES

1. Razavi, B. (2001). Design of analog CMOS integrated circuits. Boston, MA: McGrawHill, Chapter 2, Section 2