BANGLADESH UNIVERSITY OF ENGINEERING AND TECHNOLOGY
DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING

EEE 466 (January 2022) **A1**
Analog Integrated Circuits Laboratory

Final Project Report

Voltage Controlled Oscillator

Evaluation Form:

STEP	DESCRIPTION	MAX	SCORE
1	Report (Format, Reference)	10	
2	Design Method and Complete Design (Hardware Implementation)	20	
3	Video Demonstration	10	
4	Novelty of Design	20	
5	Project Management and Cost Analysis	15	
6	Considerations to Public Health and Safety, Environment and Cultural and Societal Needs	10	
7	Assessment of Societal, Health, Safety, Legal and Cultural issues relevant to the solution	10	
8	Evaluation of the sustainability and impact of designed solution in societal and environmental contexts	10	
9	Individual Contribution	20	
10	Team work	10	
11	Diversity of Team	05	
	TOTAL	150	

Signature of Evaluator: _____

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"In signing this statement, We hereby certify that the work on this project is our own and that we have not copied the work of any other students (past or present), and cited all relevant sources while completing this project. We understand that if we fail to honor this agreement, We will each receive a score of ZERO for this project and be subject to failure of this course."

Full Name: Himel Kundu **Student ID: 1906014**	**Full Name: Shadman Saquib** **Student ID: 1906020**
Full Name: Chinmoy Biswas **Student ID: 1906029**	**Full Name: Tasmin Khan** **Student ID: 1906055**

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1 Abstract

This project presents the design of an LC Voltage Controlled Oscillator (VCO) using Cadence Virtuoso, adhering to specific design parameters. The VCO, crucial in frequency synthesis and communication systems, was meticulously crafted to achieve stable oscillation and tunable frequency ranges. Employing differential pair configurations and biasing techniques, the VCO offers enhanced performance metrics such as low phase noise and linear tuning. Simulation studies validate design specifications, while layout implementation ensures manufacturability and performance optimization. The project underscores advancements in RF circuit design methodologies within Cadence Virtuoso, with implications for wireless communication and radar systems.

2 Introduction

Oscillators are an integral part of many electronic systems. Applications range from clock generation in microprocessors to carrier synthesis in cellular telephones, requiring vastly different oscillator topologies and performance parameters. Robust, high-performance oscillator design in CMOS technology continues to pose interesting challenges.

There are two types of VCOs that one may choose to design:
1) waveform oscillators 2) resonant oscillators.

Waveform oscillators:
1) ring oscillator topology 2) relaxation oscillator (which has poor phase noise performance).

Resonant oscillators:
1) LC tank oscillator topology 2) crystal oscillator (which is neither integrated nor tunable)

Ideally a given VCO topology would be able to meet all of the specifications:

1) low noise
2) low power
3) integrated
4) wide tuning range
5) small die area occupancy
6) high frequency (GHz)

As discussed below, it is unlikely that either the ringVCO (ring oscillator VCO) or LCVCO (LC tank VCO) topologies can meet all of these specifications.

Through a comparison of ringVCOs and LCVCOs, the following advantages and disadvantages may be formulated.

RingVCO advantages:
1) highly integrated in VLSI
2) low power
3) small die area occupancy
4) wide tuning range.

RingVCO disadvantages:

1) As frequency increases phase noise and jitter performance degrades.

LCVCO advantages:

1) outstanding phase noise and jitter performance at high frequency.

LCVCO disadvantages:

1) contains an inductor and a varactor (variable capacitor) which are large area components, and thus is not as suitable for VLSI
2) high power consumption
3) occupies a large die area
4) small tuning range.

Clearly, the ringVCO is most suitable for low power, highly integrated applications that require a large tuning range and a low die space area. In contrast, the LCVCO out performs the ringVCO in low noise applications.
For mobile wireless applications one desires low power, hence the ringVCO may be of choice. However, wireless applications require outstanding noise (phase noise and jitter) performance at high frequency, hence the LCVCO may be of choice.
Having said that, there may be specific applications where either the ringVCO or the LCVCO topology may be optimized to perform sufficiently well.
The aforementioned advantages and disadvantages should hold true for the fabrication technologies (0.13μm CMOS, etc) that are predicted, by IRTS road map, to be in use in the future. Hence, a design decision - to utilize either a ringVCO or a LCVCO - that is based on the above advantages and disadvantages should be a valid decision in the future when silicon CMOS fabrication technologies scale further into the deep deep sub-micron regime.
This analysis illustrates that to be able to target the most diverse range of applications, one should be knowledgeable in the design and optimization of both the ringVCO and LCVCO topologies.

We chose the LCVCO for this project.

Voltage Controlled Oscillator Analysis and Design:

An LC tank VCO can be thought of as two 1-port networks connected together.

Figure 2.1: LC Tank.

One 1-port represents the frequency selective ”tank” where the oscillations occur and the other 1-port represents the active circuit that cancels the losses in the tank. Oscillations can occur when:

i) the negative conductance of the active network cancels out the positive conductance (loss) of the tank
ii) the closed loop gain has zero phase shift.

Conditions i) & ii) above amount to a closed loop gain greater than or equal to unity magnitude with no imaginary component. The first step in designing an oscillator is to choose a circuit topology or type. For this example a balanced NMOS VCO will be chosen.

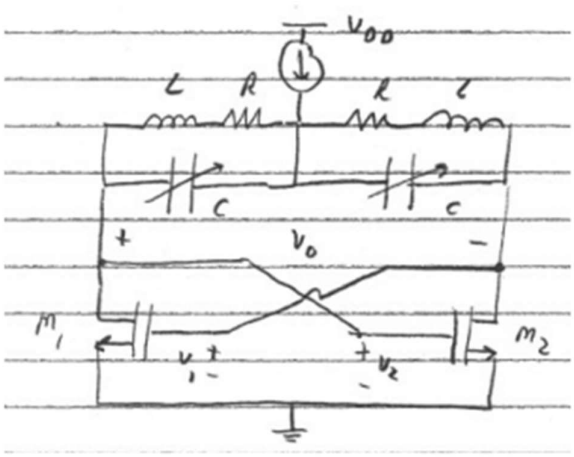


Figure 2.2: Balanced NMOS VCO.

The only losses being assumed in Figure 2.2 are those associated with the inductor. In reality there would also be losses associated with the variable capacitors (varactors) and the MOSFETs (the active devices). In practical integrated VCOs the inductors are on-chip spiral inductors with low quality factor that dominates the losses of the VCO tank.

The quality factor Q_L of the inductor is given by

$$Q_L = \frac{\omega_o L}{R}$$

where

ω_o is the oscillation frequency [rad/s]

L is the value of the inductance [H]

R is inductor's equivalent series resistance [Ω].

where ωo is the oscillation frequency [rad/s] L is the value of the inductance [H] R is inductor's equivalent series resistance [Ω]. QL in practical silicon RF IC processes ranges from 5 to 10. Values of on-chip inductances range from 0.1 nH to 10 mH in practical RF IC processes. It can be shown that the oscillation frequency of the circuit shown in Figure 2.1, assuming ideal varactors and MOSFETs is given by

$$\omega_o = \frac{1}{\sqrt[2]{LC}} \sqrt[2]{1 - \frac{R^2 C}{L}}$$

It can also be shown, under the same set of assumptions that the gm of each MOSFET must be

$$g_m \geq \frac{RC}{L}$$

for oscillation to occur.

Small Signal (a.c.) Analysis:

The oscillator is essentially a differential pair that have been cross-coupled in a positive feed back configuration.

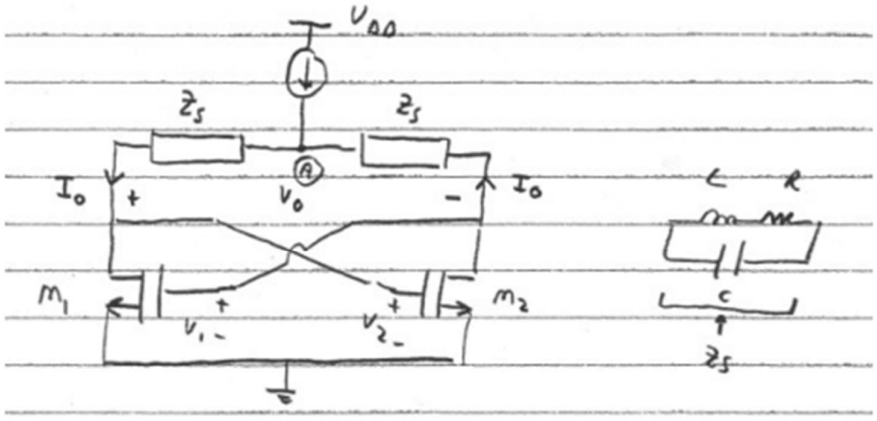


Figure 2.3: Balanced NMOS VCO with each tank represented by a series impedance.

The input of each transistor in the differential pair has been connected to the output of the opposite transistor. The output voltage vo = v1 − v2 is a differential output signal. v1 which is the input signal to M1 is also the single ended output of M2. Each individual transistor in the pair is essentially a common-source amplifier with a complex, tuned load comprised of a lossy inductor in parallel with a capacitor. The Zs load is called a ”tank” circuit since it holds the oscillating energy like a tank at the oscillation frequency. The two separate tanks form a differential load to the differential pair where node ’A’ remains, to first order, at the same potential during oscillations. Node ’A’ is a ”virtual” a.c. ground point in the same manner as the virtual ground that exists in a normal differential amplifier. Node ’A’ is not a complete a.c. short, however, since, ideally, there should be an infinite a.c. impedance between this node and the power supply rail VDD. A proper active current source must be designed to provide the d.c. biasing to node ’A’ and hence M1 and M2 as well as maintaining a high a.c. impedance between node ’A’ and the supply rail. If the a.c. impedance between node ’A’ and VDD is not high, then RF energy will ”leak” out of the tanks into the supply rail destroying the oscillations.

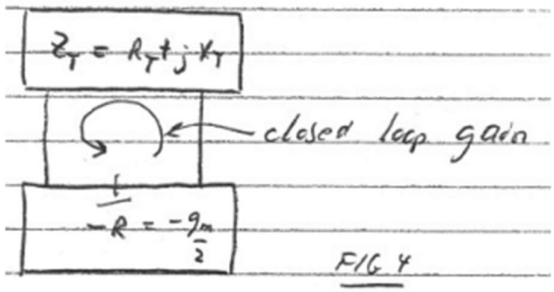


Figure 2.4: VCO of Figure 2.3.

For small signal (a.c.) analysis the current source of Figure 2.3 behaves as an open circuit. The VCO of Figure 2.3 can then be represented by Figure 2.4 as two 1-port networks. Assuming ideal MOSFETs (i.e. no parasitic resistances or capacitances), the entire differential amplifier can be modeled as a negative resistance −R (or negative conductance −Gm = − gm/2). The two tank circuits appear in series where

$$Z_T = 2Z_s = R_T + jX_T = 2(R_s + jX_s)$$

The oscillation condition requires that the closed loop gain (around the two 1-ports) be of at least unity magnitude and zero phase angle. The zero closed loop phase condition implies that at the frequency of oscillation, ωo, XT (ωo) = 0.

The magnitude of the amplifier negative resistance must be at least as large as RT (ωo), the total resistive or real loss of the two tanks. ∴ setting XT (ωo) = 0 determines ωo and setting |− 1/R | = |− gm/2 | = 1/RT (ωo) determines the minimum gm of each MOSFET for oscillation to occur. In general, the negative resistance of the differential pair must overcome all real resistive losses in the oscillator circuit. An ideal oscillator has no losses with infinite voltage swing at precisely one frequency. The presence of losses results in a finite voltage swing over a narrow spread of frequencies. How ideal an oscillator is can be directly related to the ”quality factor” of the tank.

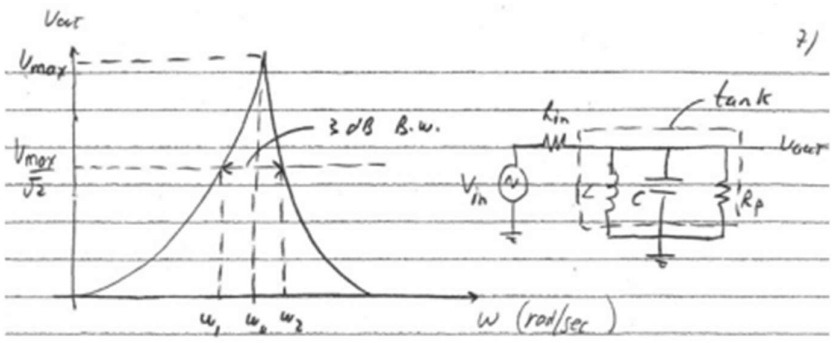


Figure 2.5: Bandwidth of an LC tank oscillator.

At resonance, a pure LC tank with no losses presents infinite impedance to an applied signal across the tank. This implies that the output voltage across the tank will be infinite if the tank is driven by a source with infinite impedance. If the tank has real losses, however, even if it is driven by an infinite impedance source (i.e. Rin = 0), the losses can be modeled as if the lossless tank had a finite impedance load, Rp not equal to ∞. The finite impedance load Rp will ”de-Q” the tank resulting in a finite output voltage.

One definition of quality factor or ”Q” is

$$Q = \frac{\omega_o}{\omega_1 \omega_2}$$

as per Figure 2.5.

It can be shown that Equation 2.5 is also equal to

$$Q_{loaded} = \frac{R_p}{\omega_o L}$$

where ω_o is the resonant frequency of the lossless tank

$$w_o = \frac{1}{\sqrt[2]{LC}}$$

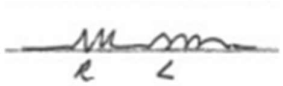
Equation 2.6 is known as a ”loaded Q”.

The ”loaded Q” can be related to something called a ”component Q” where the parallel resistance, Rp, modeling the total losses of the tank can be related to the individual losses of the inductor and capacitor components themselves.

The component Q of the inductor is given by

$$Q_L = \frac{\omega_o L}{R}$$

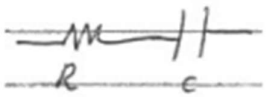
where R is the series resistance of the inductor.



The component Q of the capacitor is given by

$$Q_C = \frac{1}{R\omega_o C}$$

where R is the series resistance of the capacitor.



The total loaded Q can then be estimated as

$$\frac{1}{Q_{loaded}} = \frac{1}{Q_L} + \frac{1}{Q_C}.$$

Often capacitors have much higher component Q’s than inductors in silicon integrated processes (though this may not be the case if varactors are used as the capacitor) such that QL << QC. Then QL ≈ Qloaded

One can then write $Q_{loaded} = \frac{R_p}{\omega_o L} = Q_L = \frac{\omega_o L}{R} = Q$ as the quality factor of the lossy tank.

$$\Longrightarrow R_p = \frac{(\omega_o L)^2}{R} = (\frac{\omega_o L}{R})^2 R = Q^2 R$$

where R is the series resistance of the inductor, Rp is the equivalent parallel resis tance of the lossy tank, and Q is the quality factor of the lossy tank ≡ the component Q of the inductor ≡ the loaded Q of the lossy tank (under the assumption made thus far). From Equation 2.12, the total finite a.c. impedance shunting an otherwise perfect LC tank can be related to the series resistance of the inductor and the component Q of the inductor. It is desirable to have as large of an Rp as possible for a good oscillator. In practice, an RF IC designer sets the value of L required for an oscillator, and then attempts to layout the inductor for maximum component Q so that Rp is as high as possible. Generally over a reasonable range of on-chip inductors the maximum Q possible is more or less independent of the value of inductance provided the particular inductor layout is optimized for maximum Q given the technology being used. Also, the maximum Q is more or less independent of frequency over a fairly large frequency range since inductor layout can also be optimized for different frequencies of operation. For the above reasons, one usually attempts to determine the maximum reasonable Q one can expect over a range of inductance values and frequency ranges for a

given technology. Then this value is used as a constant in the initial design process. Typical values of Q that can be obtained in today's deep sub-micron processes (silicon CMOS) for on-chip inductors range from 5 to 10 for inductor values ranging from 0.1 to 10 nH and frequencies ranging from 1 to several GHz.

Design Constraints:

VCOs are generally designed for minimum phase noise under constraints of d.c. power dissipation, tuning range, output voltage swing and die area. Usually on-chip spiral inductors are utilized for this type of VCO. These inductors usually dominate the chip area required ranging in diameter from 100 to 500 μm. The d.c. power dissipation is given by

$$V_{supply} I_{bias} \leq P_{dissipation\_max}$$

The magnitude of the output voltage at the drains of the NMOS transistors is governed, to first order, by the a.c. impedance of the lossy tank: Vtank ≈ IbiasRp where Rp = QLωoL and Vtank is the single-ended peak-to-peak voltage swing at either the + or - output node of the VCO before any output buffering. The tuning range of a VCO is required to be in excess of a certain minimum percentage of the center frequency, ωo. The LC tank is made tunable by implementing the 'C' of the LC tank using a varactor (variable capacitor). The varactor is designed to be adjustable over some range Ctank min to Ctank max.

Assuming that $\omega_o \approx \frac{1}{\sqrt{LC}}$ (i.e. that of an ideal tank) then,

$$L_{tank} C_{tank\_min} = \frac{1}{(\omega_{max})^2}; L_{tank} C_{tank\_max} = \frac{1}{(\omega_{min})^2}$$

where $(\omega_{max} - \omega_{min})/\omega_o$ = fractional tuning range and $(\omega_{max} + \omega_{min})/2 = \omega_o$

Transistor Non-Idealities:

MOSFETs have many parasitic capacitances and resistances that determine transistor performance.

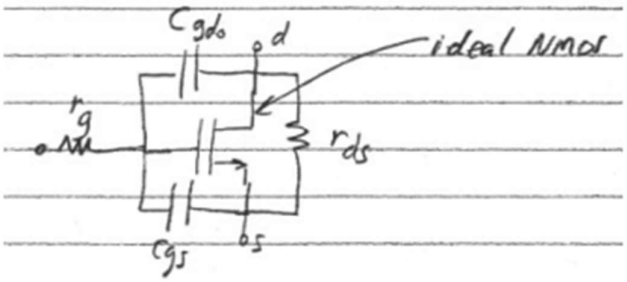


Figure 2.6: MOSFET parasitic elements.

Parasitic resistances increase the losses in the VCO requiring a higher gm compared to the ideal transistor case. Parasitic capacitances can combine with the tank capacitance, C, reducing the oscillation frequency. Therefore the tank's C must be decreased to allow for these parasitic transistor capacitances. Parasitic resistances will also contribute thermal noise increasing oscillator phase noise. rds is not a real resistance contributing noise, but results from channel path length modulation decreasing the a.c. output resistance of the MOSFET and partially de-Q's the LC tank. As shown in Figure 2.7 a) and b), ignoring the effects of gate resistance rg, it can be shown that rds appears in parallel with Rp if node 'A' can be assumed to experience no a.c. voltage fluctuations during oscillation (i.e. node 'A' is a virtual ground). All parasitics can be associated with the tank as shown

in Figure 2.7 leaving ideal NMOS transistors in the active 1-port circuit. The oscillation frequency ωo will them be altered such that

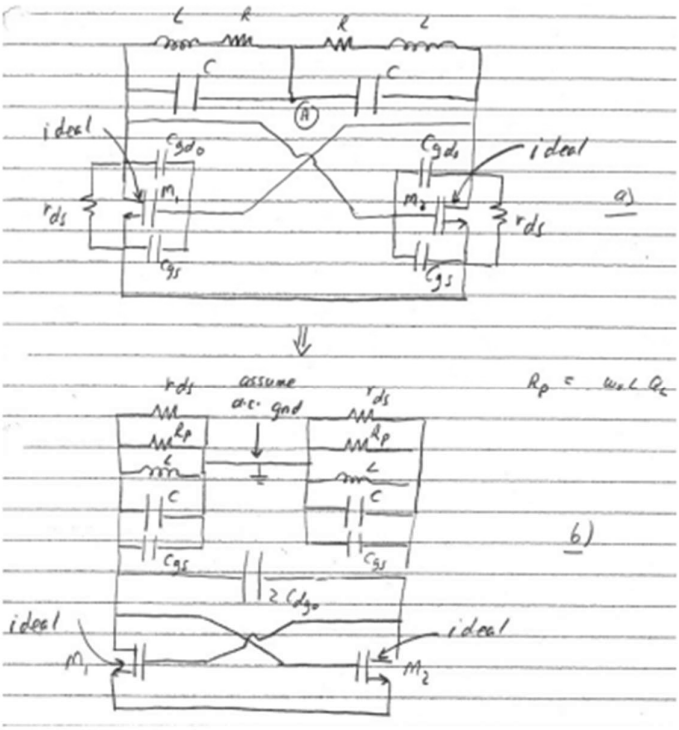


Figure 2.7: LC tank parasitic elements.

$$\omega_o = \frac{1}{\sqrt[2]{L(C + C_{gs} + 4C_{gd_o})}} \sqrt[2]{1 - \frac{R^2(C + C_{gs} + 4C_{gd_o})}{L}}$$

In the above equation it can be seen that the transistor capacitances more or less simply add to the tank capacitance, C, requiring a decrease in C compared to the ideal case for a given ωo. The start-up gm condition also changes such that the absolute minimum gm required for oscillation becomes:

$$g_m \geq \frac{1}{r_{ds}} + \frac{R(C + C_{gs} + 4C_{gd_o})}{L}$$

Equation 2.16 states the important result that the bigger the MOSFETs the higher the gm must be to achieve oscillation

Determining Transistor Width 'W':
The NMOS transistors must be biased and laid out such that the required gm is obtained to overcome all losses including those of the tank and the transistors themselves. The above amounts to determining the Vgs (the bias) and W for a given minimum transistor channel length Lchannel, which is fixed for a given process technology. For modern CMOS processes Vgs is selected such that Vgs − Vt ≈ 0.4 to 0.5, where Vt is the MOSFET threshold voltage. If Vgs − Vt is too high, gm is degraded due to effects such as mobility degradation and saturate velocity effects for channel carriers. If Vgs −Vt is too small then W must be very large such that the transistor will not fit into the require area, or such that gm is always too large according to Equation 2.16 too obtain. To estimate the required gm one must iterate on device equations for Id, gm, rds, Cgs, Cgdo and the equation for start-up criterion of Equation 2.16. Assume the MOSFETs are in saturation. A basic Level 1 MOS model gives:

$$I_{dsat} = \frac{k_p}{2}\frac{W}{L_{channel}}(V_{gs} - V_t)^2 = \frac{g_m}{2}(V_{gs} - V_t)$$

$$g_m = \frac{dI_{dsat}}{dV_{gs}} = k_p\frac{W}{L_{channel}}(V_{gs} - V_t)$$

$$r_{ds} = \frac{1}{\lambda I_{dsat}}$$

$$C_{gs} = \frac{2}{3}C_{ox}WL_{channel}; C_{gd_o} = C_{GD_o}W$$

Certain model parameters must be determined from the design kit for the CMOS process including:

$L_{channel}$ = min channel length

V_t = threshold voltage

k_p

λ - models channel length modulation

$C_{ox} = t_{ox}/\epsilon_{ox}$, t_{ox} = gate oxide thickness

G_{GD_o} = gate-to-drain capacitance per unit gate width W.

Some of the model parameters must be determined for a combination of other parameters. Begin the iteration process assuming ideal MOSFETs and including only the tank losses due to R

$$\therefore g_m = \frac{RC}{L}$$

(once C and L are known - see design procedure steps)

from Equation 2.18 we have

$$W = \frac{g_m L_{channel}}{k_p(V_{gs} - V_t)}$$

then calculate I_{dsat}, r_{ds}, C_{gs}, C_{gd_o} from Equations 2.17 to 2.20.

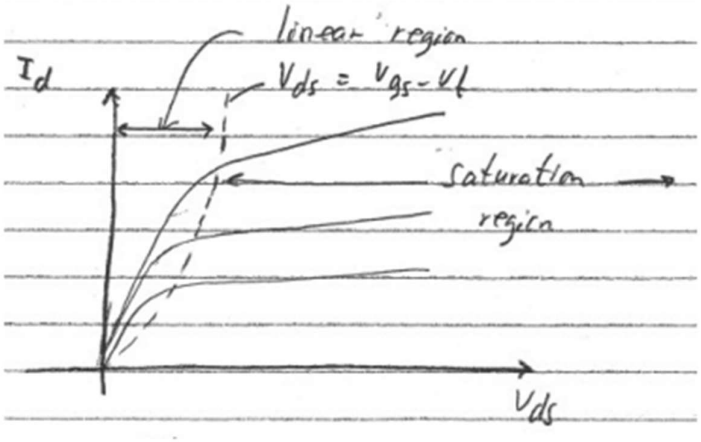


Figure 2.8: MOSFET I-V characteristics.

Idsat is the drain current under saturation conditions. A higher gm will be required for non-ideal case

using

$$g_m = \frac{1}{r_{ds}} + \frac{R(C + C_{gs} + 4C_{gd_o})}{L}$$

Idsat is the drain current under saturation conditions.
A higher gm will be required for non-ideal case using:

$$g_m = \frac{1}{r_{ds}} + \frac{R(C + C_{gs} + 4C_{gd_o})}{L}$$

W is then increased according to Equation 2.22, etc. until convergence is obtained. Tank C can then be adjusted to obtain the require ωo from Equation 2.15 once final values of Cgs, Cgdo , etc., are known. The above method is only approximate and W and gm will have to be adjusted once realistic higher level NMOS models are used (i.e. BSIM3) and transistor layout is completed since actual layout will affect Cgs and Ggdo . The above assumes that one will use a very wide single stripe MOSFET. In real ity multiple finger MOSFETs are used to obtain a total W to reduce series gate resistance and to provide a more compact layout with lower parasitic capacitances. Actual gm should be above the minimum estimated using Equation 2.23 by some safety factor αmin (e.g. 2 or 3). Therefore, incorporate this safety factor into the iteration from the beginning.

Oscillator Phase Noise:

Noise is injected into an oscillator by the devices that constitute the oscillator itself including the active transistors and passive elements.

This noise will disturb both the amplitude and frequency of oscillation.

Amplitude noise is usually unimportant because non-linearities that limit the amplitude of oscillation also stabilize the amplitude noise.

Phase noise, on the other hand, is essentially a random deviation in frequency which can also be viewed as a random variation in the zero crossing points of the time-dependent oscillator waveform.

Let $\gamma(t) = Acos\lfloor \omega_o t + \phi_n(t) \rfloor$ where A is the noiseless oscillator amplitude, ω_o is the oscillator frequency, $\phi_n(t)$ is the phase noise, $\gamma(t)$ is the oscillator output signal.

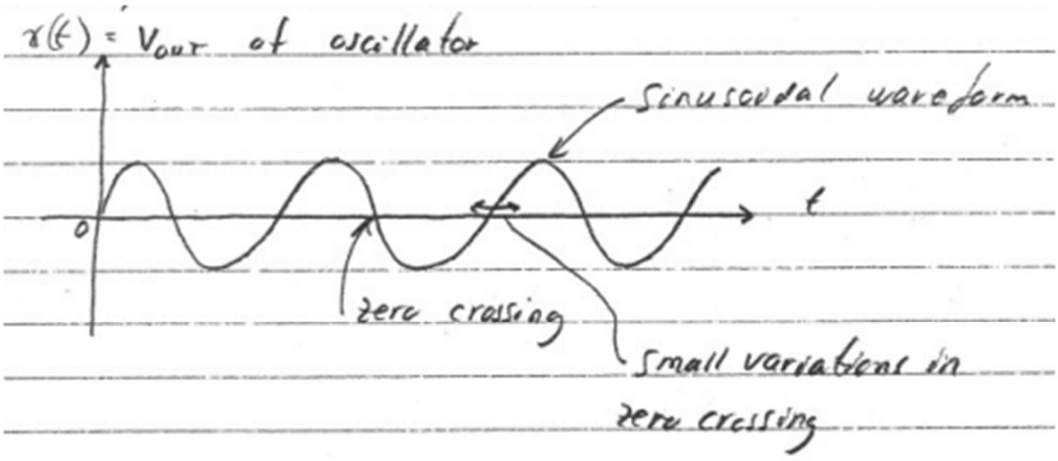


Figure 2.9: Illustration of phase noise in the time domain.

For Small $\phi_n(t)$

$$\gamma(t) = A\cos\lfloor\omega_o t + \phi_n(t)\rfloor$$
$$= A\lfloor\cos(\omega_o t)\cos(\phi_n(t)) - \sin(\omega_o t)\sin(\phi_n(t))\rfloor$$
$$\approx A\cos(\omega_o t) - A\phi_n(t)\sin(\omega_o t)$$

since $\cos(\phi_n(t)) \approx \cos(0) = 1$ and $\sin(\phi_n(t)) \approx \phi_n(t)$ for small $\phi_n(t)$

$\therefore$ the spectrum of the noise noise $\phi_n(t)$ is effectively translated to the oscillation frequency ω_o

i.e. the phase noise signal is amplitude modulating a sinusoid signal of frequency ω_o that is in turn superimposed on the ideal oscillator itself.

An oscillator, however, is a frequency selective (or narrow band, high quality factor) circuit and will tend to reject out of band (i.e. frequencies offset from ω_o) signals to some degree. This rejection increases at larger offsets from ω_o.

As a result, the effect of the noise sources is to produce "skirts" on either side of the ideal impulse function of the oscillator in the frequency domain.

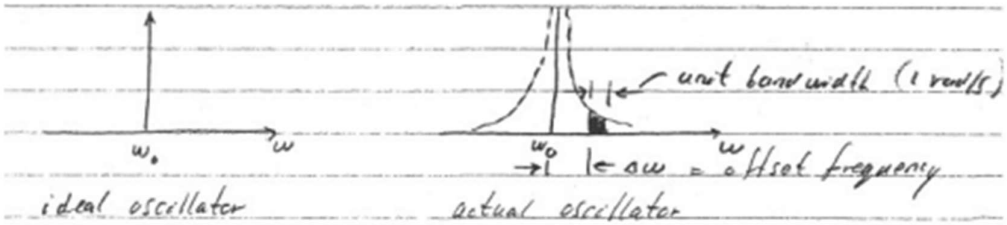


Figure 2.10: Illustration of phase noise in the frequency domain.

To measure or quantify phase noise, one considers a unit bandwidth at an offset $\Delta\omega$ with respect to ω_o, calculates the noise power in this bandwidth, and divide the result by the average carrier power.

e.g. carrier power = -2dBm, noise power measured in a 1kHz bandwidth at an offset of 1MHz = -70 dBm

0 dBm

= 1 mW of power,

dBm

$= 10\log_{10}(\frac{Power\_in\_watts}{10^{-3}watts})$

$= 10\log_{10}(Power\_in\_mW)$

$\therefore$ -70dBm $= 10\log_{10}(Power\_in\_mW)) \implies = -70dBm \Leftrightarrow P = 10^{-7}mW = 10^{-10}W$

$\therefore$ noise power in 1Hz bandwidth $= \frac{10^{-7}}{10^3} = 10^{-10}mW/Hz \Leftrightarrow 10log_{10}(10^{-10}) = -100dBm$

Dividing by carrier power amounts to adding 2dBm

$\therefore$ phase noise = -100 - (-2) = -98 dBc/Hz

dBc means "in dB with respect to carrier power."

Quality Factor of the Oscillator:

Phase noise of an LC oscillator depends on the Q of the LC tank circuit.

For an LC tank, Q is an indication of how much of the energy is lost as it is transferred from the capacitor to the inductor and vice versa.

Three Definitions of Q

1) One definition of Q defines it as:

$2\pi\frac{energy\_stored}{energy\_dissipated}$ per cycle

2) Q can also be defined as the "sharpness" of the magnitude of the frequency response

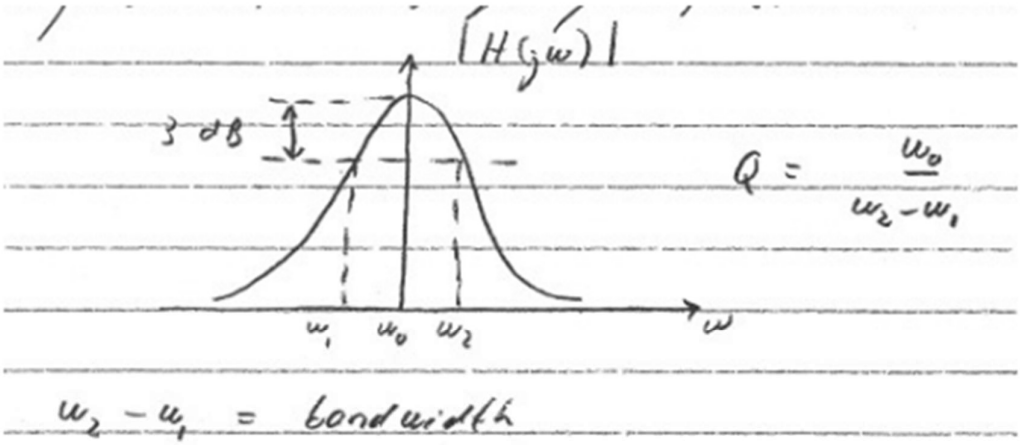


Figure 2.11: Calculation of Q from the frequency response.

3) Q can also be defined with respect to the phase of the open-loop transfer function $\phi(\omega)$ at the resonance of the LC tank in an oscillator

$Q = \frac{\omega_o}{2}\left|\frac{d\phi(\omega)}{d\omega}\right|$ at $\omega = \omega_o$

where ω_o = resonant frequency

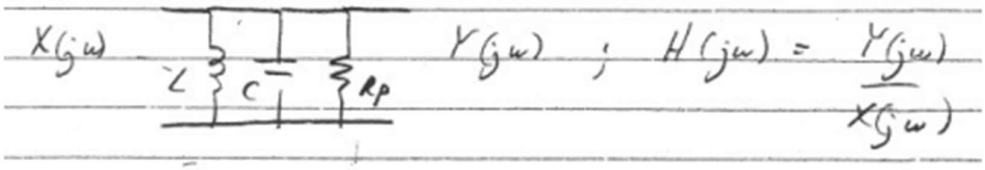


Figure 2.12: LC tank VCO open-loop transfer function.

$H(j\omega) = Z(j\omega)$ = open-loop transfer function

$$\phi(j\omega) = tan^{-1}\left(\frac{Imag(Z(j\omega))}{Real(Z(j\omega))}\right)$$

$$\frac{1}{Z} = j\omega C + \frac{1}{j\omega L} + \frac{1}{R_p} = j\left(\omega C - \frac{1}{\omega L}\right) + \frac{1}{R_p}$$

$$Z = \frac{1}{j(\omega C - \frac{1}{\omega L}) + \frac{1}{R_p}} = \frac{j(\frac{1}{\omega L} - \omega C) + \frac{1}{R_p}}{((\omega C - \frac{1}{\omega L}))^2 + (\frac{1}{R_p})^2}$$

$$\phi(j\omega) = tan^{-1}\left(\frac{\frac{1}{\omega L} - \omega C}{\frac{1}{R_p}}\right) = tan^{-1}\left(\frac{R_p(1-\omega^2 LC)}{\omega L}\right) = tan^{-1}[R_p(\omega L)^{-1}(1-\omega^2 LC)]$$

use $\frac{d(tan^{-1}u)}{dx} = \frac{1}{1+u^2}\frac{du}{dx}$

$$\therefore \frac{d\phi}{d\omega} = \frac{1}{1+(\frac{R_p}{\omega L}(1-\omega^2 LC))^2}\left[\frac{-R_p}{(\omega L)^2}(1-\omega^2 LC) - 2\frac{\omega LC}{\omega L}R_p\right]$$

$$\omega_o = \frac{1}{\sqrt{LC}} \therefore 1 - \omega_o^2 LC = 0$$

$$\therefore \frac{d\phi}{d\omega}|_{\omega=\omega_o} = -2CR_p$$

$$\frac{\omega_o}{2}|\frac{d\phi}{d\omega}|_{\omega-\omega_o} = \omega_o CR_p = \frac{R_p}{X_C} \text{ where } X_C = \frac{1}{\omega_o C}$$

at resonance $X_L = X_C$ where $X_L = \omega_o L$

$$\therefore \boxed{Q = \frac{\omega_o}{2}|\frac{d\phi}{d\omega}|_{\omega=\omega_o} = \omega_o CR_p = \frac{R_p}{\omega_o L}}$$

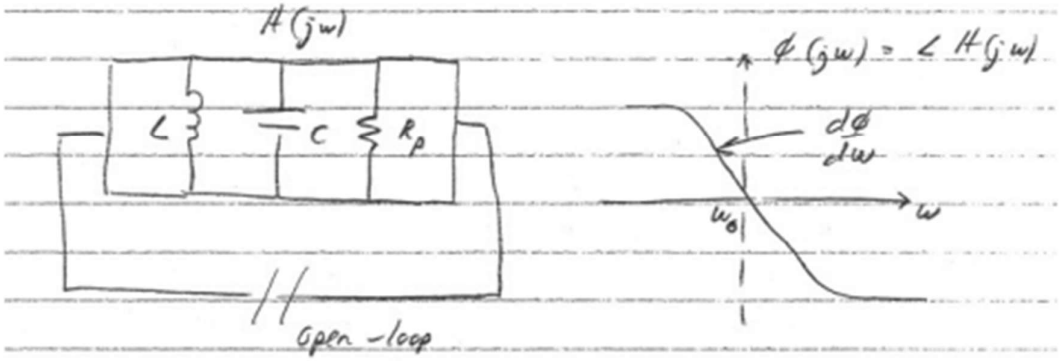


Figure 2.13: LC tank and phase function.

For steady state oscillation, the total phase shift around the feedback loop must be zero.

If the oscillator frequency ω deviates slightly, say due to noise injection, then the larger the change in the loop phase the greater the tendency for the oscillator to return to its center frequency.

The open-loop Q is a measure of how much the closed-loop system opposes variations in the frequency of oscillation.

3 Design

3.1 Design Method

Certain design specifications must be given:
a) max d.c. power dissipation = VsupplyIbias
b) min output voltage swing (single-ended) = Vtank
c) tuning range in percentage = ωmax−ωmin ωo × 100%
d) αmin > 1

e) chip area
f) Frequency of operation (ωo) The goal of the design is then to develop a VCO that meets the above constraints with minimum phase noise. An alternative strategy may be to design a VCO with a pre-specified phase noise but where the d.c. power dissipation is minimized.

Design Procedure Steps:

1) Set $I_{bias} = \frac{P_{d.c.max}}{V_{supply}}$

2) Determine max Q_L of inductors for a given process at required frequency ω_o. This can be determined in may ways including

i) already known from previous design experience in that particular process

ii) read from model elements in design kit

iii) determined through exhaustive design and optimization of inductor using electromagnetic simulation packages

iv) measured data taken from test inductors already fabricated in the same process.

3) Using $V_{tank} = I_{bias}R_p = I_{bias}\omega_o L Q_L$, set L so that V_{tank} is at the minimum required voltage swing for the design. I_{bias}, ω_o and Q_L area already known.

Caution: values of L must be chosen such that it is in a practical value range to be fabricated as well as being at a value that results in a practical value of capacitance, C, for the varactor.

4) Using $\omega_o = \frac{1}{\sqrt[2]{LC}}\sqrt[2]{1 - \frac{R^2C}{L}}$ where $R = \frac{\omega_o L}{Q_L}$ = effective series resistance of inductor, calculate the required value of C for the LC tank with ω_o being the center frequency of the VCO.

5) Given the minimum closed loop gain $\alpha_{min} > 1$ calculate the minimum transconductance of each NMOS transistor g_m such that $g_m = \alpha_{min}\frac{RC}{L}$

6) Take transistor non-idealities into account to arrive at a new g_m and also a transistor width, W, *as per Prof. Hamel's E&CE 439 lecture notes*.

3.2 Circuit Diagram

3.3 Full Source Code of Firmware

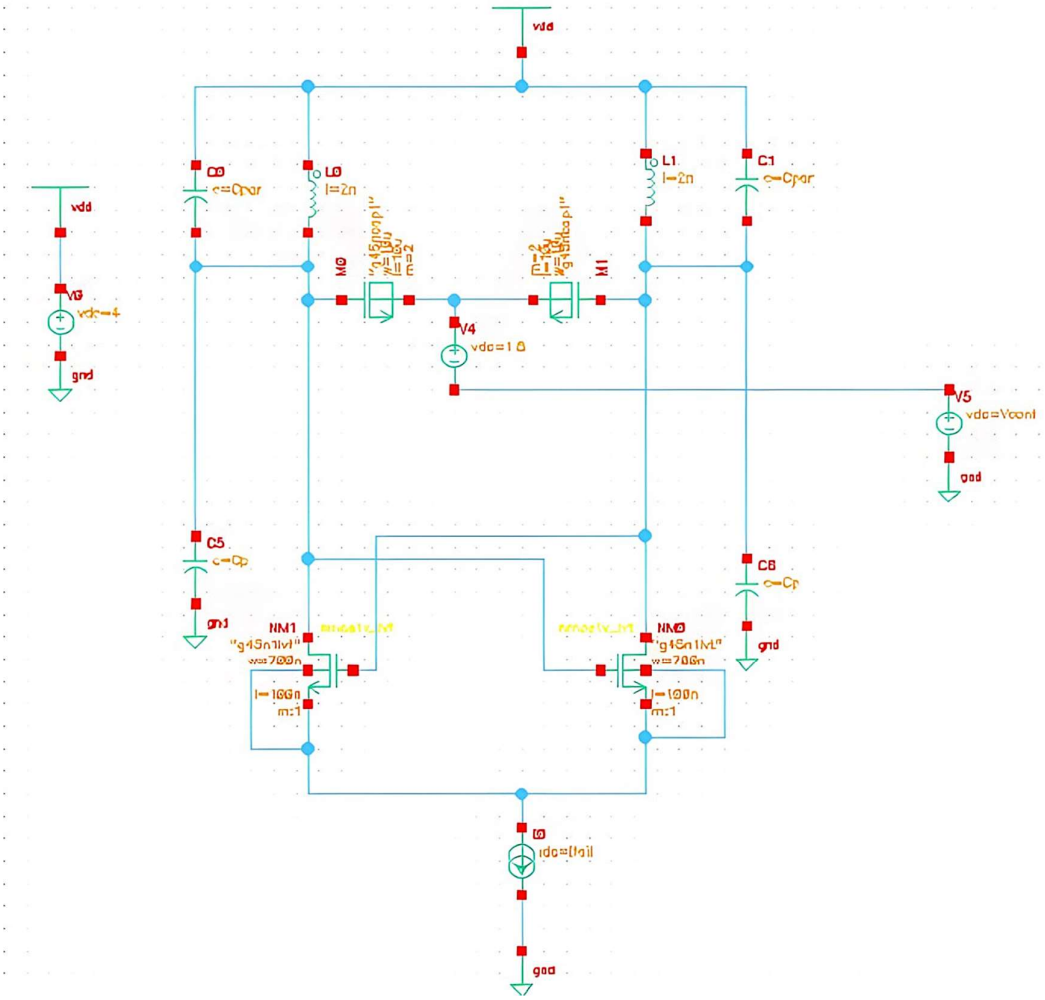
Use small font size, Consolas Size 7, double column Test	

Table: Source Code for the main program

4 Implementation

4.1 Description

The voltage Controlled Oscillator designed below is an LC Cross coupled VCO. We have used two cross coupled NMOS from gpdk045 library of Cadence Virtuoso. The model of the NMOS is nmos1v. We have chosen W=700nm and L=100nm, that is, a W/L ratio of 7. The tail current source provides 40mA current. The supply voltage is 4V. The LC tank has an inductor of 2nH and two capacitors. One of them is a paracytic capacitor (cpar) and the other one is the contributing capacitor of the LC tank.



Two varactor capacitors, that is, nmos with drain, body and source shorted, havev been used for the variable capacitor network. At the junction of the two varactor capacitors' drain (or body/source), a control voltage is given to tune the frequency from 850 to 880 MHz. The model of the varactor we have used in our circuit is nmoscap1v of gpdk045 library. We have taken Cp=14.5Pf and Cpar=4fF.

We have also made a layout of our VCO circuit. We have used the layout of generic inductor and capacitor from gpdk045 library.

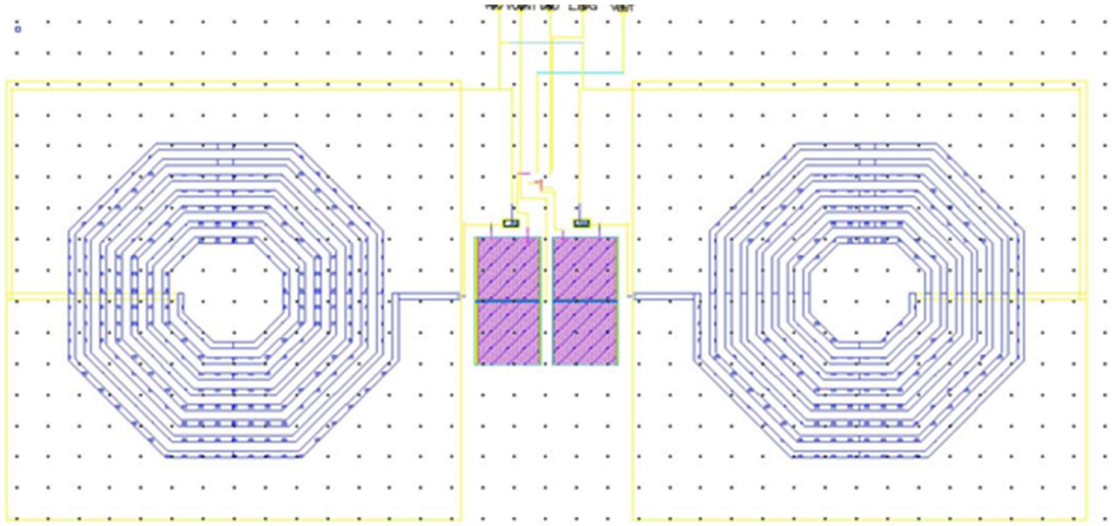


Figure: Layout of LC Cross Coupled Voltage Controlled Oscillator Circuit

4.2 Results

The differential output of our designed VCO is a sinusoid. Initially there is a build up of oscillation as can be seen from figure 3. The plot has been taken for the control voltage of 2.4 V.

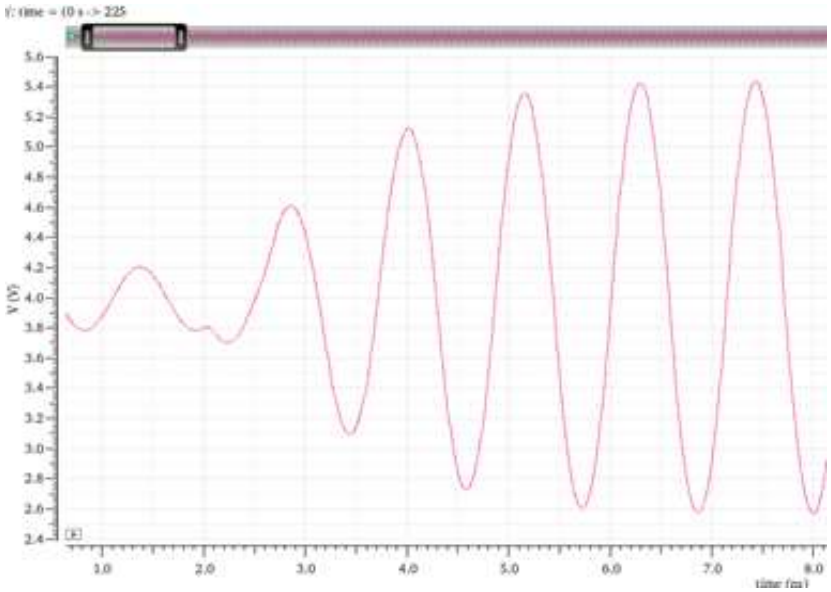


Figure 3 : Initial build up of Oscillation of the sinusoid (Vcont=2.4 V)

At stable condition, we get an almost clean sinusoidal output with a frequency of 880MHz and a peak to peak voltage of 2.8724V.

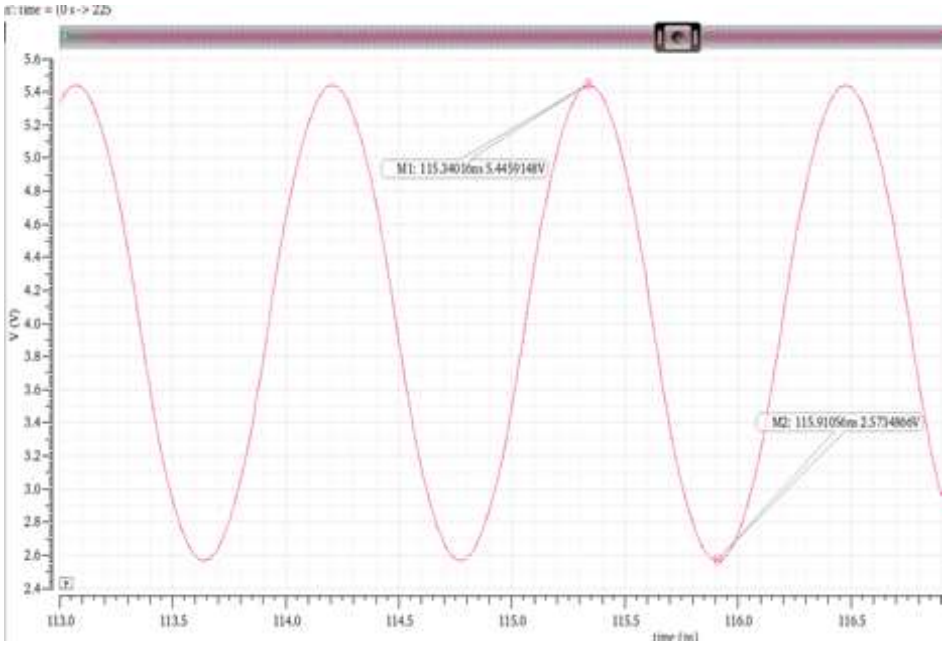


Figure 4: Output at Stable condition (Vcont=2.4V)

The sine wave has a DC offset of 4 V since we have energized the LC tank with 4 V power supply. For the control voltage of 2.4 V, we get a frequency of 880 MHz.

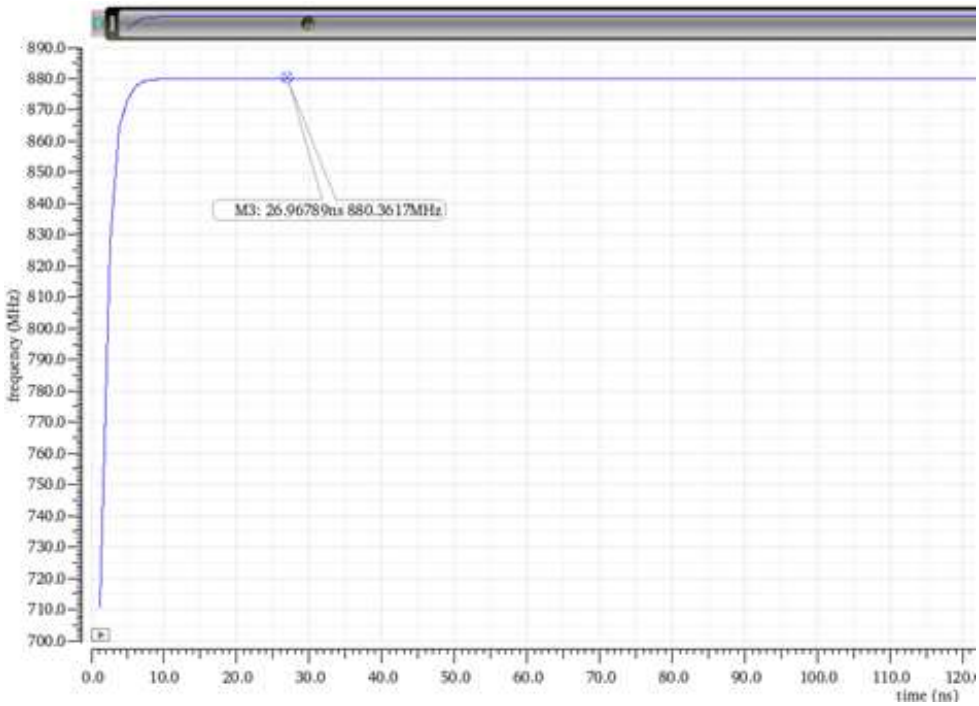


Figure 5: Frequency = 880 MHz at stable condition

For a control signal of 0.5 V, we get a frequency of 856 MHz and a peak to peak voltage of 1.124 V

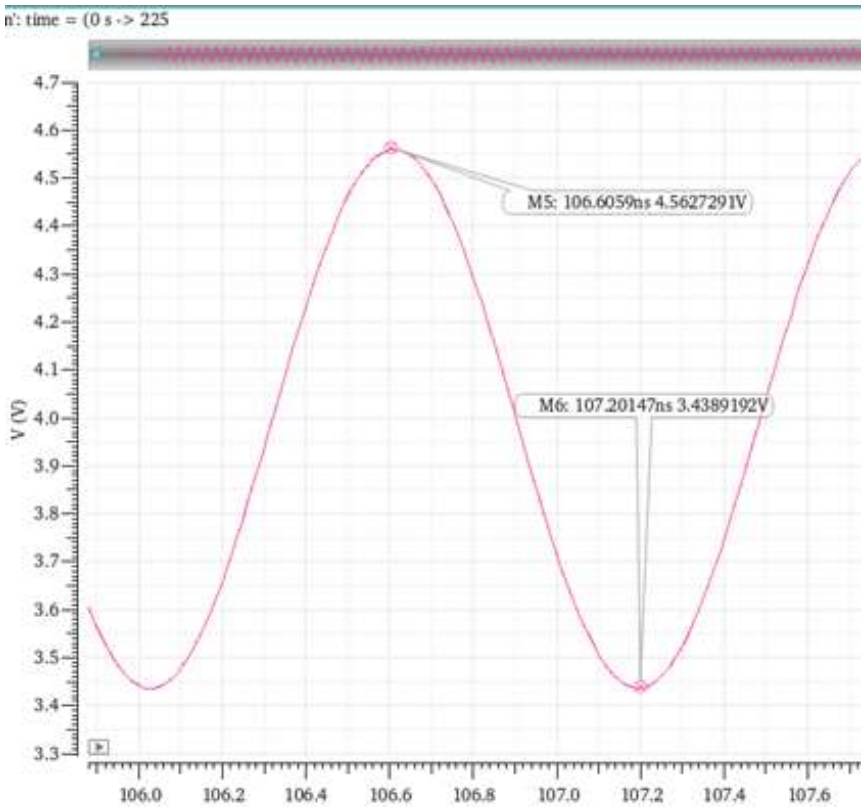


Figure 6 : Stable Oscillation at Vcont = 0.5 V

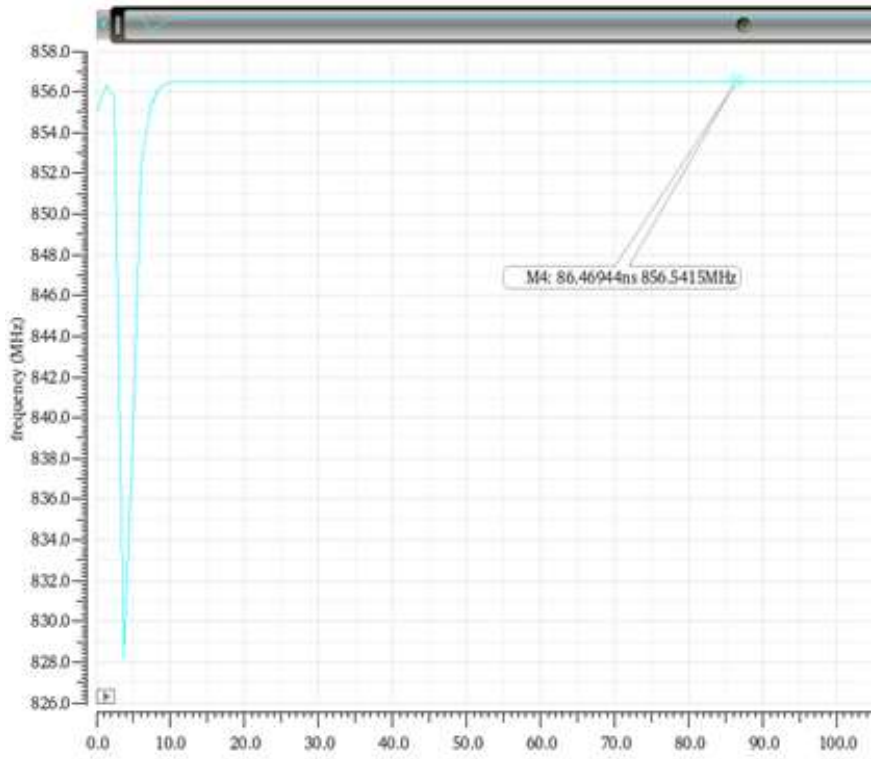


Figure 7: Frequency of 856 MHz at Vcont= 0.5 V

For a control signal of 1.4 V, we get a frequency of 870 MHz and a peak to peak voltage of 2.183 V.

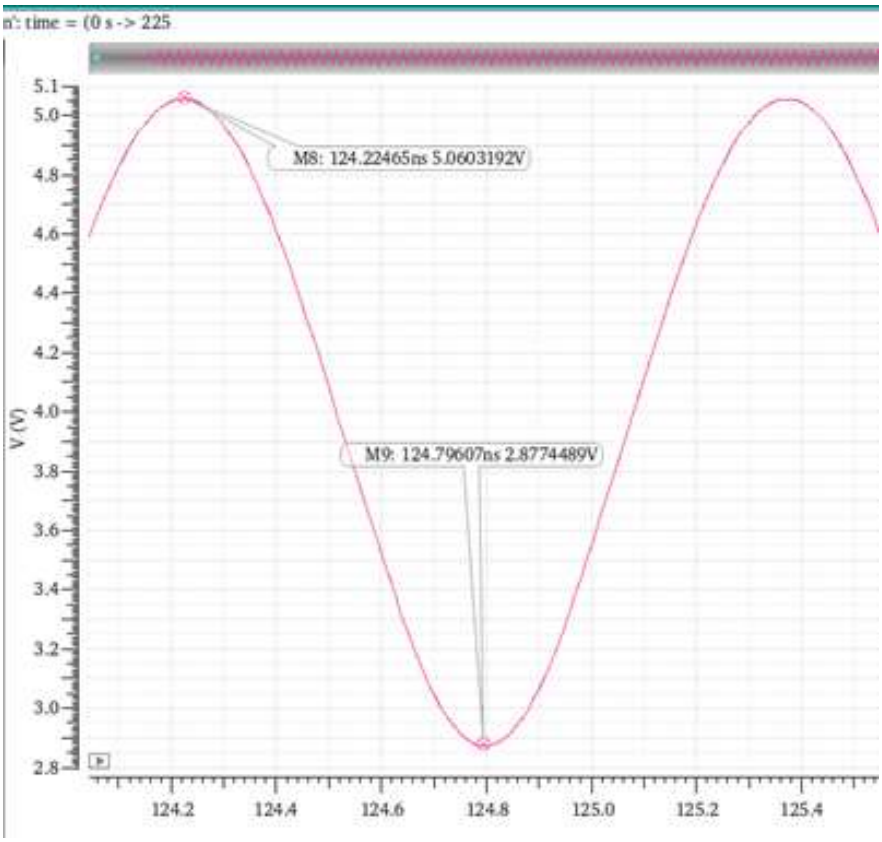


Figure 8 : Stable Oscillation at Vcont = 1.4 V

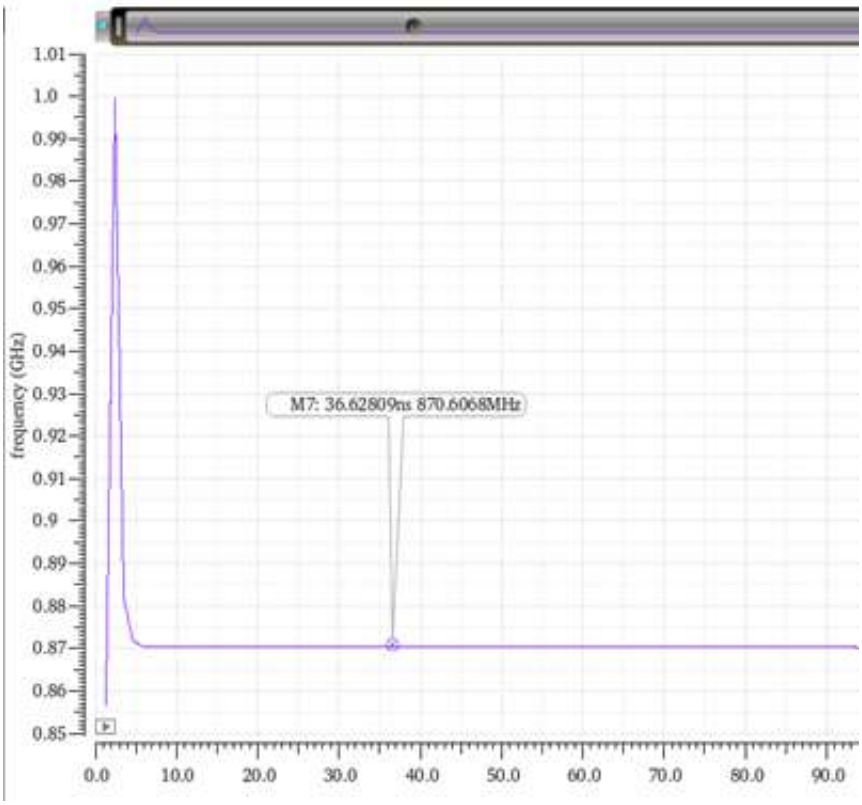


Figure 9: Frequency of 870 MHz at Vcont= 1.4 V

Comparison:

Control Voltage (V)	Frequency (MHz)	Peak to Peak Voltage (V)
0.5	856	1.124
1.4	870	2.183
2.4	880	2.872

We can observe from the table that, with an increase in frequency, there is an increase in peak to peak voltage of the sinusoidal output. The reason is the variable impedance of the LC tank at different frequency. The LC tank serves as a load to the common source NMOS configuration. With the change in the impedance of the load, the output resistance also changes and the output voltage thus changes with frequency.

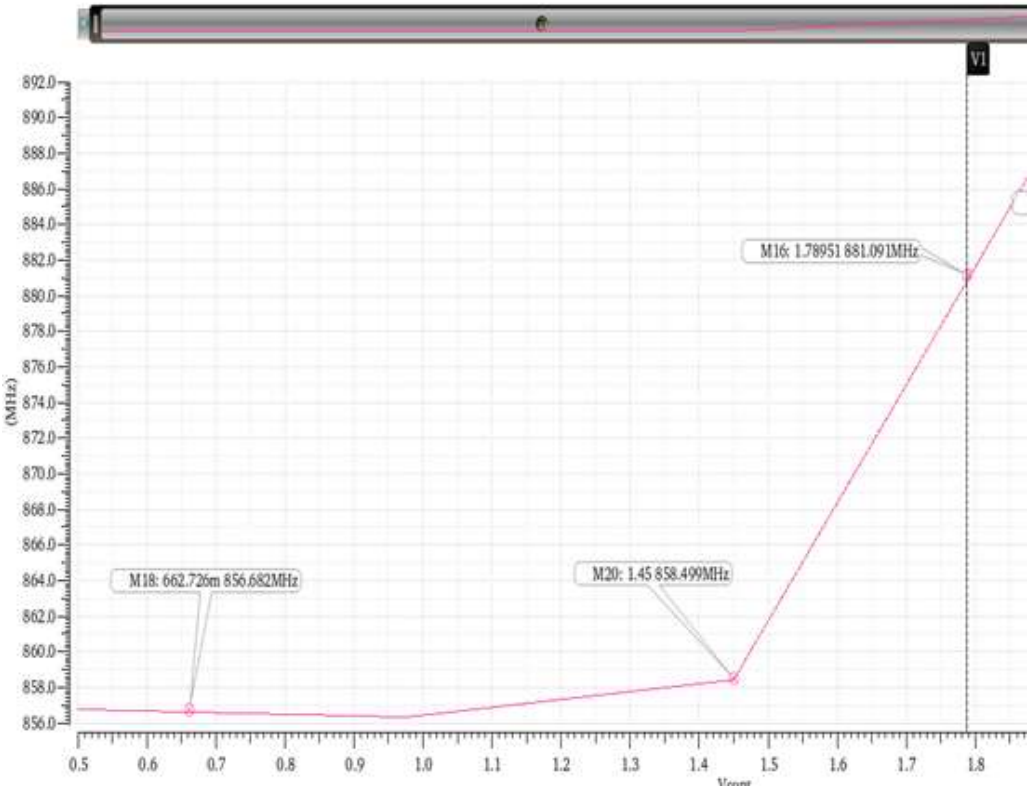


Figure 10: Control Voltage VS Frequency

The plot shows that, there is a very satisfactory linear region from the control voltage of 1.45 V to 1.8 V with a frequency range of 858 MHz to 881 MHz. In this operating region, the VCO serves as a linear device.

Phase Noise:

For a control voltage of 0.5 V, we get phase noise of -152.192 dBc/Hz. The result is satisfactory and lower than the maximum value of phase noise of -130 dBc/Hz according to the specification.

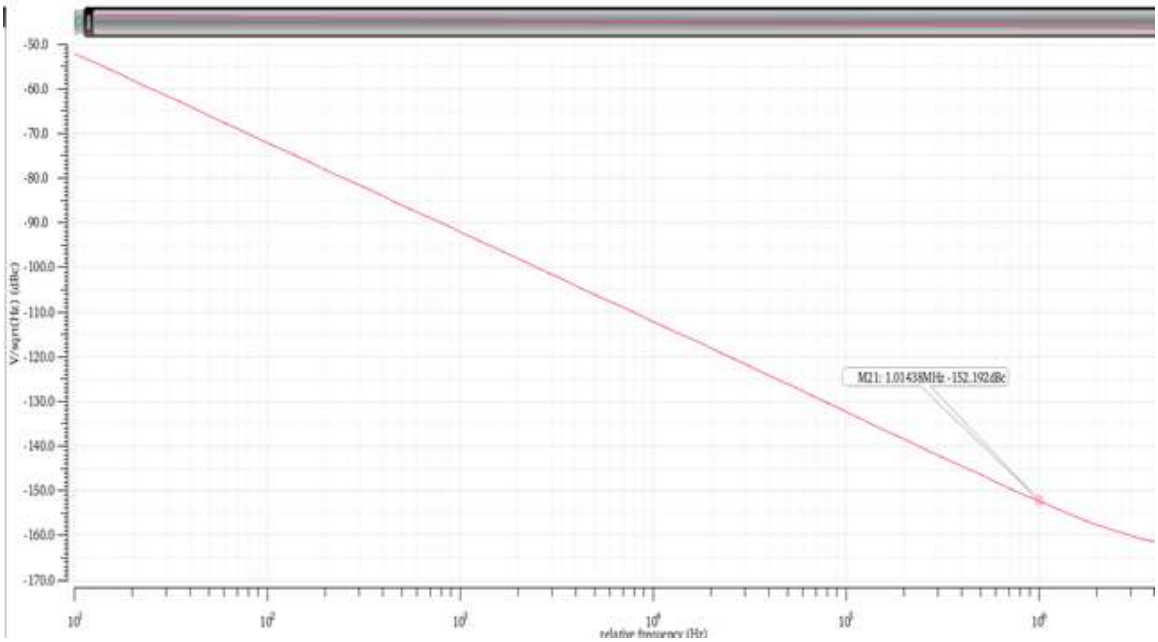


Figure 11: Phase Noise for Vcont = 0.5V at 1 MHz offset

For a control voltage of 2.4 V, we get phase noise of -157.967 dBc/Hz. The result is satisfactory and lower than the maximum value of phase noise of -130 dBc/Hz according to the specification.

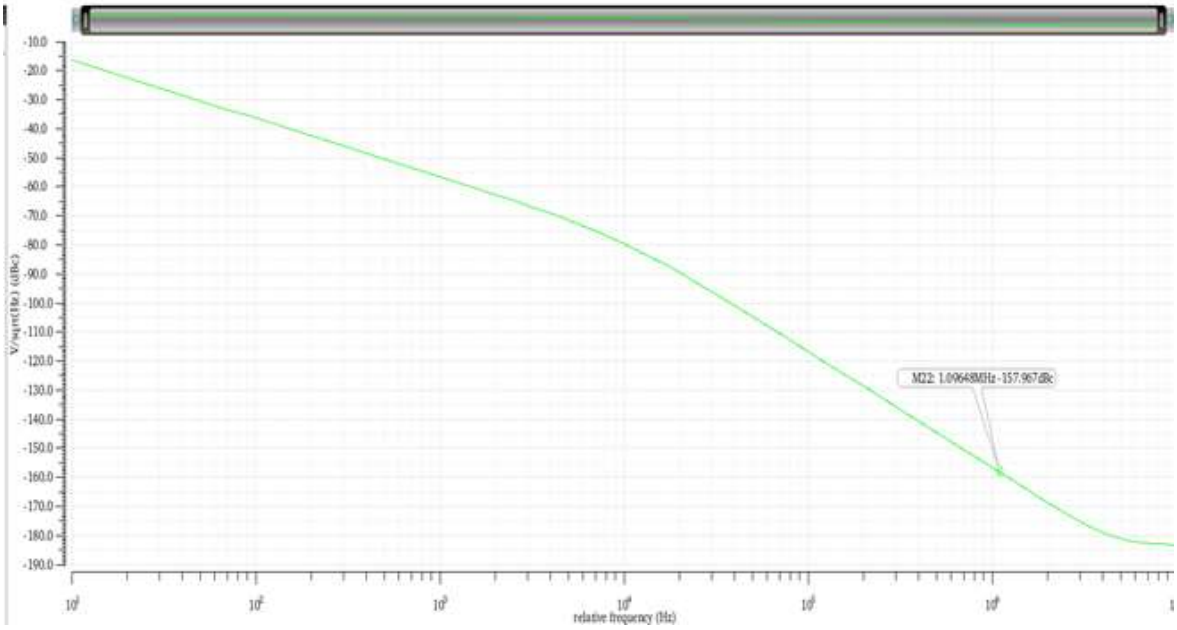


Figure 12: Phase Noise for Vcont = 2.4 V at 1 MHz offset

Output Power:

The output power is -6.57 dBm when control voltage is 0.5 V and 12.2588 dBm when control voltage is 2.4 V

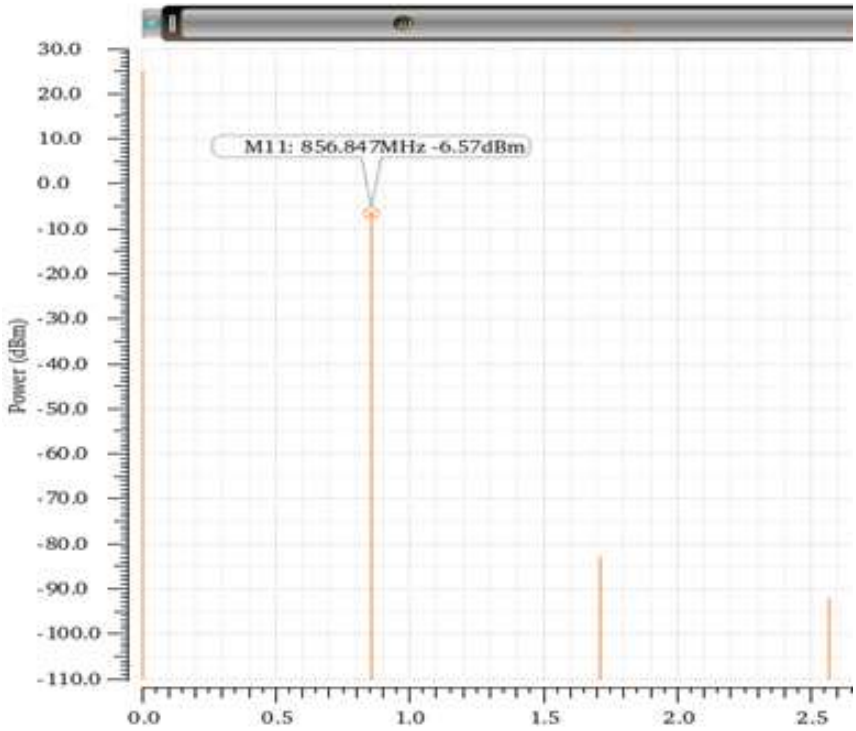


Figure 13: Output Power of the first harmonic when vcont=0.5V

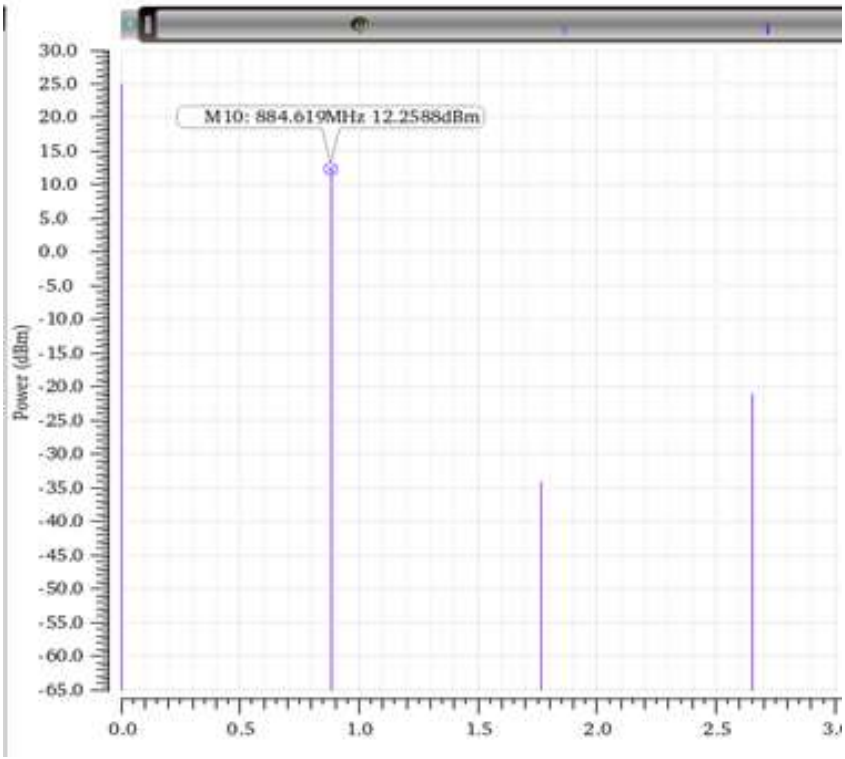


Figure 14: Output Power of the first harmonic when vcont=2.4 V

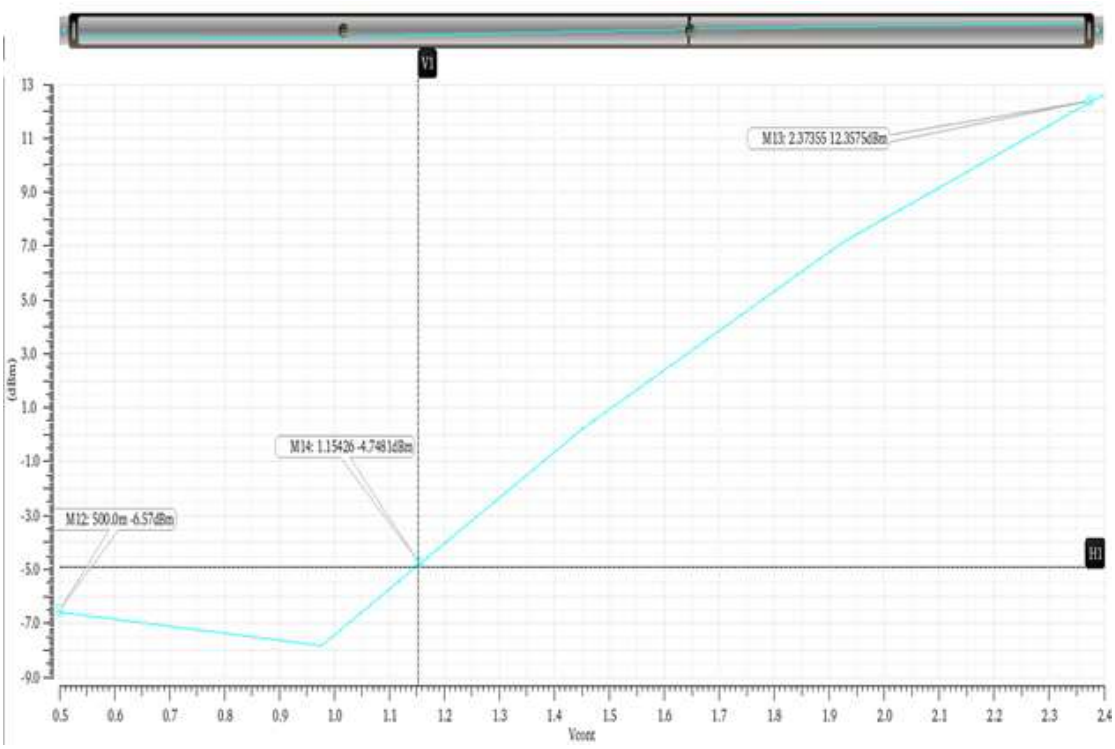


Figure 15: Control Voltage VS Power (dBm)

From 1.15 V , the output power is above -5dBm and linear for the rest of the range of control signal. Overall, the design meets all the specifications more or less

5 References

[1] Design of Analog CMOS Integrated Circuits, Second Edition, Behzad Razavi
[2] LC Tank Voltage Controlled Oscillator Tutorial, John Starr Hamel, Ryan Norris