Lab Report: EEE 466
Group No 15
Lab No 02

LAB TITLE: Study of Single Stage Common Source CMOS Amplifier Design

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ABSTRACT

In this experiment, we simulated five topologies of single-stage CS amplifier. The five configurations were all CS amplifiers with different loads such as: Resistive load, Diode connected load, Current source load, Active load and Triode load. We first applied a bias voltage and then superimposed a small AC signal of 10mV at the input. Then a small signal AC analysis was carried out and the amplifier output was plotted.

KEYWORDS:

Single-stage, CS amplifier, Load, AC analysis, Bias

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INTRODUCTION

A common-source amplifier is one of three basic single-stage field-effect transistor (FET) amplifier topologies, typically used as a voltage or transconductance amplifier. This amplifier has higher input resistance They are commonly used in power supplies, motor control circuits, and audio amplifier. Ther are one of the most used configurations and hence it is significantly important to learn the different topologies as studied in this experiment,

THEORY

CS amplifiers do not have a linear input-output relation but we can however approximate it to a linear equation for a small range of input AC signal. This is called the small signal analysis. We can get the small signal gain Av from the slope of the linear input-output function. The formulas for Av in the five topologies are as below:

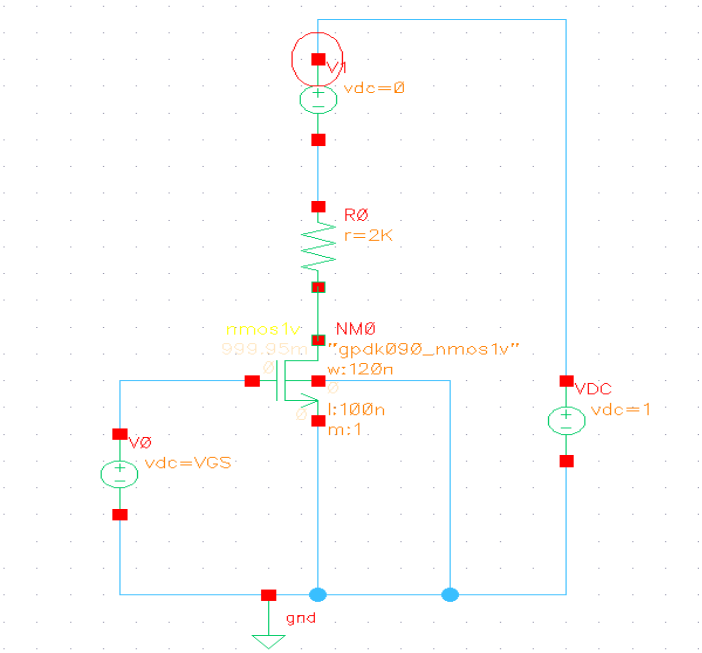
1. Common-Source (CS) Stage with Resistive Load: $Av = -g_m R_D$
2. Common-Source (CS) Stage with Diode Connected Load: $Av = \text{sqrt}((W_1/L_1)/(W_2/L_2))\text{^}0.5$
3. Common-Source (CS) Stage with Current Source Load: $Av = -g_{m1}(r_{O1} \parallel r_{O2})$
4. Common-Source (CS) Stage with Active Load $Av = -g_{m1}r_{O1}$
5. Common-Source (CS) Stage with Triode Load: $Av = -g_{m1}R_{om2}$

TOOLS USED

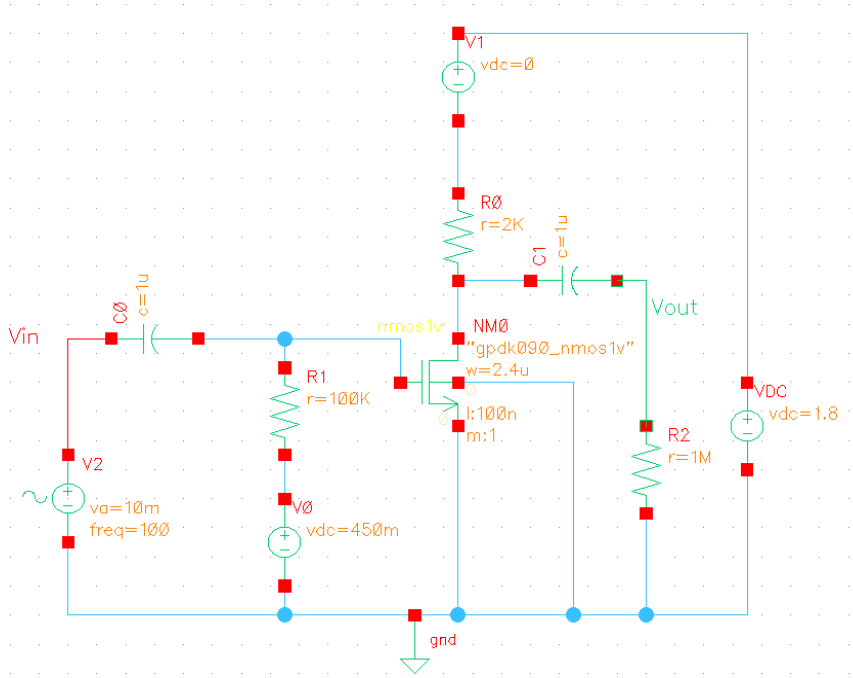
Cadence, Virtuoso, Simulation Software

PROCEDURE

1-1. Common-Source (CS) Stage with Resistive Load:

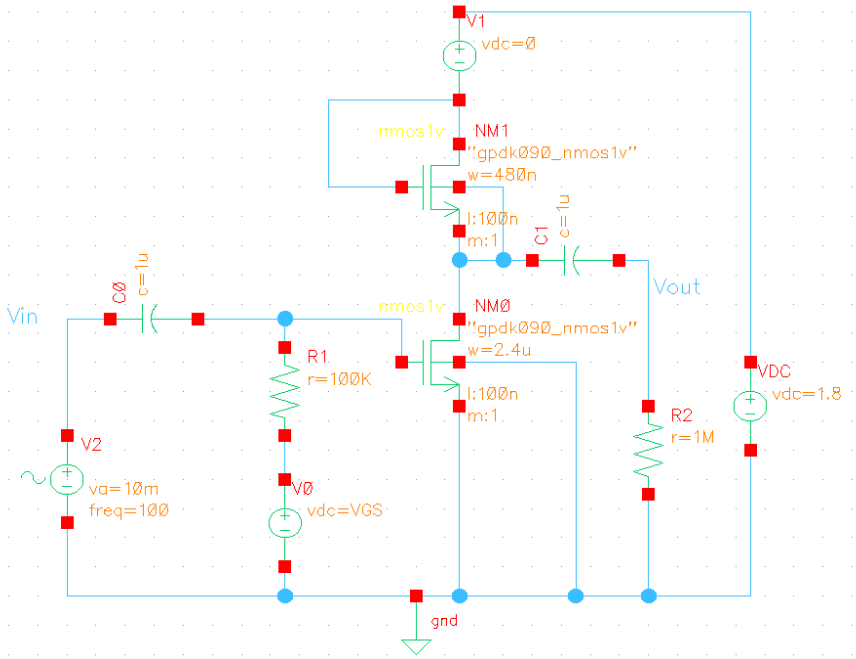


First, we biased the transistor keeping V_{DC}=1 V and varying V_{GS}. From this we got the plot of g_m vs V_{gs} and determined the maximum g_m point. We then chose Vgs = 450 mV as the gate bias which will be effective for rest of the circuits.



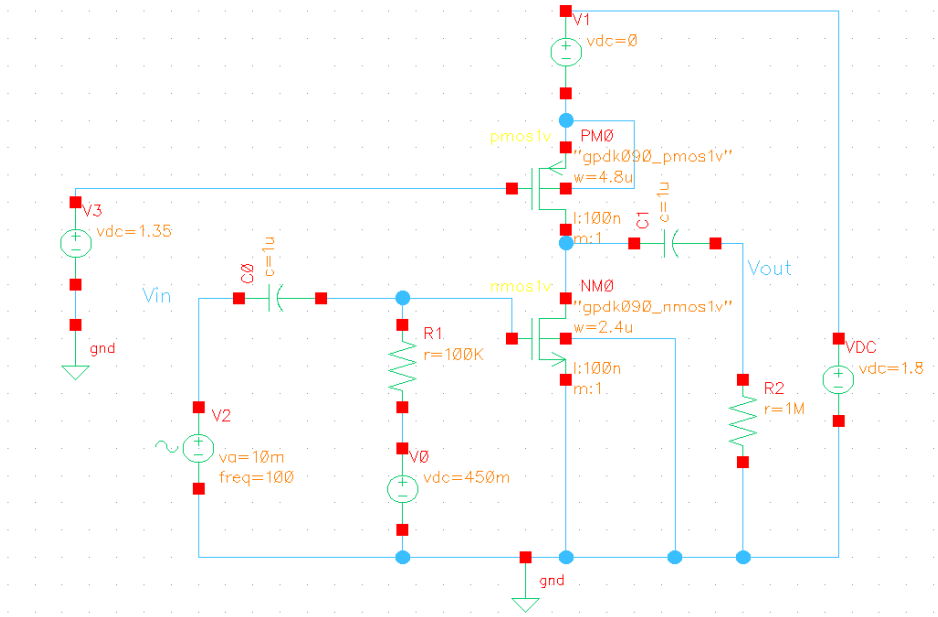
Next we set the circuit with a small signal AC of 10 mV and 100 Hz superimposed on the DC bias. From this we got the input output transient analysis plot as well as the gain vs frequency plot via frequency sweep.

1-2. Common-Source (CS) Stage with Diode Connected Load:



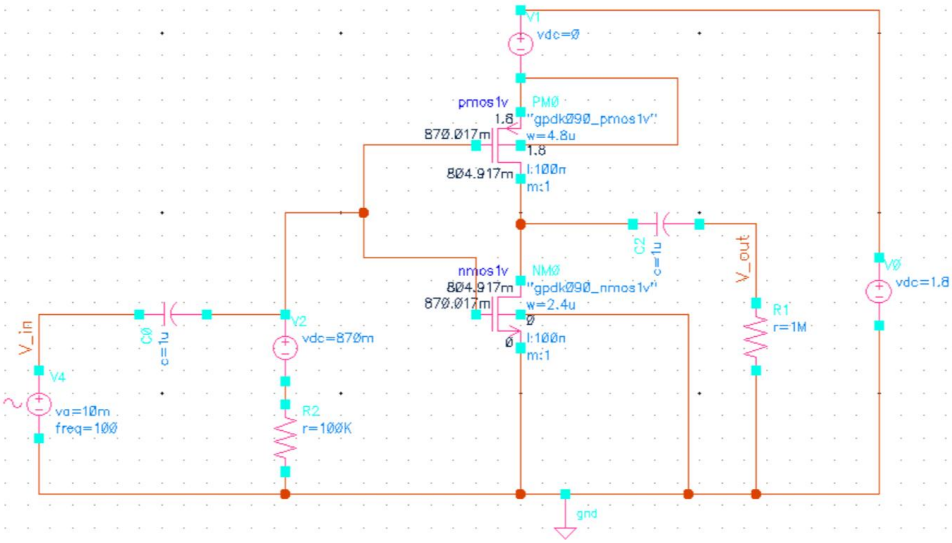
We replaced R_D from the previous circuit with a diode connected NMOS to get this circuit making the second MOS running in saturation, effectively a resistor. This enables us to have alternatives for when it gets complicated to fabricate resistors in a reasonable physical size. From this circuit we acquired the gain vs frequency plot.

1-3. Common-Source (CS) Stage with Current Source Load:



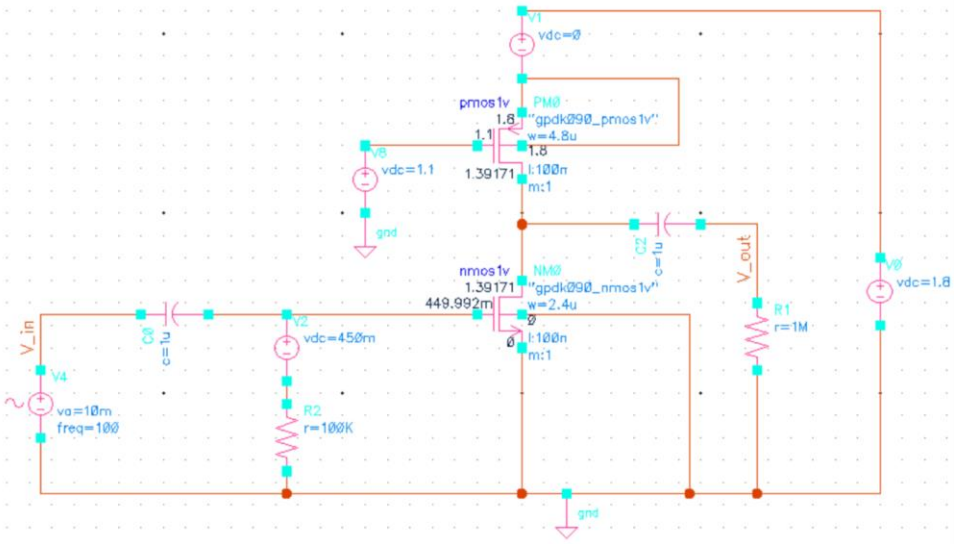
Increasing the load impedance in single stage CS-amplifier increases the gain but that also increases the resistive loss. An alternative to this is using a current source built with MOSFET operating in saturation. In out circuit the resistor has been replaced with a PMOS operating in saturation. We performed ac analysis in two different W/L settings of PMOS to observe the change in amplification.

1-4. Common-Source (CS) Stage with Active Load:



We can also opt for both the MOSFETs operating as amplifying devices making the gain even higher. This makes the additional pMOSFET an ‘active’ load working in saturation. The complementary CS stage helps amplification by each MOS enhance each other. For this circuit we did small signal analysis to get the gain.

1-5. Common-Source (CS) Stage with Triode Load:

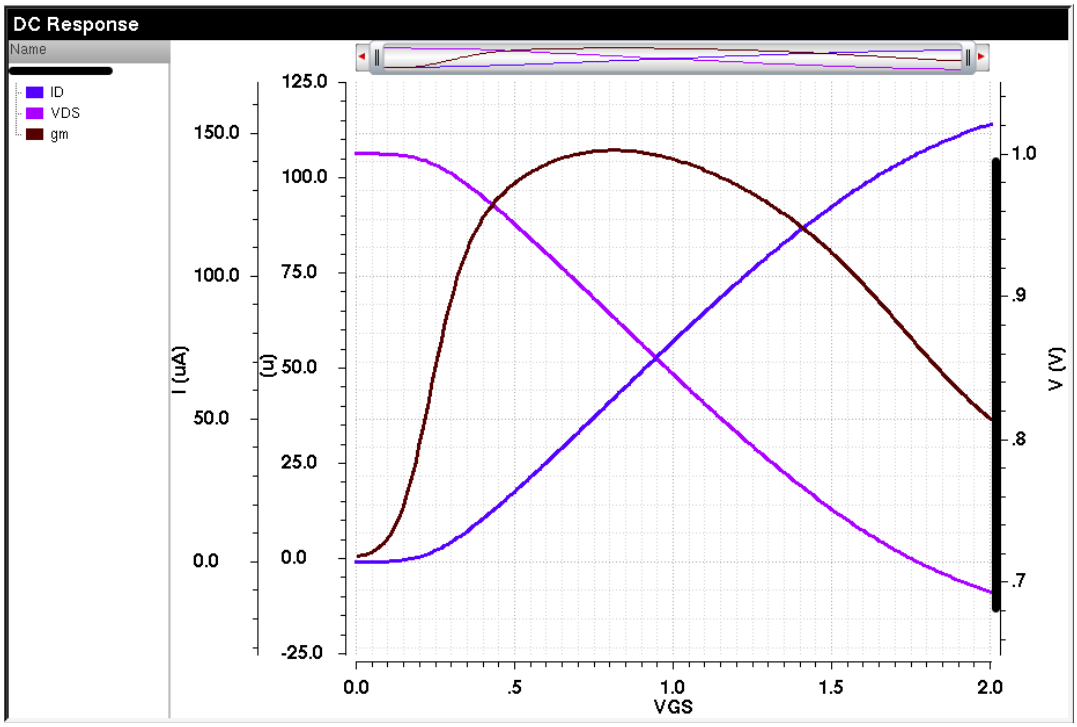


If the additional MOS is made to operate in deep triode region then it behaves like a resistor with almost linear characteristics and therefore can serve as a load in the CS stage. To do this we will need to bias the gate at a sufficiently low level to keep operating in triode region for all output voltage swing. Since it's a PMOS, we applied 1.1 V positive voltage to achieve the desired effect and then did small signal analysis.

RESULTS

1-1. Common-Source (CS) Stage with Resistive Load:

i) **Drain current, output voltage and transconductance vs Vgs for V_{DD} = 1V**

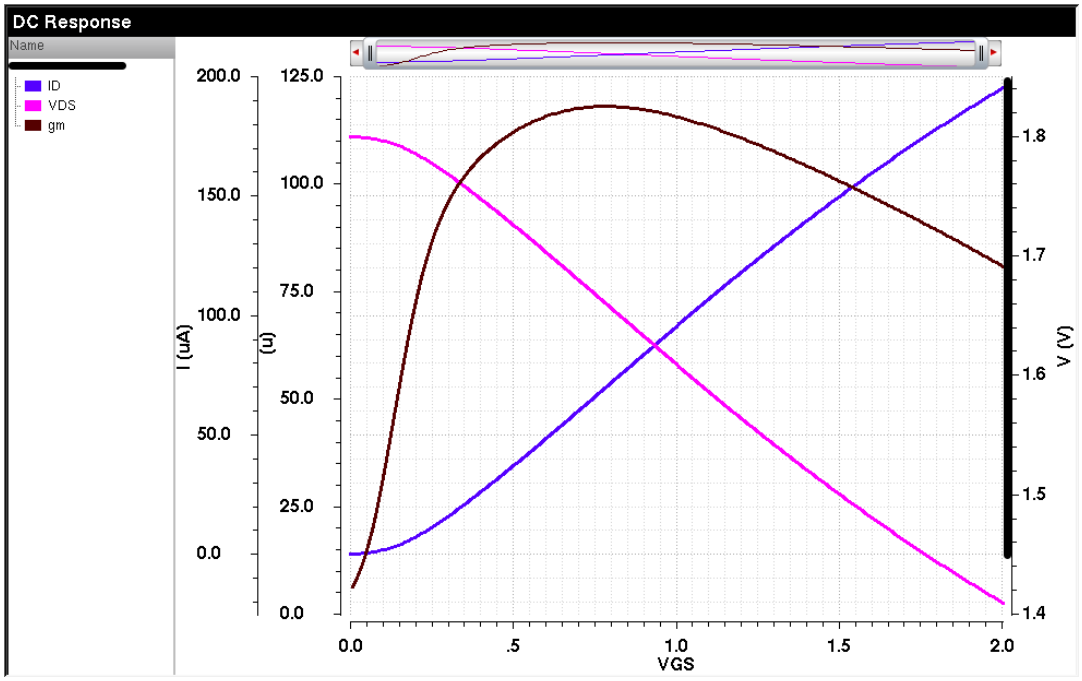


ii) At around Vgs=0.8 mV, gm is maximum of approximately 107u

iii) For a very large voltage swing, the gain will vary with changing Vgs instead of being constant. This leads to nonlinearity which is an undesirable effect. As a result, we may not get the desired output as designed.

iv) To increase the swing, we can increase bias voltage at drain V_{DD}

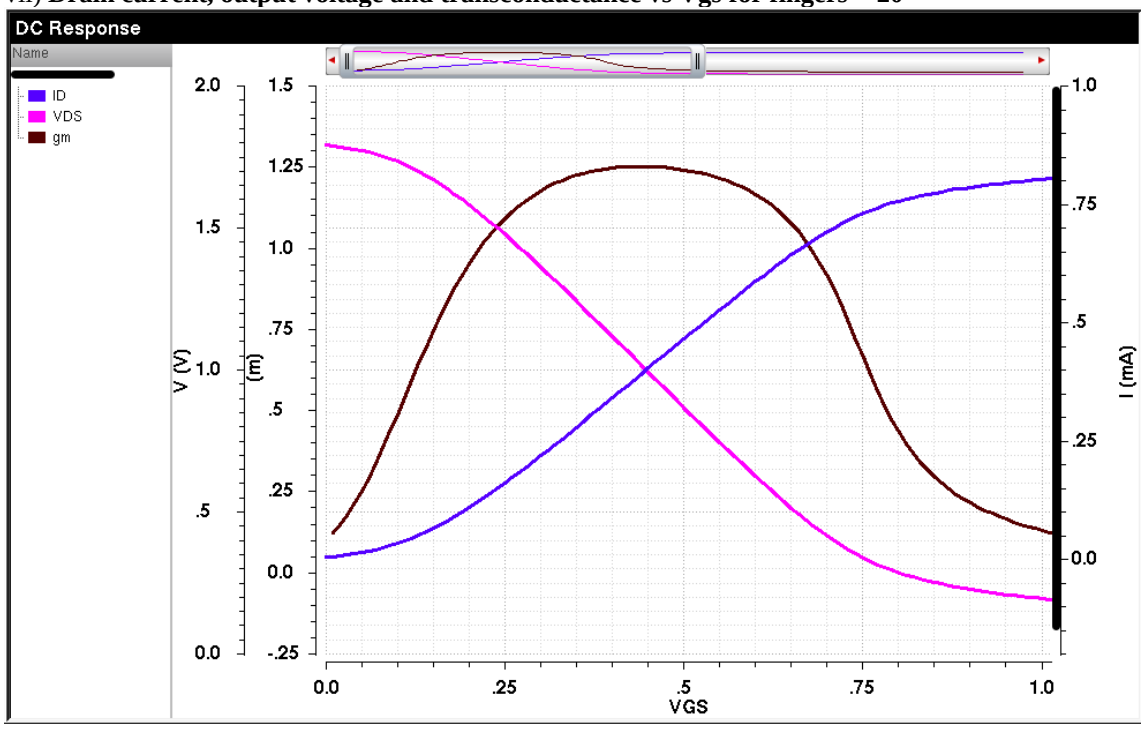
v) **Drain current, output voltage and transconductance vs Vgs for V_{DD} = 1.8 V**



Now, the output swing can be expressed as (VDD – VTH). So, increasing VDD to 1.8V surely increases the swing. However, as seen from the plot, the current swing also increases and thus now consumes more power from the supply.

vi) To increase the gain of this amplifier I would use a current source instead of the resistance this effectively achieving the intrinsic voltage gain A_V = gmro

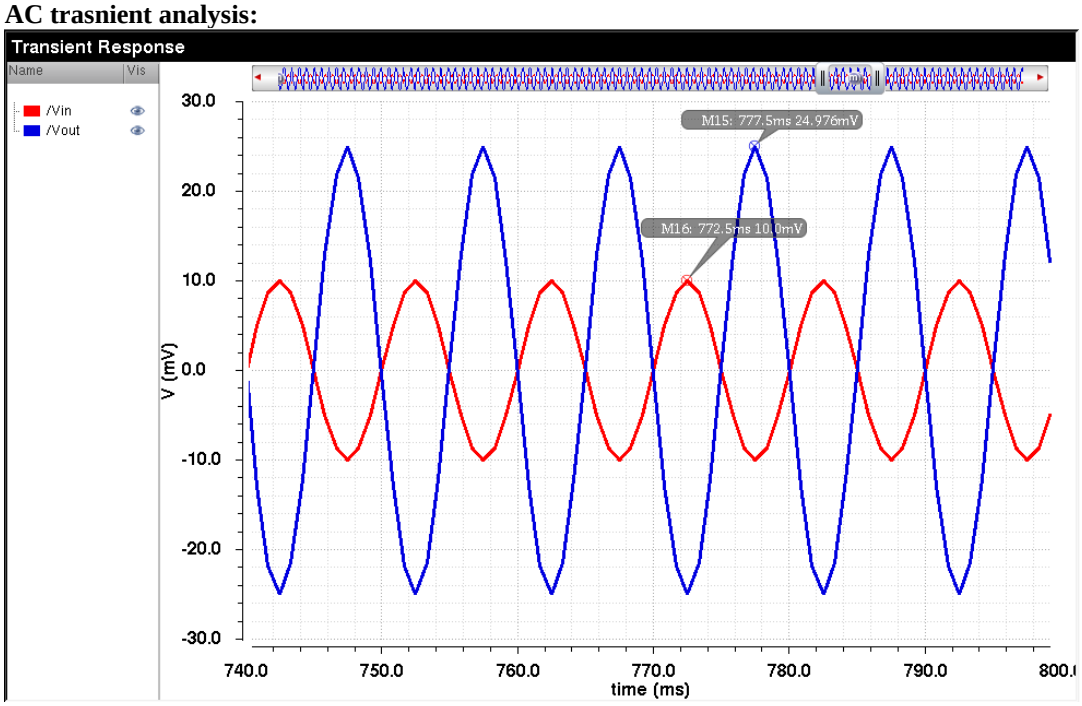
vii) **Drain current, output voltage and transconductance vs Vgs for fingers = 20**



Here increasing fingers increases the width and a larger device size leads to greater device capacitance which is a rather problematic effect. This then limits the voltage swing. Now, the gain increases significantly with a maximum gm of around 1.25 m. But the current swing increases as well, going from uA to mA range and thus consumes more power now compared

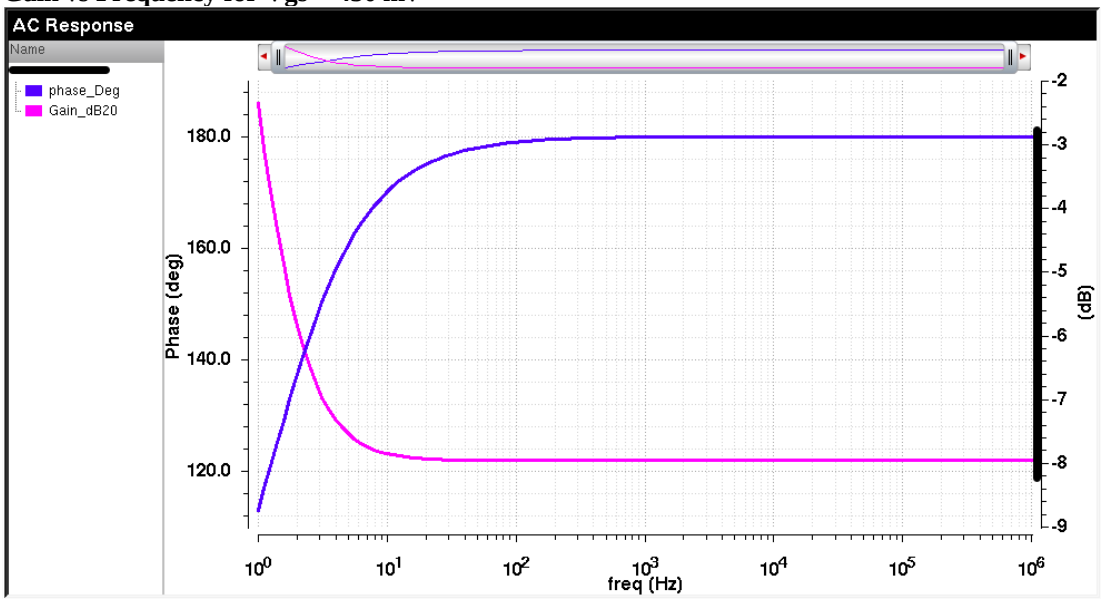
to the previous cases.

AC trasnient analysis:



The output is inverted due to the negative gain effect. Theoretically, $A_V = - g_m R_D = 1.25m * 2k = - 2.5$
From the plot, AV = -24.976m / 10m = - 2.49 So, the simulation is pretty exact.

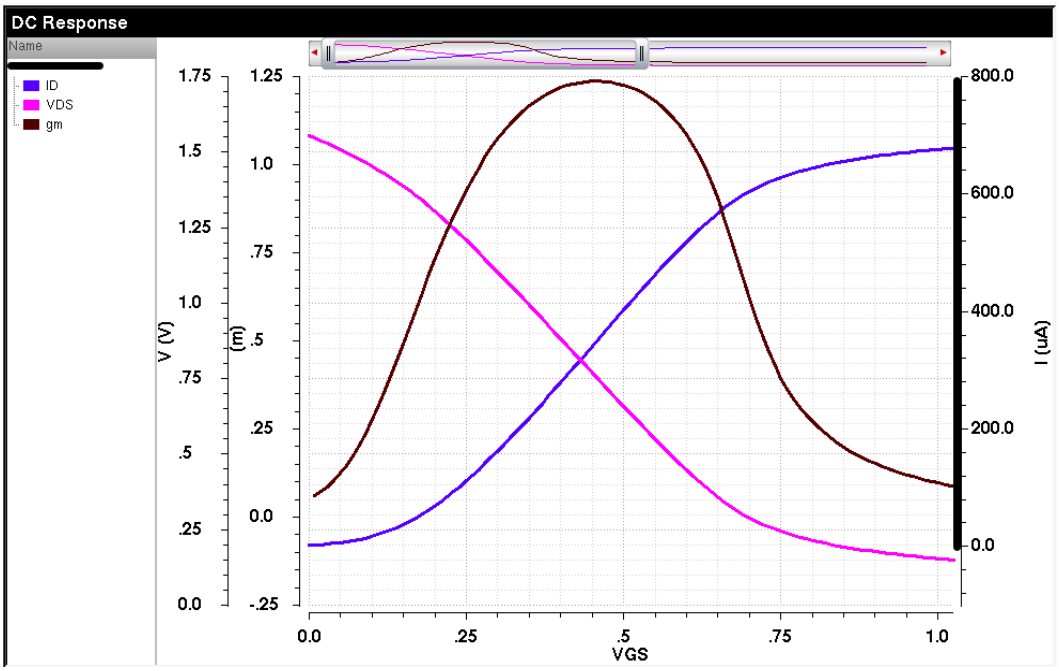
Gain vs Frequency for Vgs = 450 mv



Here, gain = −7.95 dB = 2.497468 at 100 H_Z, this too is very close to the previous result.

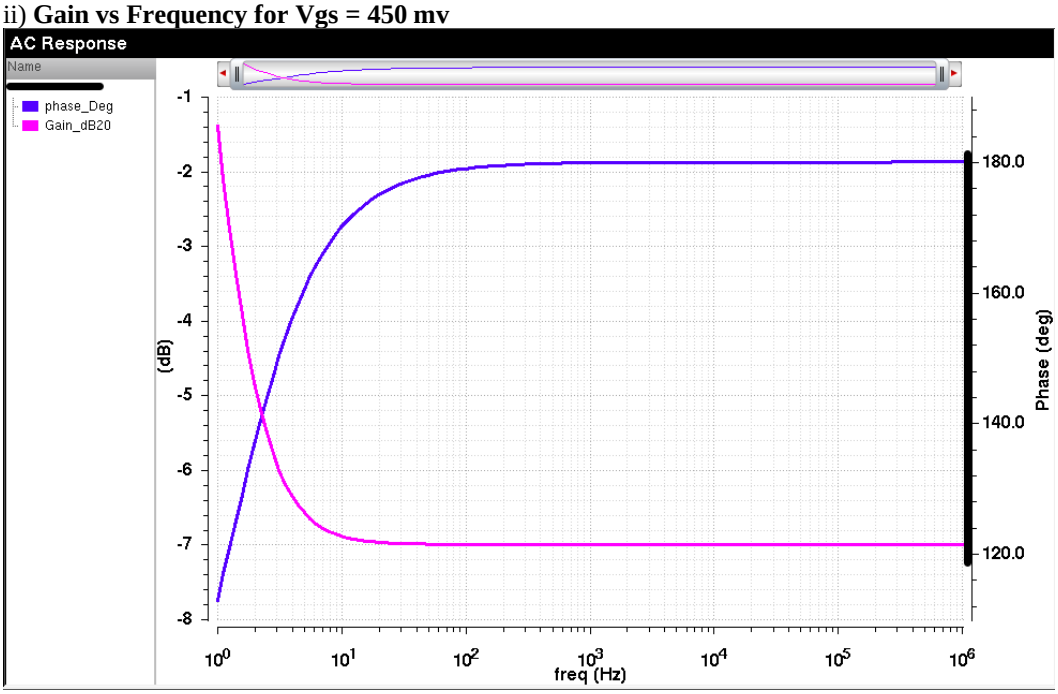
1-2. Common-Source (CS) Stage with Diode connected Load:

i) **Drain current, output voltage and transconductance vs Vgs for V_{DD} = 1.8 V**



Here the maximum gm is found to be around 1.25 m

ii) **Gain vs Frequency for Vgs = 450 mv**



The gain here at 100 Hz is around A_V = -7 dB = -2.24

The gain can be expressed as Av = sqrt $((W_1/L_1) /(W_2/L_2))$
So, we can fabricate the first MOS with a higher width and decrease so for the second MOS to increase the voltage gain. Cautions should be taken to consider the trade-offs of modifying physical dimensions.

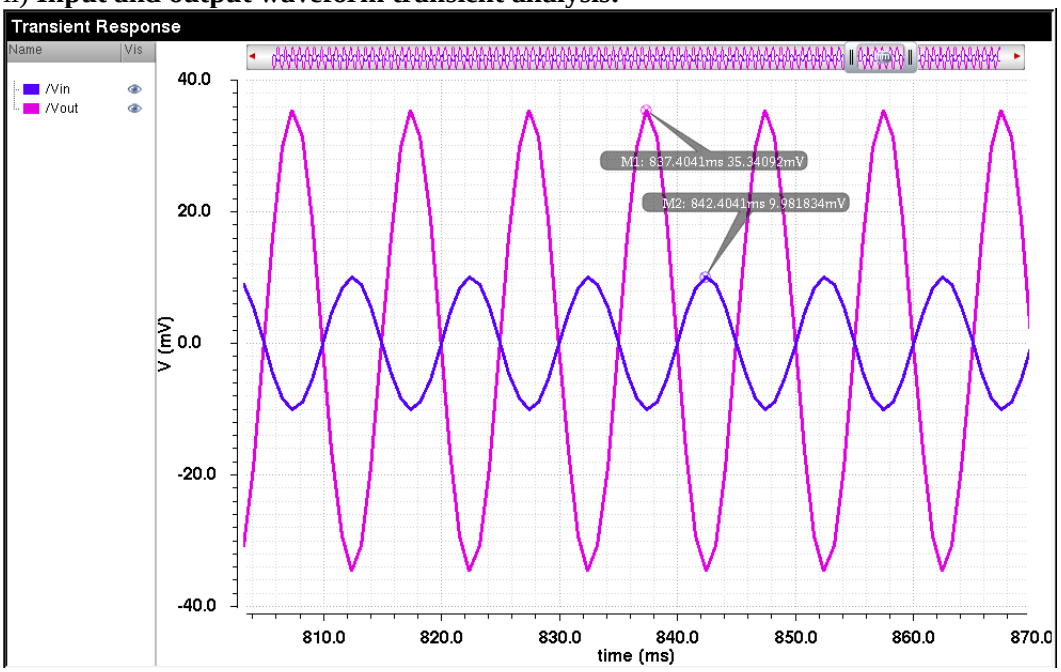
1-3. Common-Source (CS) Stage with Current Source Load:

i) DC bias voltage: 449.992 mV

```
DC Analysis `dcOp'
******************
Important parameter values:
    reltol = 1e-03
    abstol(V) = 1 uV
    abstol(I) = 1 pA
    temp = 27 C
    tnom = 27 C
    tempeffects = all
    gmindc = 1 pS

DC Operating Point:
    V(net02) = 449.992 mV
    V(net2) = 450 mV
    V(net3) = 1.8 V
    V(net4) = 1.8 V
    V(net05) = 503.646 mV
    V(net012) = 1.35 V
    I(V0:p) = -84.7225 pA
    I(V1:p) = 268.054 uA
    I(V2:p) = 0 A
    I(V3:p) = 104.028 pA
    I(VDC:p) = -268.054 uA
    V(Vin) = 0 V
    V(Vout) = 0 V
```

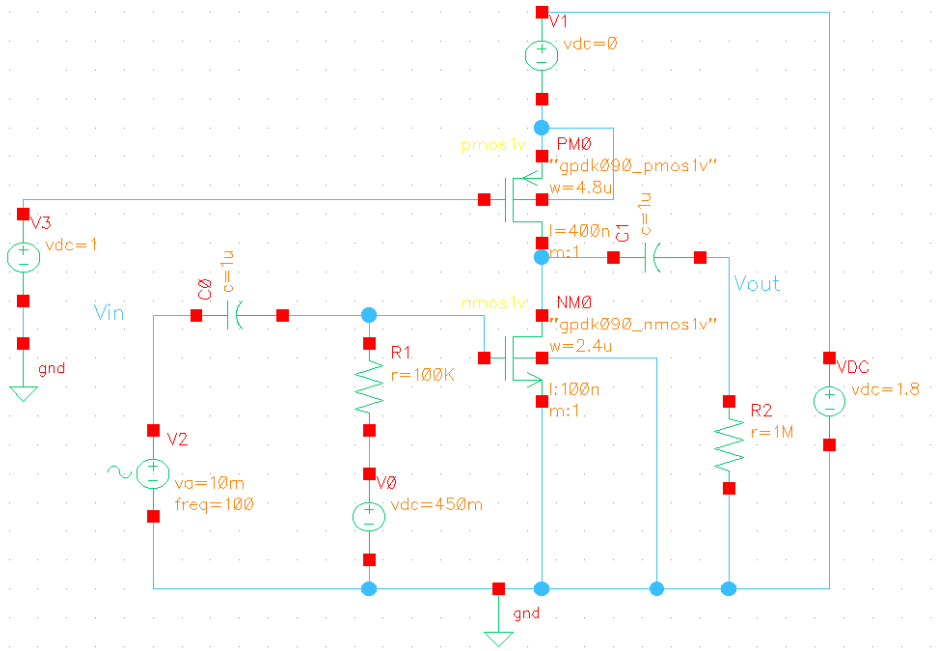
ii) **Input and output waveform transient analysis:**



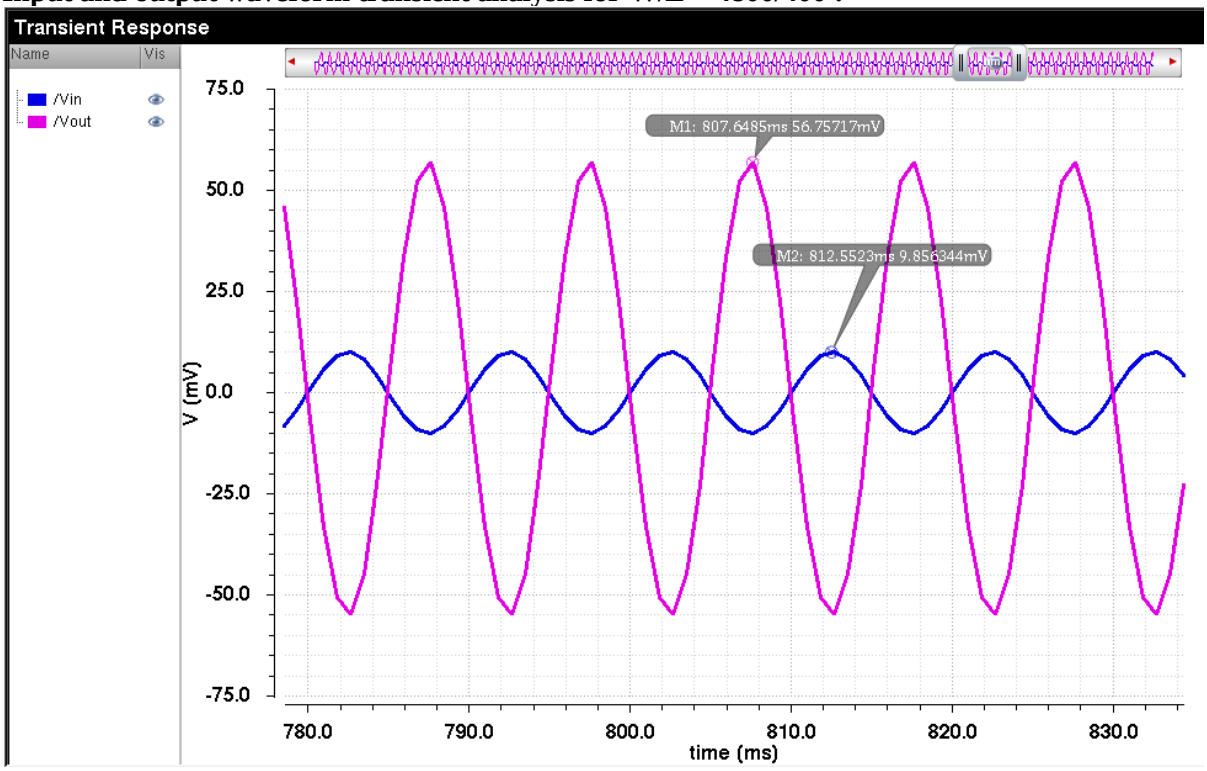
iii) gain = - 35.34 m/9.98 m = - 3.45

iv) The gain formula is $Av = -g_{m1}(r_{O1} \parallel r_{O2})$. So. we can increase the channel lengths to increase either of the resistances to increase overall voltage gain.

v) **Modified schematic:**



Input and output waveform transient analysis for W/L = 4800/400 :



Here gain = - 56.75/ 9.85 = - 5.76. So, the gain has actually increased after the modification of L keeping W constant. However, increasing channel length also increases the overdrive voltage as ΔV α sqrt (L)
So, the PMOS gate bias was lowered to ensure that it operates in the saturation region.

1-4. Common-Source (CS) Stage with Active Load:
i) DC bias voltage 804.195 V

```
DC Operating Point:
    V(NM0:int_d) = 804.195 mV
    V(NM0:int_s) = 721.263 uV
    V(net3) = 1.8 V
    V(net4) = 804.917 mV
    V(net08) = 16.9025 uV
    V(net09) = 870.017 mV
    V(net9) = 1.8 V
    V(PM0:int_d) = 805.638 mV
    V(PM0:int_s) = 1.79928 V
    I(V0:p) = -1.23645 mA
    I(V1:p) = 1.23645 mA
    I(V2:p) = 169.025 pA
    I(V4:p) = 0 A
    V(V_in) = 0 V
    V(V_out) = 0 V
```

We had to increase the gate bias voltage to ensure that $V_{SD}>V_{SG}-V_T$ for PMOS and stays in saturation.

ii) **AC transient analysis:**

iii) The gain here is Av = - 55/10 = - 5.5

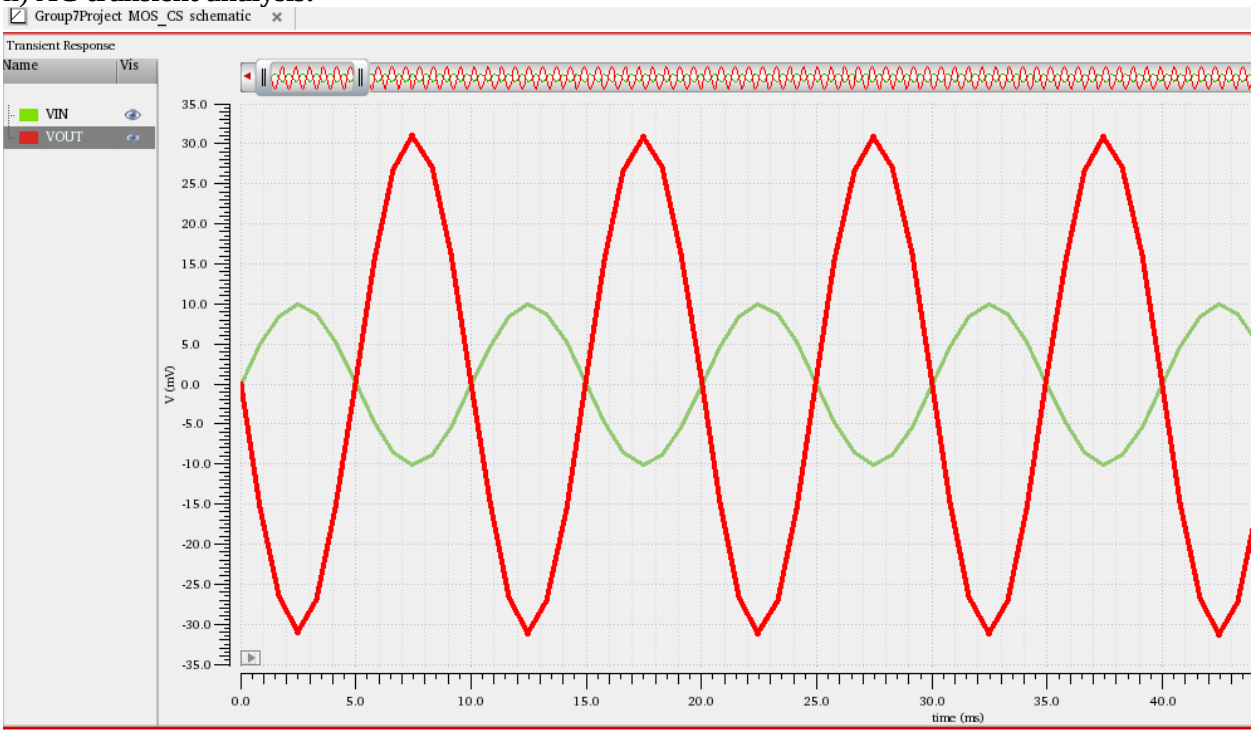
iv) Here the Vgs needs to be varied with careful consideration. Too low Vb will keep pmos in saturation but nmos might enter the triode region. Too high Vb will keep nmos in saturation but might make pmos go into triode. There is only a little bit of swing available for bias voltage depending on the difference between the two threshold voltages of NMOS and PMOS. Thus, this tricky maintenance of the FETs in the saturation region poses some design challenges.

1-5. Common-Source (CS) Stage with Triode Load:

i) DC bias voltage 1.3914 V.

```
DC Operating Point:
    V(NM0:int_d) = 1.3914 V
    V(NM0:int_s) = 304.683 uV
    V(net2) = 449.992 mV
    V(net3) = 1.8 V
    V(net4) = 1.39171 V
    V(net08) = -8.10047 uV
    V(net09) = 1.1 V
    V(net9) = 1.8 V
    V(PM0:int_d) = 1.39201 V
    V(PM0:int_s) = 1.7997 V
    I(V0:p) = -522.358 uA
    I(V1:p) = 522.358 uA
    I(V2:p) = -81.0047 pA
    I(V4:p) = 0 A
    I(V8:p) = 557.46 pA
    V(V_in) = 0 V
    V(V_out) = 0 V
```

ii) **AC transient analysis:**



iii) The gain here is Av = - 31.5/10 = - 3.15

CONCLUSION

All the five topologies had their merits and demerits. We looked at possible alternatives and changes in behavior corresponding to any modification in the circuit. We also tried modifying fabrication of the mos. In all the configurations, the voltage gain was negative indicating an inversion in the output. All these designs are

crucial while designing amplifiers for a system.

REFERENCES

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2. Gray, Paul R., Hurst, Paul J., Lewis, Stephen H, Meyer, Robert G,
Analysis and Design of Analog Integrated Circuits (4th Edition), John Wiley & Sons. Inc.