Lab Report: EEE 466
Group No 15
Lab No 03

LAB TITLE: Layout design and verification of Single Stage amplifier with Cadence Virtuoso Layout Suite L Editor

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ABSTRACT

With a PMOS current source load and a conventional CS amplifier circuit, this experiment taught us how to design a CMOS fabrication layout. Unlike the previous laboratories, we utilized a different tool, the gpdk045, which supports PVS. We used DRC and PVS technologies to ensure that we adhered to standard design guidelines. These resources were essential to utilizing CADENCE Virtuoso Layout Editor to create the layout.

KEYWORDS:

1. gpdk045
2. Layout
3. DRC
4. PVS
5. LVS

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INTRODUCTION

The construction of a CS (Common-Source) amplifier using a PMOS (P-type Metal-Oxide Semiconductor) current source load is the main objective of this report. First, we create a thorough schematic of the CS amplifier.

Next, we carefully consider the circuit's design as we develop the layout. We get closer to finishing the CS amplifier circuit when we combine the layout and schematic into a single, cohesive entity after identifying and correcting any design errors.

THEORY

The gain of a one-stage CS amplifier is equal to $AV = -gm(ro||RD$).
Where ro1 and ro2 are the output impedances.

By changing the channel length, MOSFETs can have their output resistance altered for a given drain current. Put more simply, the channel length (L) and the parameter lambda (λ) are roughly inversely related, meaning that a longer channel length corresponds to a smaller lambda value. Thus, since the combination of routs 1 and 2 determines the gain of the shown stage, we can infer that longer transistors will result in a greater voltage gain.

There are rules pertaining to the minimum width, minimum spacing, minimum enclosure, and minimum extension for different circuit parts when it comes to the layout design phases. The lab instructions provide a handy organization of these rules.

TOOLSUSED

Cadence Virtuoso Software

PROCEDURE

• We started by making a schematic file for the CS amplifier with PMOS current source load.

• Created an empty layout file with the same name.

• Set up the display and editing features in the options menu.

• Followed steps to draw the CS amplifier layers in the layout.

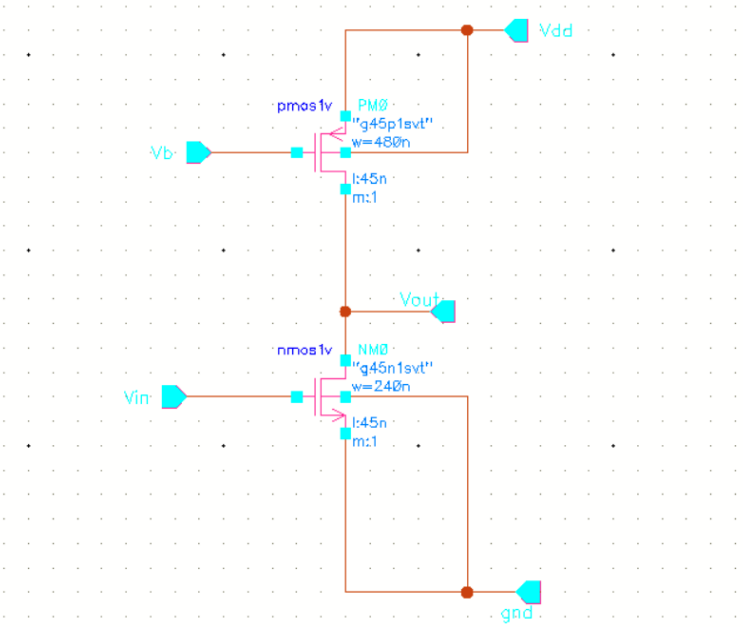
• Added labels for Vdd, gnd, Vin, and Vout.

• Used DRC to check for design errors and fixed them based on the DRC reports.

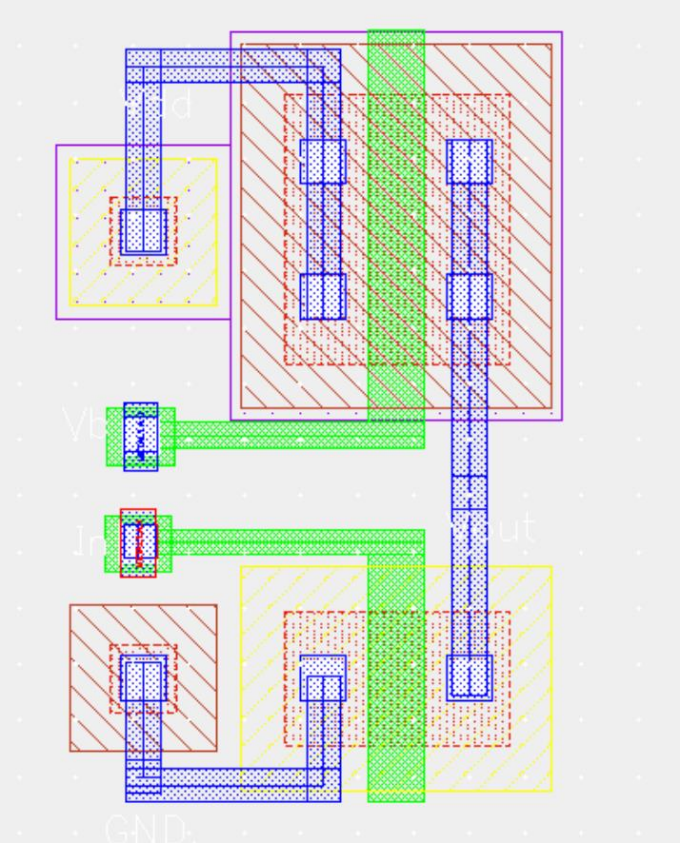
• Employed LVS to ensure the layout matched the logical relations in the schematic file, making corrections where needed.

RESULTS

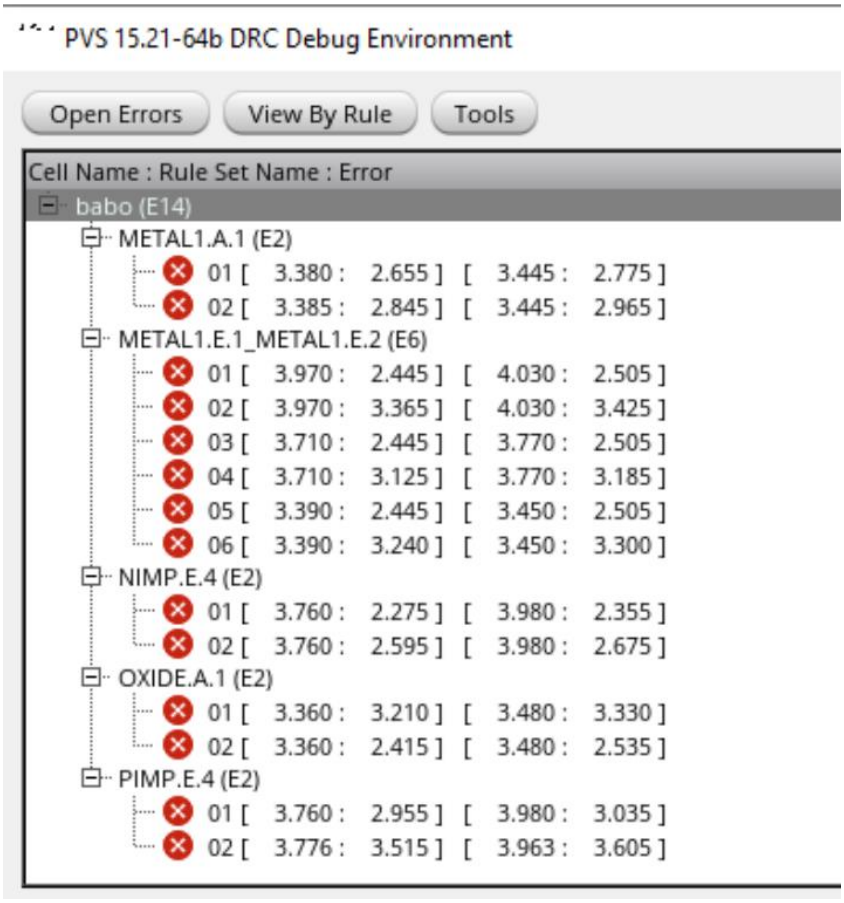
Schematic:



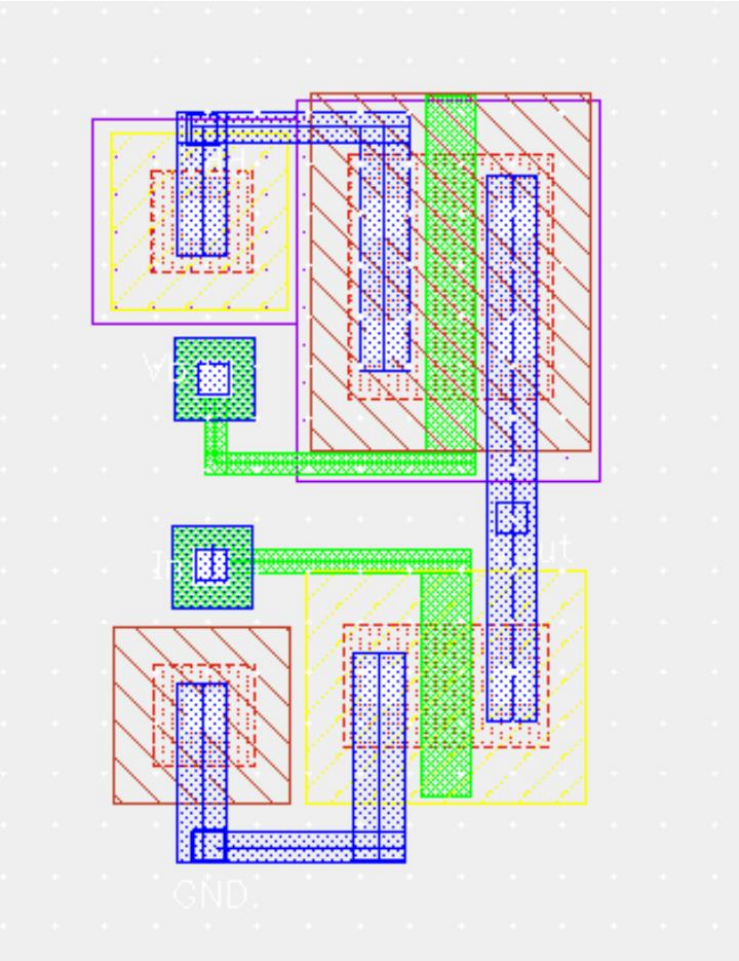
Initial Layout:



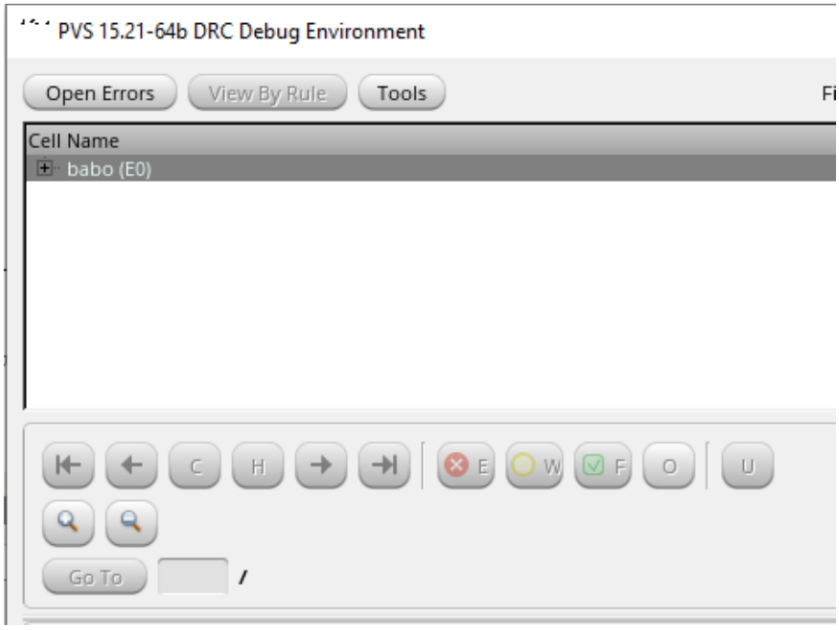
Initial DRC Errors:



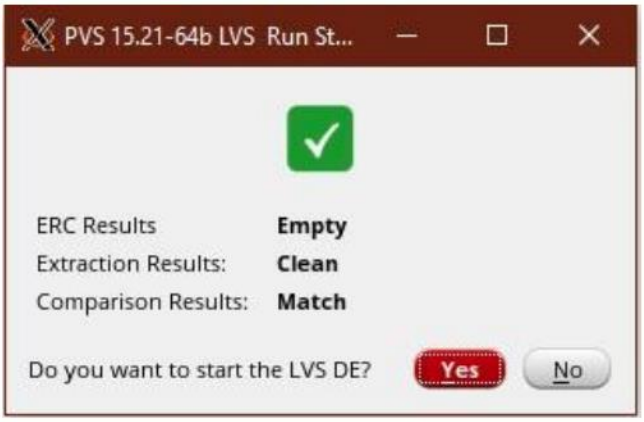
Final Layout:



DRC cleared:



LVS matched:



Report:

Task 1

The layout has been shown.

Task 2

The layout errors that we faced were:

Enclosure Errors: Exposed features suffer shorts, opens, and fabrication risks.

Spacing Errors: Elements too close create shorts, crosstalk, and fabrication risks.

Overlap Errors: Unintended overlaps lead to shorts, leaks, and fabrication challenges.

Width Errors: Narrow lines weaken signals, while wide lines waste space and increase capacitance.

Minimum Area Error: Sometimes if minimum dimension is not met for some elements, it shows error.

Task 3

Before we build the circuit, we need a perfect plan. First, we make sure the wiring diagram (schematic) works flawlessly. Then, we set clear rules for laying out all the pieces (components) and connecting them (routing). Next, we sketch a rough outline (floorplan) considering how signals flow and where power and ground lines will go. Building the circuit takes precision. Snapping to a grid keeps everything lined up. Checking the rules often (DRC) catches mistakes. Using different layers for different parts (metal, polysilicon, diffusion) keeps things organized and clear. Shorter, well-planned connections (routing) improve signal quality. Keeping power and ground lines separate reduces noise and voltage dips. And labeling everything clearly makes future changes easier.

Conclusion:

We started by creating a schematic of a CS amplifier with a PMOS current source load, and then we built the layout while making sure that different layers' design guidelines were followed. We then carried out a Design Rule Check (DRC) to find and address any mistakes. Once all problems were fixed, we used the PVS plugin to do a Layout vs. Schematic (LVS) check to make sure the schematic and layout were in alignment. The comparison findings verified that the layout and schematic exactly matched, and the LVS results showed no faults.

Reference:

Razavi, B. (1999). Design of analog CMOS integrated circuits.
https://cds.cern.ch/record/475329/files/0072380322_TOC.pdf