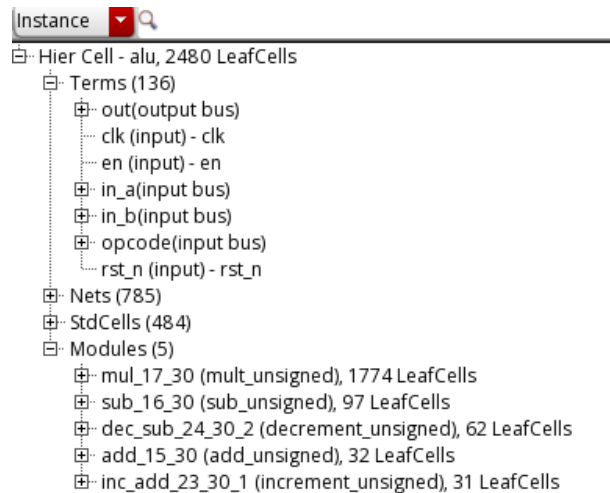


We will be doing physical design for an ALU module with functionalities such as multiplication, subtraction, addition, decrement and increment. We will use an already synthesized Verilog netlist for this. The steps to do the physical design are described as follows

Design import



Floor planning



Defining die boundary:

Specify Floorplan

Basic Advanced

Design Dimensions

Specify By: ☒ Size ☐ Die/IO/Core Coordinates

☐ Core Size by: ☒ Aspect Ratio: Ratio (H/W): 0.98893442

☒ Core Utilization: 0.679473

☐ Cell Utilization: 0.679473

☐ Dimension: Width: 97.6

Height: 96.52

☒ Die Size by: Width: 100.0

Height: 99.94

Core Margins by: ☒ Core to IO Boundary

☐ Core to Die Boundary

Core to Left: 1.2 Core to Top: 1.71

Core to Right: 1.2 Core to Bottom: 1.71

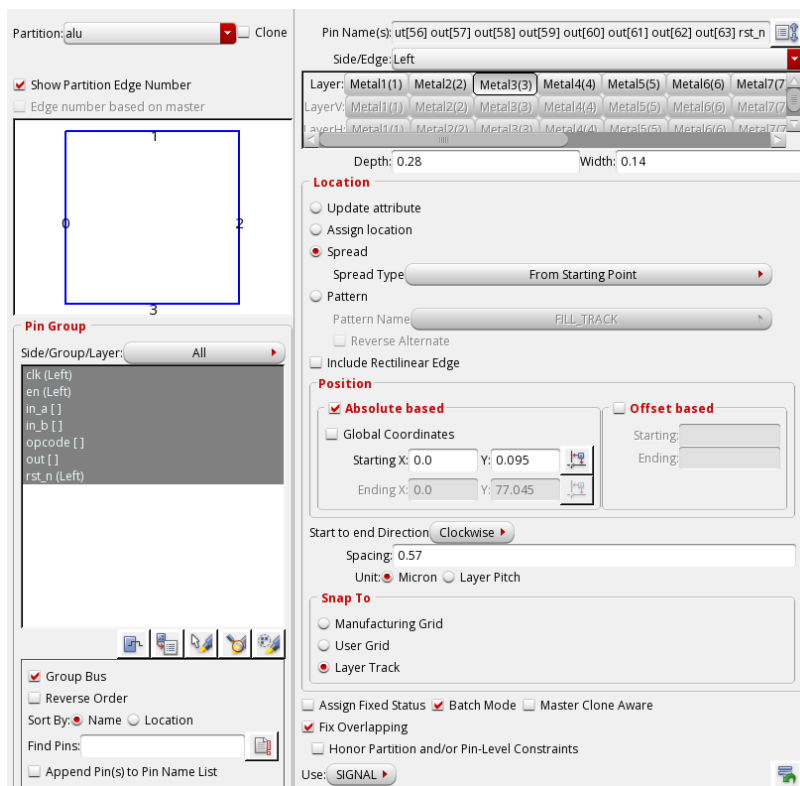
IO Box Calculation Use: ☐ Max IO Height ☒ Min IO Height

Floorplan Origin at: ☒ Lower Left Corner ☐ Center

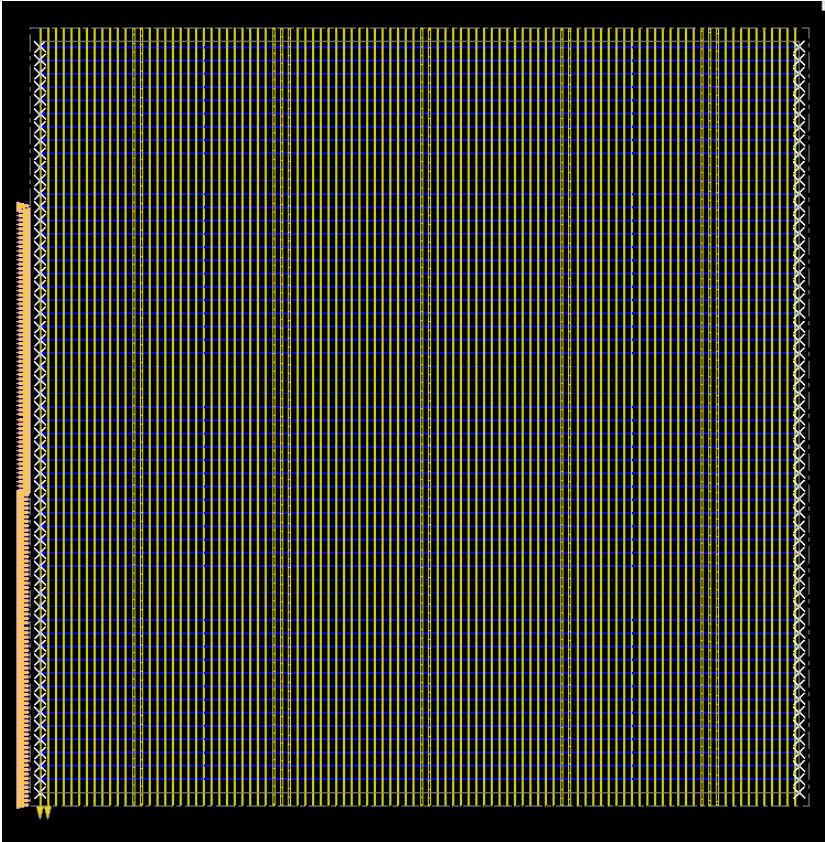
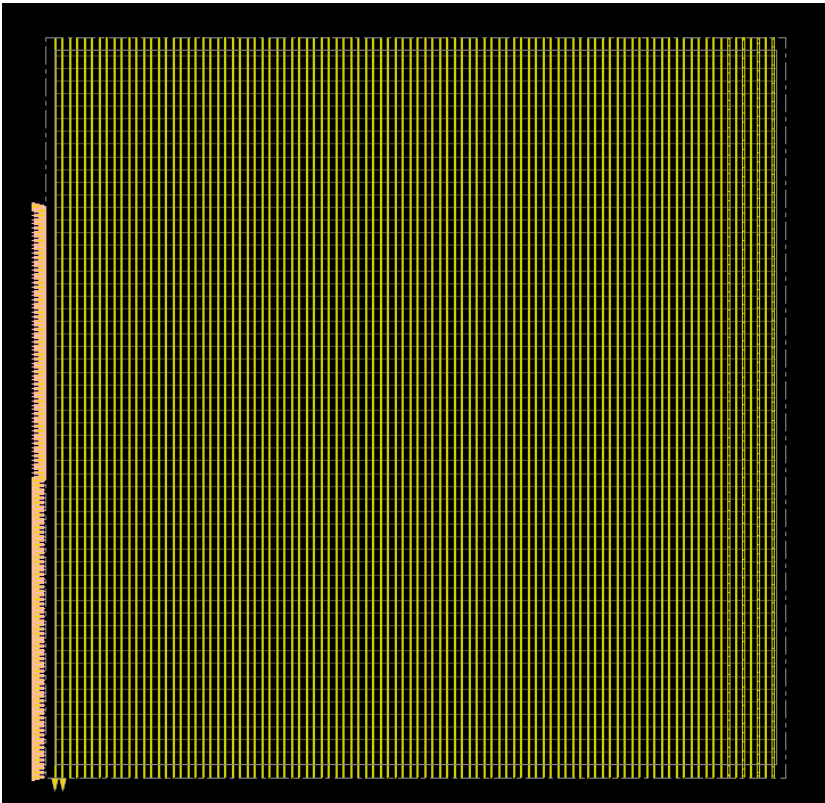
Unit: Micron



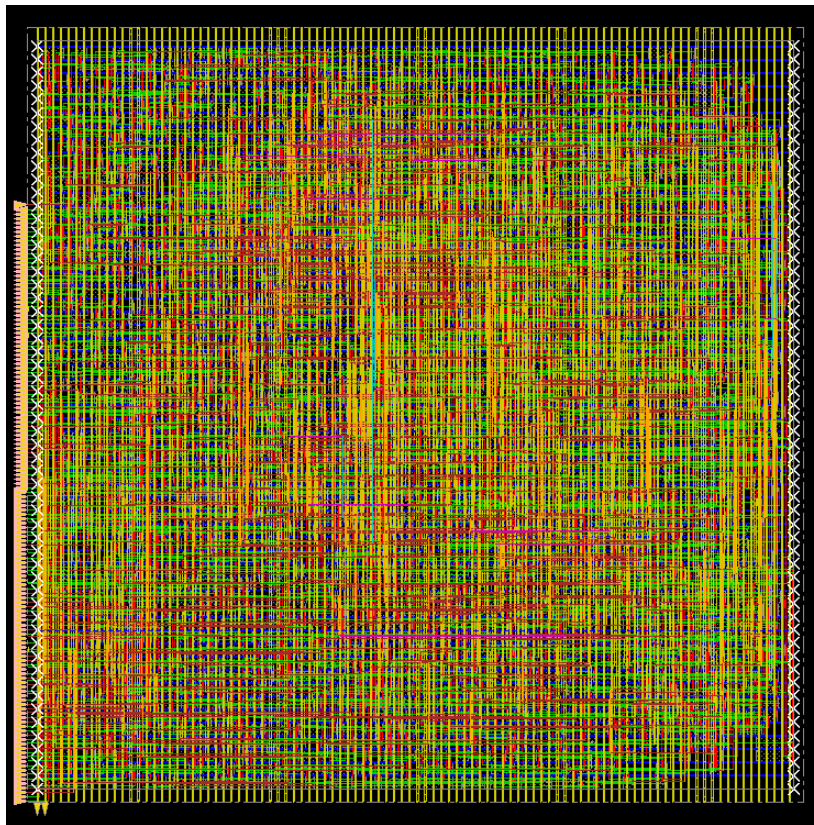
Creating pins



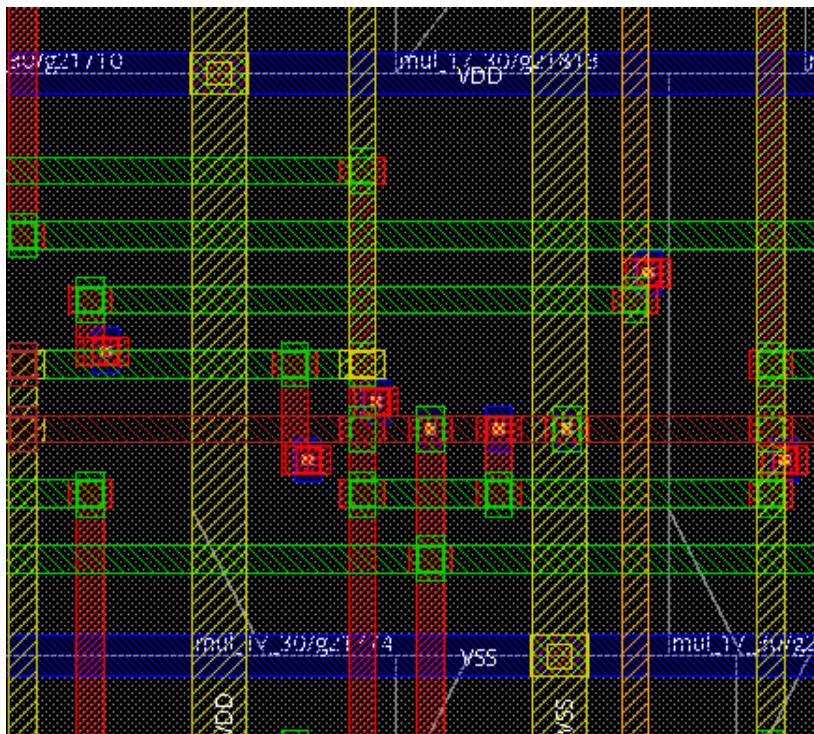
Creating power mesh



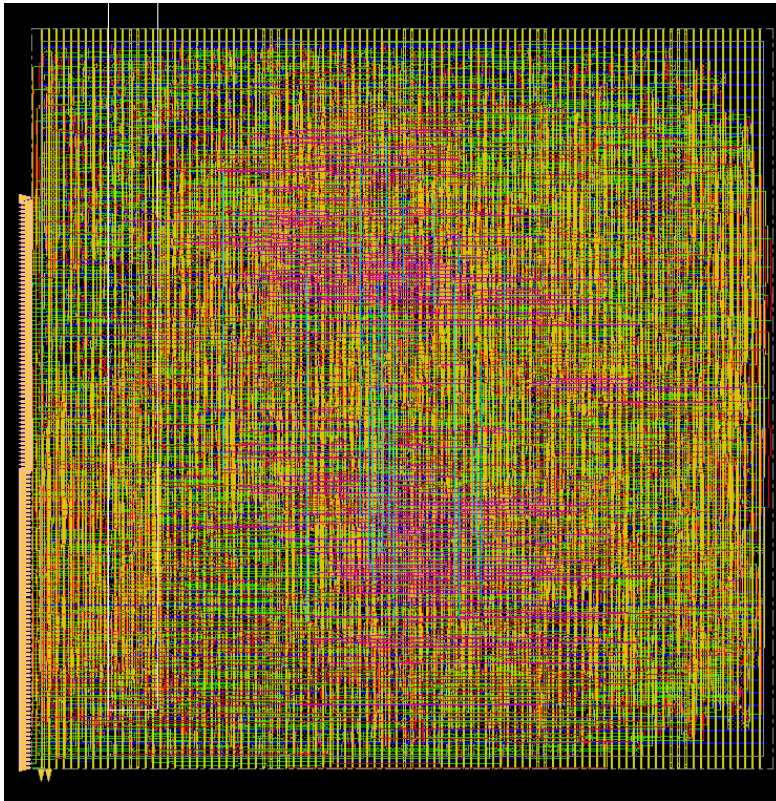
Placement:



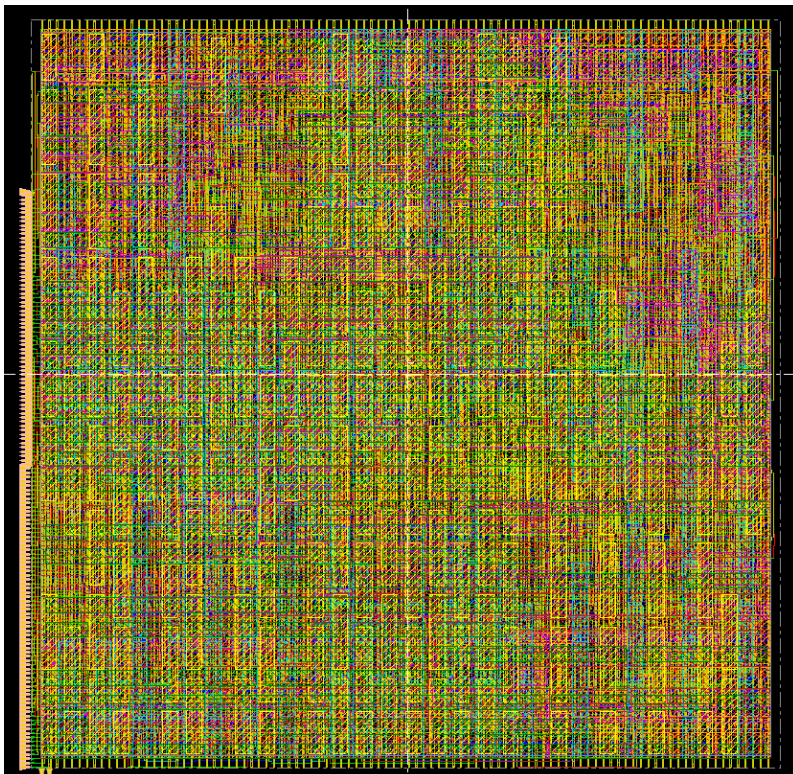
Zoomed view:



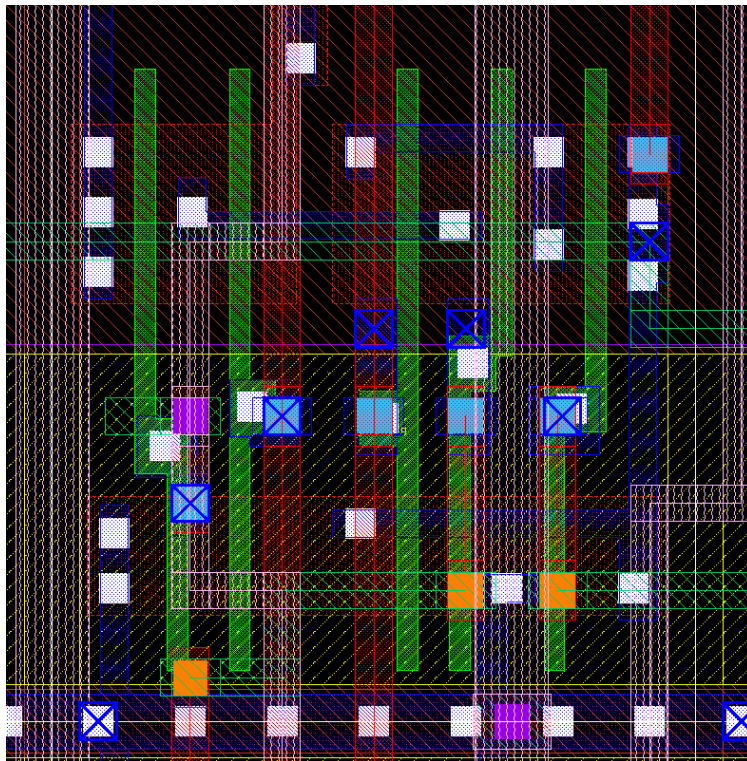
Clock tree synthesis and nano routing



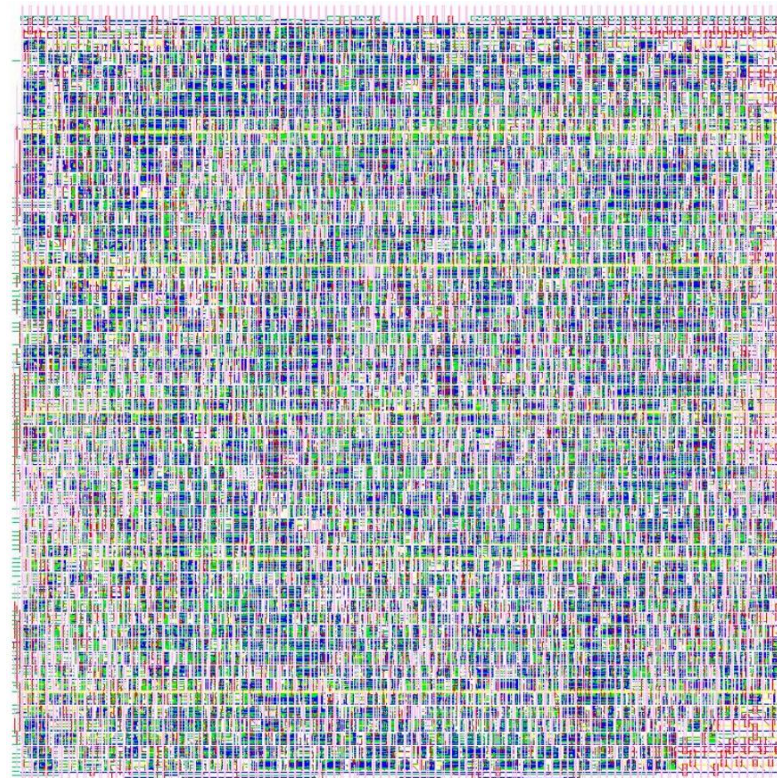
Adding filler cells and metal filling

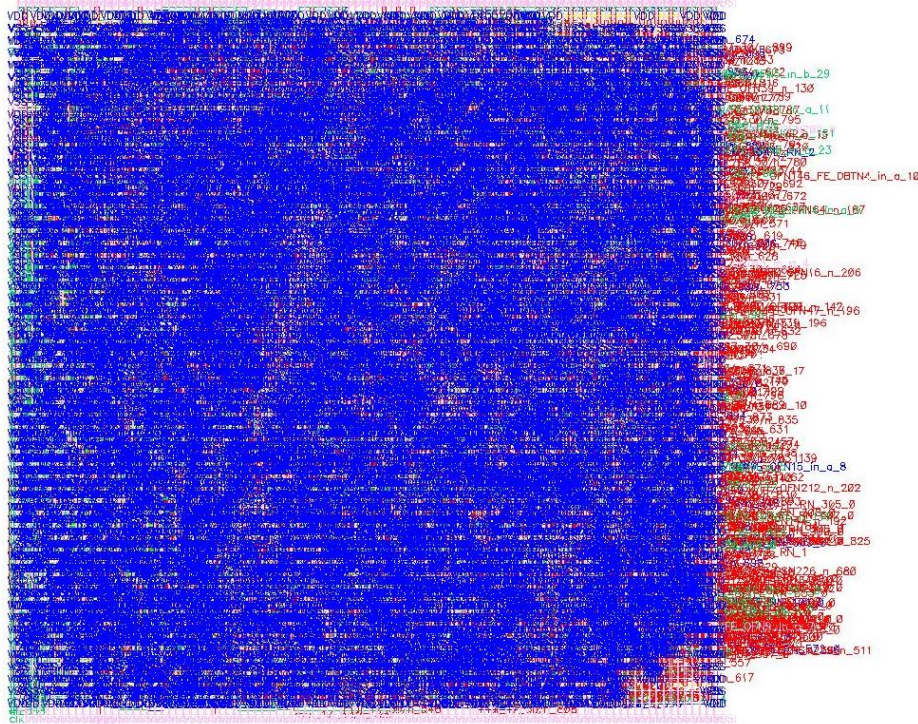


Zoomed view:



Exporting data





DRC error check

Outputting Results ...

#####

ONE LAYER BOOLEAN:	Cumulative Time CPU =	0 (s)	REAL =	0 (s)
TWO LAYER BOOLEAN:	Cumulative Time CPU =	2 (s)	REAL =	3 (s)
POLYGON TOPOLOGICAL:	Cumulative Time CPU =	1 (s)	REAL =	1 (s)
POLYGON MEASUREMENT:	Cumulative Time CPU =	0 (s)	REAL =	0 (s)
SIZE:	Cumulative Time CPU =	2 (s)	REAL =	2 (s)
EDGE TOPOLOGICAL:	Cumulative Time CPU =	1 (s)	REAL =	1 (s)
EDGE MEASUREMENT:	Cumulative Time CPU =	0 (s)	REAL =	0 (s)
STAMP:	Cumulative Time CPU =	0 (s)	REAL =	0 (s)
ONE LAYER DRC:	Cumulative Time CPU =	2 (s)	REAL =	2 (s)
TWO LAYER DRC:	Cumulative Time CPU =	5 (s)	REAL =	5 (s)
NET AREA:	Cumulative Time CPU =	0 (s)	REAL =	0 (s)
DENSITY:	Cumulative Time CPU =	0 (s)	REAL =	0 (s)
MISCELLANEOUS:	Cumulative Time CPU =	2 (s)	REAL =	2 (s)
CONNECT:	Cumulative Time CPU =	0 (s)	REAL =	0 (s)
DEVICE:	Cumulative Time CPU =	0 (s)	REAL =	0 (s)
ERC:	Cumulative Time CPU =	0 (s)	REAL =	0 (s)
PATTERN_MATCH:	Cumulative Time CPU =	0 (s)	REAL =	0 (s)
DFM FILL:	Cumulative Time CPU =	0 (s)	REAL =	0 (s)

Total CPU Time : 16(s)
Total Real Time : 16(s)
Peak Memory Used : 33(M)
Total Original Geometry : 42401(391995)
Total DRC RuleChecks : 562
Total DRC Results : 0 (0)
Summary can be found in file alu.sum
ASCII report database is /home/vlsi05/cds_digital_exp4/alu.drc_errors.ascii
Checking in all SoftShare licenses.

Design Rule Check Finished Normally. Mon Nov 4 15:53:00 2024

Cell Name
B:alu(E0)