Introduction

Analysis

Upon analyzing the problem, these following solutions were thought of.

#	Circuit	Skipping	Problem
1	Combination of asynchronous counter of mod 10, mod 6 and mod 2	Extra glitch pulse when 11 is found	Asynchronous counters have delay issue
2	Combination of synchronous 10,6 and 2 counter	Change with preset and reset	Probable glitch
3		Change by input modification	
4	Combination of 0-59 synchronous and 0-11 synchronous counter	Skipped by truth table	Very complex circuit for 2 seven segments
5	Combination of 1 0-15 skipping and 3 regular 0-15 counter	Skipping in one counter	Requires 32 Flip Flops for only second and minutes

After further analysis, the second and third were found suitable for operation. The second solution was found very easy to implement and the circuitry was comparatively simple. However as this solution requires glitch the third solution was chosen to be implemented.

Implementation

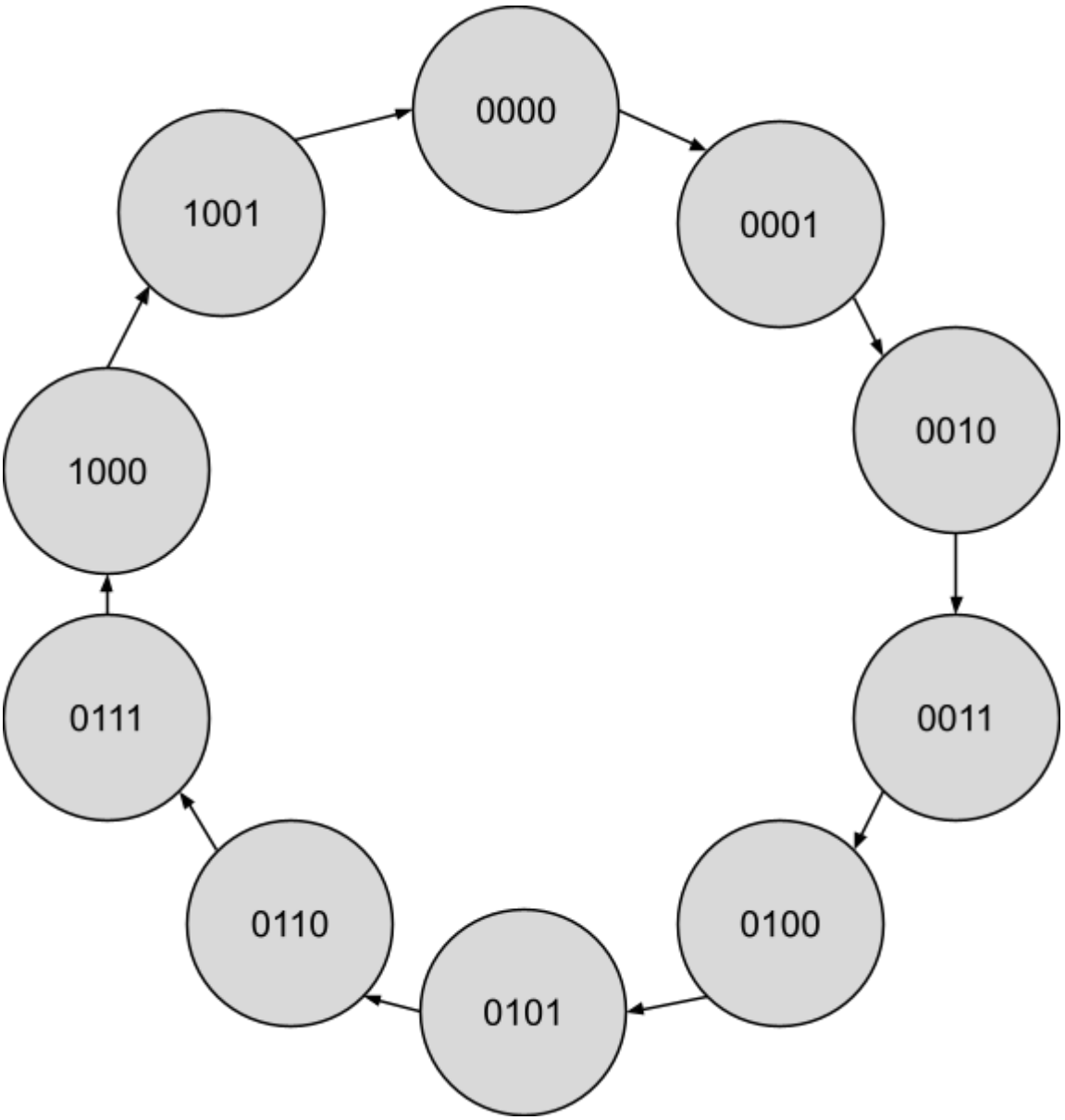
Memory Elements (templates)

T1. A 4 bit counter 0-9
T2. A 3 bit counter 0-5
T3. A 5 bit two output counter (4 bit and one bit) 0-9 and 0-1
T4. A 1 bit AM/PM indicator

Seconds and minutes was implemented with a T1 (for ones) T2 (for tens). For hours the 4 bits was used for ones and the 5th bit was used for tens

The seconds complex received the original clock source and upon completion of seconds a pulse was generated and used as the clock source for the minutes complex. Same is followed from minutes to hour and hour to meridian

0 to 10 Sequential Counter



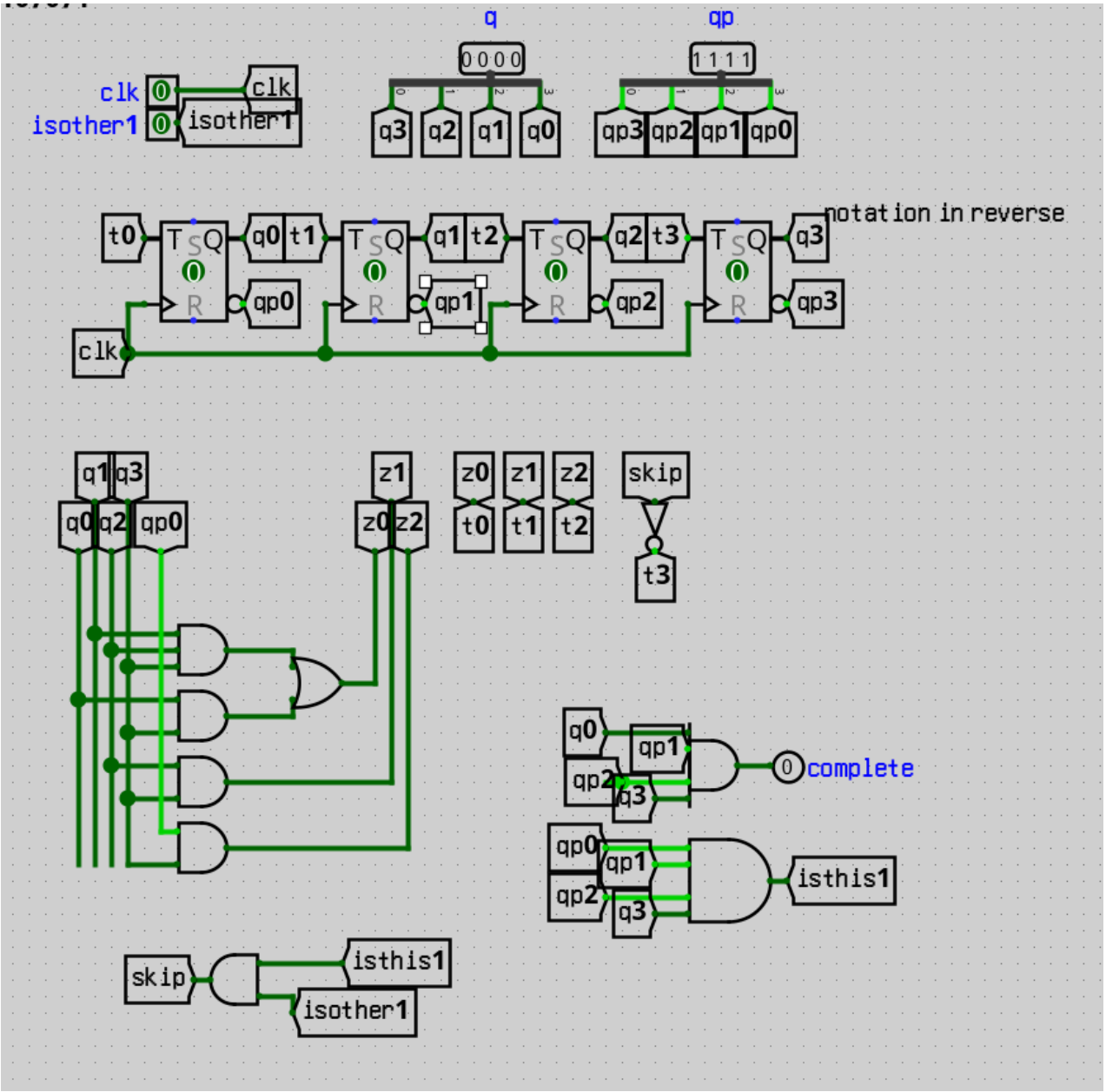
State Table

q_3	q_2	q_1	q_0	q_3^+	q_2^+	q_1^+	q_0^+	t_3	t_2	t_1	t_0
0	0	0	0	0	0	0	1	0	0	0	1
0	0	0	1	0	0	1	0	0	0	1	1
0	0	1	0	0	0	1	1	0	0	0	1
0	0	1	1	0	1	0	0	0	1	1	1
0	1	0	0	0	1	0	1	0	0	0	1
0	1	0	1	0	1	1	0	0	0	1	1
0	1	1	0	0	1	1	1	0	0	0	1
0	1	1	1	1	0	0	0	1	1	1	1
1	0	0	0	1	0	0	1	0	0	0	1
1	0	0	1	0	0	0	0	1	0	0	1
1	0	1	0	-	-	-	-	-	-	-	-
1	0	1	1	-	-	-	-	-	-	-	-
1	1	0	0	-	-	-	-	-	-	-	-
1	1	0	1	-	-	-	-	-	-	-	-
1	1	1	0	-	-	-	-	-	-	-	-
1	1	1	1	-	-	-	-	-	-	-	-

Regular equation

$t_0=1$
$t_1=q_1' \cdot q_o$
$t_2 = q_1 \cdot q_0$
$t_3 = q_2 \cdot q_1 \cdot q_0+q_3 \cdot q_0$

Circuit Diagram (0-9 Counter with skipping)



It's a regular 0-9 counter module with skipping by modifying the inputs.
The circuit takes 2 **inputs**

1. clk
2. isother1

And provides 3 **outputs**

1. Q
2. Q'
3. complete

Here clock is the module clock and the other one is for checking if 1 is on the tens place.

Skipping

Q	T current	T required to switching to $(1101)_2$
1011	0111	0110

So the input LSB needs to be flipped for skipping 2.
As the LSB of T is always 1, the equation for flipping the LSB is:

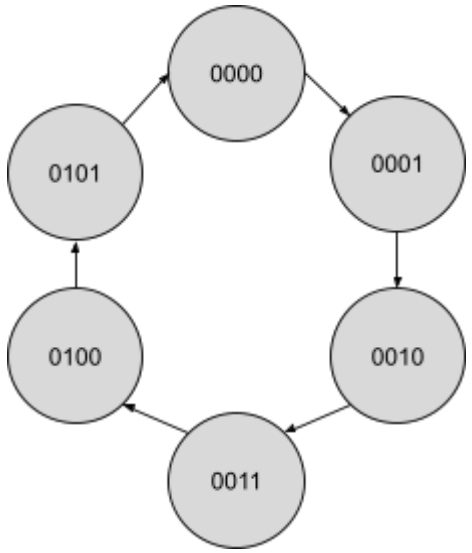
$t_0 = 1 \cdot skip'$

$\Rightarrow t_0 = skip'$

The Skip is produced by having 1 on the tens FF and 1 on the ones. Which are checked by 4 input ands.

0 - 5 Sequential Counter

State Diagram



State Table

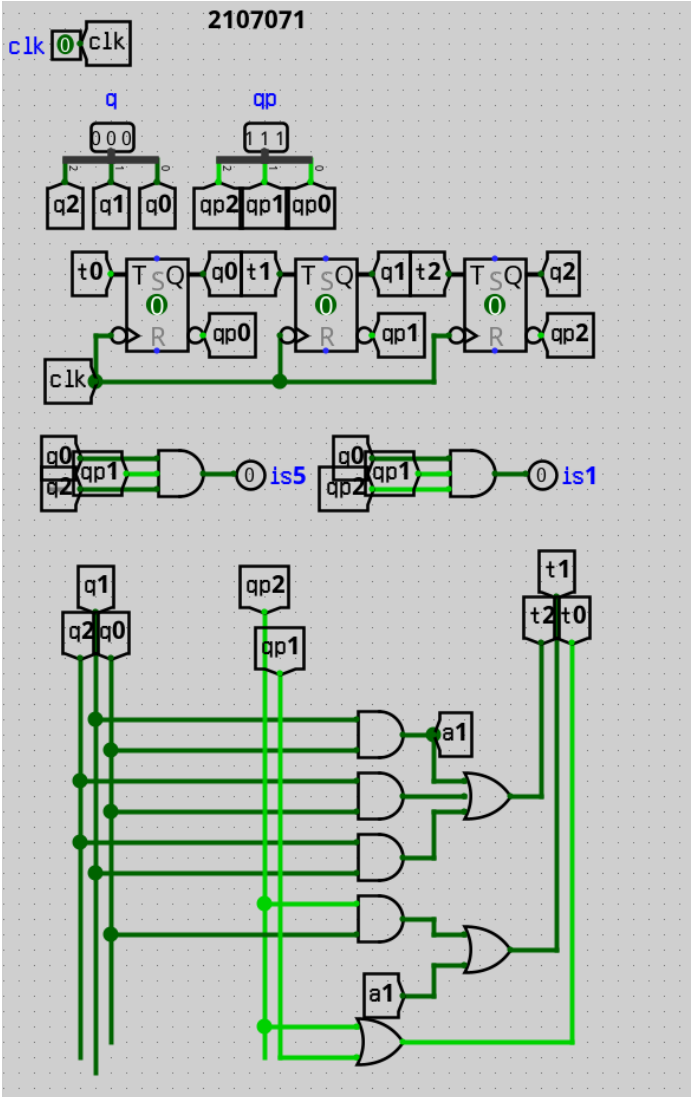
q_2	q_1	q_0	q_2^+	q_1^+	q_0^+	t_2	t_1	t_0
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	1
0	1	0	0	1	1	0	0	1

0	1	1	1	0	0	1	1	1
1	0	0	1	0	1	0	0	1
1	0	1	0	0	0	1	0	1
1	1	0	-	-	-	-	-	-
1	1	1	-	-	-	-	-	-

Equations

$t_0=1$
$t_1=q_1' \cdot q_o$
$t_2 = q_1 \cdot q_0+q_2q_0$

Circuit Diagram



It's a regular negative edge triggered 0-5 counter module with skipping by modifying the inputs.
The circuit takes 1 **input**

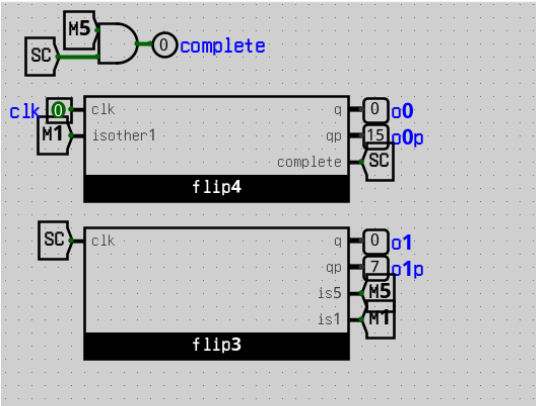
1. clk

And provides 4 **outputs**

1. Q
2. Q'
3. is1 (for skipping)
4. is5 (for complete and next clock)

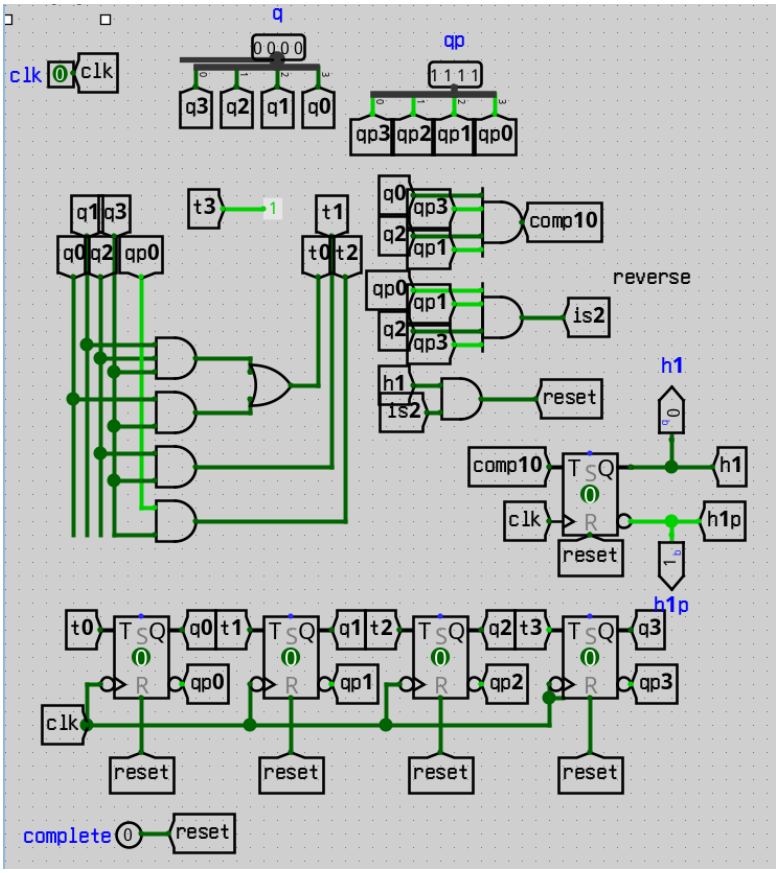
The flip flops are negative edge triggered to ensure that the previous clock source and this block are mutually simultaneous.The checks of specific numbers are made with 3 input and gates

The Block



The block is an arrangement of a 0-9 counter and 0-5 counter. The is1 output from the 0-5 counter is provided as input for the 0-9 counter for skipping 12. This block serves as the storage medium for both seconds and minutes. It produces the next clock signal on 5 on the 0-5 counter and 9 on flip4.

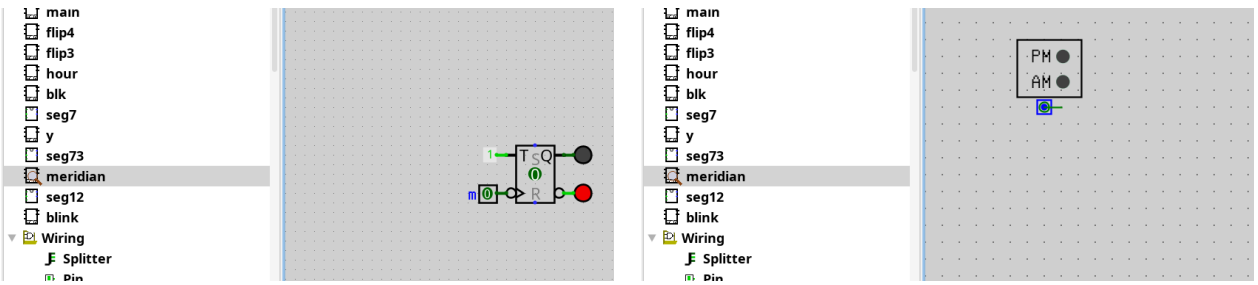
Hour



This circuit holds 4 bit 0-9 data and one bit 0-1 data for displaying hours from 0-12.It's first 4 digits state table is the same as the 4 bit FF's state table. The other flip flop is a normal TFF that triggers on 9 on the first 4 bit flip flop .All 5 Flip Flops are reset on $(0001)_2$ on the first 4 and 1_2 on the last 1.

Meridian

A one bit flip flop that changes on 12 hour completion



BCD to 7 Segment Display decoder

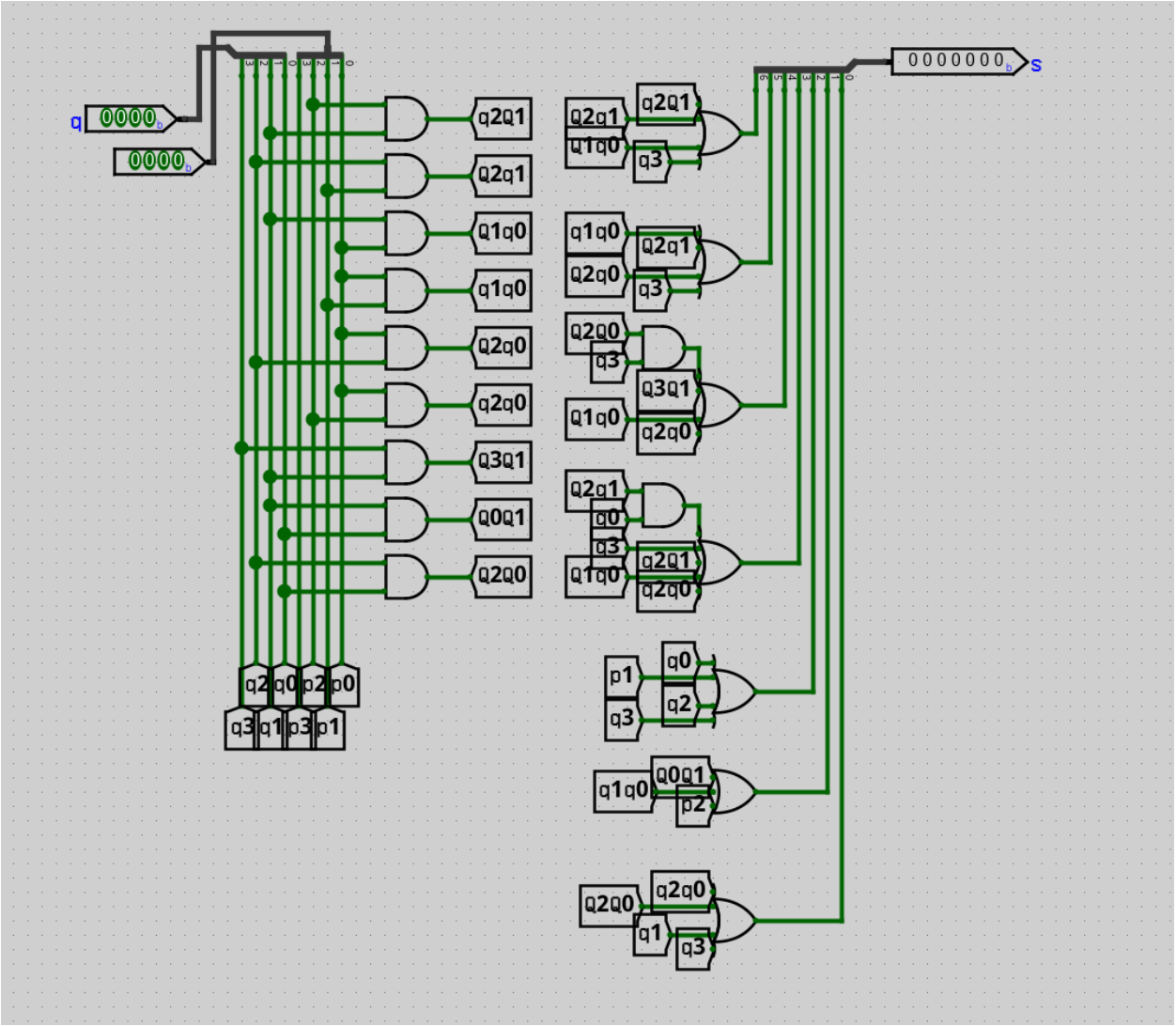
Truth Table

q_3	q_2	q_1	q_0	g	f	e	d	c	b	a
0	0	0	0	0	1	1	1	1	1	1
0	0	0	1	0	0	0	0	1	1	0
0	0	1	0	1	0	1	1	0	1	1
0	0	1	1	1	0	0	1	1	1	1
0	1	0	0	1	1	0	0	1	1	0
0	1	0	1	1	1	0	1	1	0	1
0	1	1	0	1	1	1	1	1	0	1
0	1	1	1	0	0	0	0	1	1	1
1	0	0	0	1	1	1	1	1	1	1
1	0	0	1	1	1	0	1	1	1	1
1	0	1	0	-	-	-	-	-	-	-
1	0	1	1	-	-	-	-	-	-	-
1	1	0	0	-	-	-	-	-	-	-
1	1	0	1	-	-	-	-	-	-	-
1	1	1	0	-	-	-	-	-	-	-
1	1	1	1	-	-	-	-	-	-	-

Equation

$a = q_2' \cdot q_0' + q_1 + q_2 \cdot q_0 + q_3$
$b = q_2' + q_1' \cdot q_0' + q_1 \cdot q_0$
$c = q_1' + q_0 + q_2$
$d = q_2' \cdot q_0' + q_2' \cdot q_1 + q_2 \cdot q_1' \cdot q_0 + q_1 \cdot q_0' + q_3$
$q = q_2' \cdot q_0' + q_1 \cdot q_0'$
$f = q_1' \cdot q_0' + q_2 \cdot q_1' + q_2 \cdot q_0' + q_3$
$g = q_2' \cdot q_1 + q_2 \cdot q_1' + q_3 + q_1 \cdot q_0'$

Circuit Diagram



This circuit takes two 4 bit inputs

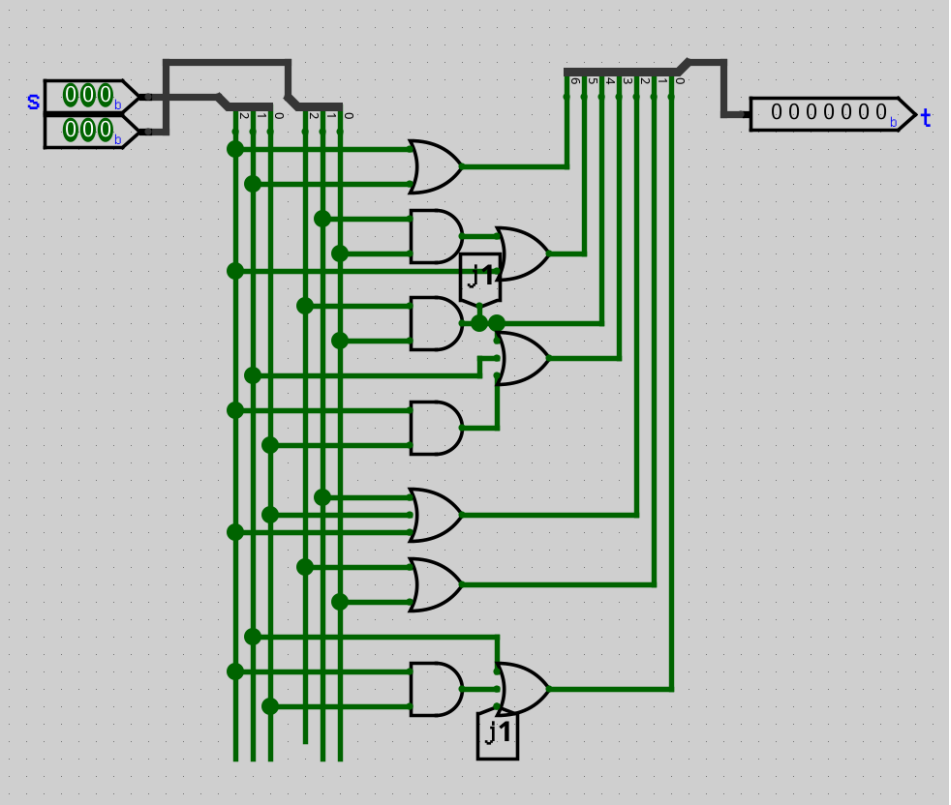
1. $(X)_{BCD}$
2. $(X')_{BCD}$

and decodes it to 7 segment. As the 0-9 counter produces the invert, it is reused here instead of inverting the X again. Tunnels were used to ensure usage of minimum gates.

Base 6 to 7 Segment decoder

Truth Table

q_2	q_1	q_0	g	f	e	d	c	b	a
0	0	0	0	1	1	1	1	1	1
0	0	1	0	0	0	0	1	1	0
0	1	0	1	0	1	1	0	1	1
0	1	1	1	0	0	1	1	1	1
1	0	0	1	1	0	0	1	1	0
1	0	1	1	1	0	1	1	0	1
1	1	0	-	-	-	-	-	-	-
1	1	1	-	-	-	-	-	-	-



Equation

a = $q2' \cdot q0' + q1 + q2 \cdot q0$
b = $q2' + q0'$
c = $q1' + q0$
d = $q2' \cdot q0' + q1 + q2 \cdot q0$
e = $q2' \cdot q0'$
f = $q1' \cdot q0' + q2$
g = $q1 + q2$

Circuit : Base 6 7 Segment decoder

Hour tens - seven segment

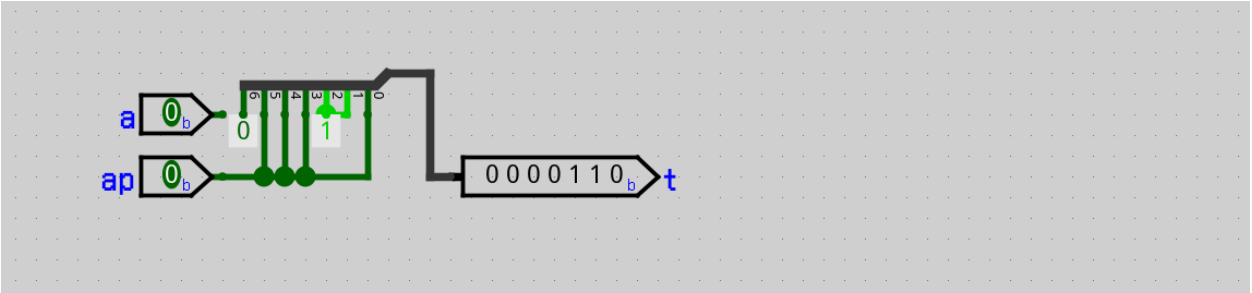
Truth Table

q	g	f	e	d	c	b	a
0	0	1	1	1	1	1	1
1	0	0	0	0	1	1	0

Equation

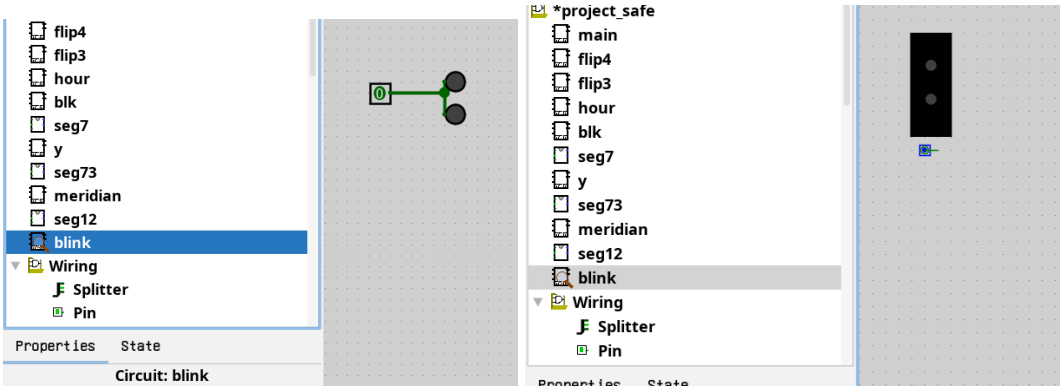
a=q’ b=1 c=1 d=a’ e=a’ f=a’ g=0

Circuit

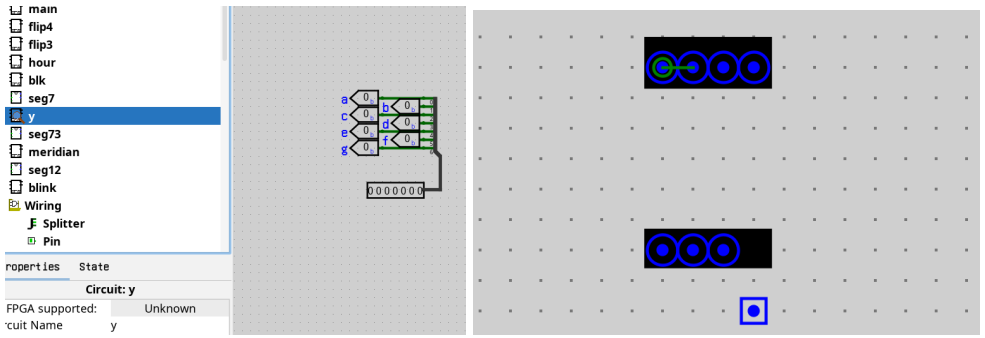


Some Extra Circuit Elements for circuit simplification.

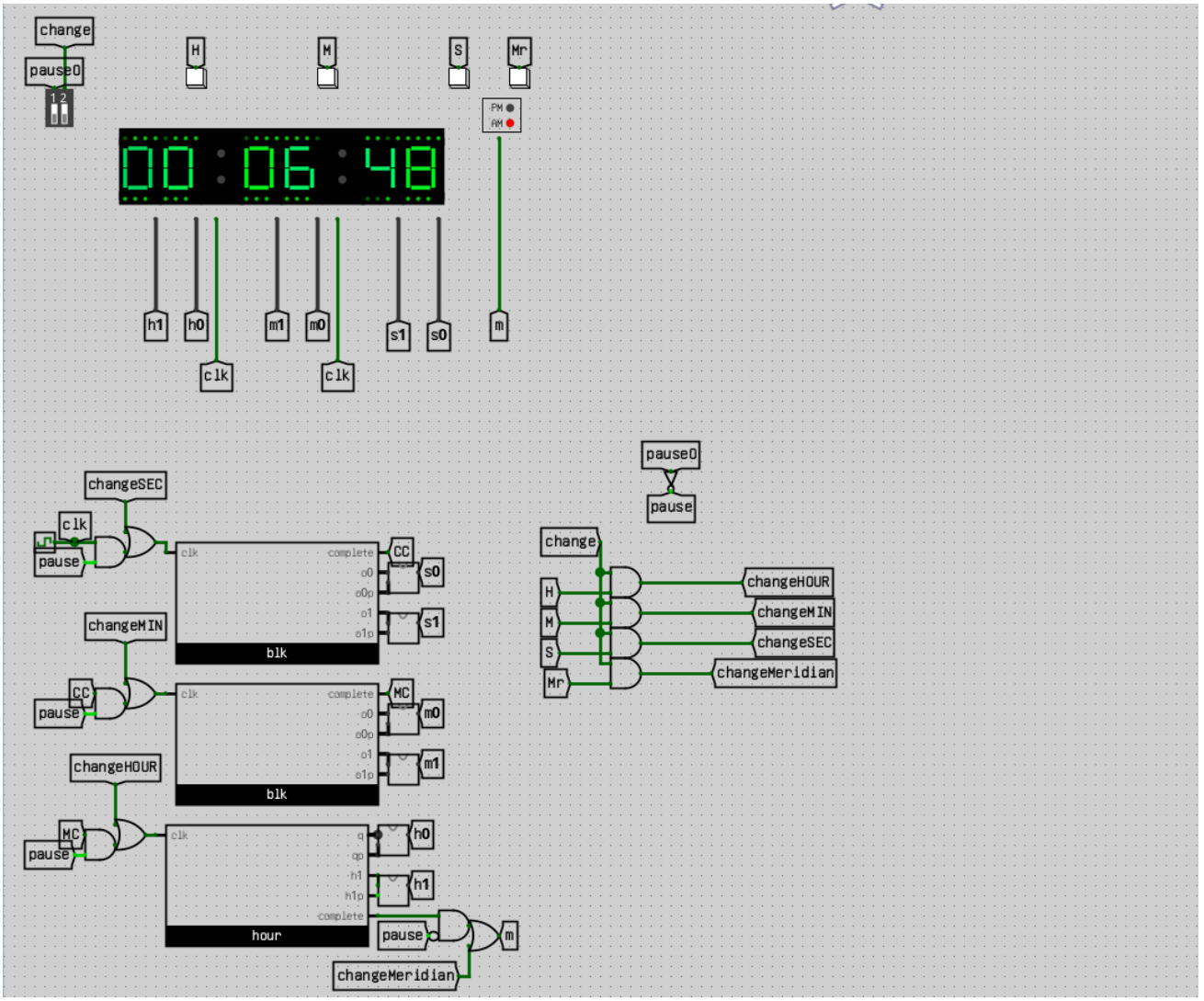
1. Blink



2. 7 Segment Placer



The Merged Circuitry



A 1 Hz clock was added to the circuitry. This clock source was given to the seconds block. The minutes block was clocked from the ‘second’ block's complete output. The Hour was also clocked from the minute's complete output likewise. The same case goes for meridian.

However these clock chaining was not done in a simple manner. But in basic principle it works in the above method. In the above circuit 6 extra inputs manipulates the clock's state (pause,change,H,M,S,Mr)
Here the actual connection for the clock is
clk · pause + trigger
Here the trigger is specific for a specific block.The State changing buttons are enabled using the change trigger, which just and the pressed button with change. The change is simply done by sending a clock pulse to the clock circuit and advancing one state. Linked triggering/ chained triggering is prevented by the pause trigger. The on state of change allows the trigger to pass to the clock.

Discussion

The glitch produced in the hour will not affect the circuit as the required time period for hour pulse is very large. The flip flops in each block forms synchronous counters and the clock passed per block(one block to another) is asynchronous. The 0-9 counter and 0-5 counters are chained keeping the first one positive edge triggered and the next one negative edge triggering to ensure simultaneous change ; the same setup is done between AM/PM and hour.

Usage of tunnels made the circuit easy to debug and work with. The custom IC formats gave the clock setup a better look. Using multibit lines also improved debuggability.

Though there were many ways to accomplish this same task. This method was balanced in case of time, labor and efficiency.

Required Memory Elements

T Flip Flop : 20 (10 7473 IC)

Basic Gates

AND

1. 4 input : 6
2. 3 input : 7
3. 2 input : 59

OR

1. 5 input : 1
2. 4 input : 15
3. 3 input : 9

4. 2 input : 9

NOT Gate :

1. 1 input : 3

Optimized IC Requirements:

1. IC 7421 (3)
2. IC 7411 (3)
3. IC 7408 (15)
4. IC 7402 (1)
5. IC 7432 (3)
6. IC 4075B (3)
7. IC 4072B (8) , one five input used with 7432
8. IC 7476 (10) , JK flip flop forming TFF

Total IC required : 42