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SG2002
Preliminary Datasheet

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revised record

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CONTENTS

Revised records 2
1 Product Overview 8
1.1 Overview 8
1.2 Architecture 9
1.2.1 Overview 9
1.2.2 Processor Cores 9
1.2.3 TPU 10
1.2.4 Video Codec 10
1.2.5 Video Interface (SG2002) 10
1.2.6 ISP and Image Processing 11
1.2.7 CV Hardware Acceleration Engine 11
1.2.8 Audio Codec (SG2002) 12
1.2.9 Network Interface 12
1.2.10 Safety System Module 12
1.2.11 Intelligent and Safe Operating Environment 12
1.2.12 Peripheral Interface (SG2002) 13
1.2.13 External Memory Interface 13
1.2.14 SDK 13
1.2.15 Chip Physical Specifications 14
1.3 Startup and upgrade modes 14
1.3.1 Overview 14
1.3.2 Correspondence between the startup mode and the corresponding signal latch value 14
1.3.3 Mirror Burn Mode 14
1.3.4 Secure Start 15
1.4 Address Space Mapping 16
2 Hardware Characteristics 20
2.1 Packages and Pinouts 20
2.1.1 Package SG2002 ..... SG2002
2.1.2 Pinouts SG2002 ..... SG2002
2.2 Pin Information Description 22
2.3 Welding process recommendations 23
2.4 Chiu Min Parameters 24
2.4.1 Moisture-proof packaging for Calculus products 24
2.5 Electrical Performance Parameters 27
2.5.1 Power consumption parameters 27
2.5.2 Temperature and thermal resistance parameters (SG2002) 27
2.5.3 Destructive voltage 28

2.5.4 Upper and Lower Power Sequence (SG2002) 28

2.5.5 Power supply DC/AC Electrical parameters 31
2.5.6 1.8V IO Electrical Parameters 33
2.5.7 18OD33 IO (VDDIO=1.8V) Electrical Parameters 33
2.5.8 18OD33 IO (VDDIO=3.0V) Electrical Parameters 34
2.5.9 Audio GPIO Electrical Parameters 36
2.5.10 ETH GPIO Electrical Parameters 36
2.5.11 MIPI Rx Electrical Specifications 36
2.5.12 Sub-LVDS Electrical Parameters 38
2.5.13 HiSPi Electrical Parameters 38
2.5.14 MIPI /LVDS Tx Electrical Parameters 39
2.5.15 SDIO Electrical Parameters 40
2.5.16 VI RAW/BT.601/BT.656/BT.1120 Electrical Parameters 40
2.5.17 Electrical parameters BT.601/BT.656/8080 in VO (Video out) 41
2.5.18 AUDIO CODEC Electrical Parameters 41
2.6 Interface Timing 42
2.6.1 SPI NOR Interface Timing 42
2.6.2 SPI NAND Interface Timing 43
2.6.3 VI Interface Timing 45
2.6.4 VO Interface Timing 45
2.6.5 AIAO (I2S/PCM) Interface Timing 47
2.6.6 I2C Interface Timing 49
2.6.7 SPI Interface Timing 50
2.6.8 MIPI Rx Interface Timing 51
2.6.9 Sub-LVDS Interface Timing 52
2.6.10 HiSPi Interface Timing 53
2.6.11 MIPI Tx Interface Timing 54
2.6.12 SDIO/MMC Interface Timing 56

Table of Contents

Figure 1-1 SG2002 Architecture Diagram 9
Figure 2-1 SG2002 Package Dimensions, Top View 20
Figure 2-2. SG2002 Package Dimensions, Bottom View 21
Figure 2-3 SG2002 Pinouts 22
Figure 2-4 Lead-Free Reflow Process Curves 23
Figure 2-5 Vacuum Drying Packaging Information 24
Figure 2-6 Dry Pack, Humidity Card, Chip and Tray Tray 25
Figure 2-7 SPI NOR Interface Timing Chart 42
Figure 2-8 SPI NAND Input Direction Timing Chart 43
Figure 2-9 SPI NAND Output Direction Timing Chart 43
Figure 2-10 VI Interface Timing Diagram 45
Figure 2-11 VO Interface Timing Diagram 45
Figure 2-12 BT.656 Interface Timing Diagrams 46
Figure 2-13 BT.601 Interface Timing Chart 46
Figure 2-14 BT.1120 Interface Timing Diagram 46
Figure 2-15 8080 Interface Timing Diagram 47
Figure 2-16 I2S & PCM Interface Receive Timing Chart 47
Figure 2-17 I2S & PCM Interface Transmit Timing Chart 48
Figure 2-18 I2C Interface Timing Diagram 49
Figure 2-19 SPI Interface Timing Diagram 50
Figure 2-20. Clock Data Timing Diagram for MIPI Rx at 0.08Gbps ≤ Data Speed ≤ 1.5Gbps 51
Sub-LVDS Clock Data Timing Chart 52
Figure 2-22. HiSPi Clock Data Timing Chart 53
Figure 2-23 MIPI TX Interface Data Pair Clock Timing Chart 54
Figure 2-24 TX EYE Diagram Specification 55
Figure 2-25 Transmitter Eye Diagram Validation Setup 55
Figure 2-26 Data Input/Output Timing Diagram for SDIO/MMC Single Edge (SDR) 56
Figure 2-27 Timing Diagram of Data Input/Output Direction for SDIO/MMC Dual Edge DDR50 Mode 57
Figure 2-28 Data Command Output Direction Timing Diagram for SDIO/MMC HS200 and SDR104 Modes 58

Table of Contents

Table 2-1 Lead-Free Reflow Solderer Cover Parameters 23
Table 2-2 Humidity Classification and Storage Time (Floor Life) 25
Table 2-3 Baking Temperature and Schedule 26
Table 2-4 SG2002 Thermal Resistance Parameters 27
Table 2-5 Temperature-Related Parameters 27
Table 2-6 Destructive Voltage Parameters (SG2002) 28
Table 2-7 SG2002 Power Supply Electrical Parameters (Recommended Operating Conditions) 31
Table 2-8 1.8V IO Electrical Parameters 33
Table 2-9 18OD33 IO (VDDIO=1.8V) Electrical Parameters 33
Table 2-10 18OD33 IO (VDDIO=3.0V) Electrical Parameters 34
Table 2-11 Audio GPIO Electrical Parameters 36
Table 2-12 ETH GPIO Electrical Parameters 36
MIPI D-PHY High Speed (MISH) Differential DC Electrical Parameters 37
MIPI D-PHY High Speed (MIHS) Differential AC Electrical Parameters 37
Table 2-15 MIPI D-PHY Low Power (MILP) Differential DC Electrical Parameters 37
Table 2-16 MIPI D-PHY Low Power (MILP) Differential AC Electrical Parameters 38
Table 2-17 Sub-LVDS(SL) Differential DC Electrical Parameters 38
Table 2-18 Sub-LVDS(SL) Differential AC Electrical Parameters 38
Table 2-19 HiSPi Differential DC Electrical Parameters 38
Table 2-20 HiSPi Differential AC Electrical Parameters 39
Table 2-21 MIPI HS Transmitter DC Specifications 39
Table 2-22 MIPI HS Transmitter AC Specifications 39
Table 2-23 MIPI LP Transmitter DC Specifications 39
Form 2-24 MIPI LP Transmitter AC Specifications 40mm
Table 2-25 LVDS Transmitter DC/AC Specifications 40mm
Table 2-26 Audio CODEC Overall Indicator Table 41
Table 2-27 Audio DAC Electrical Parameters 41
Table 2-28 Audio ADC Electrical Parameters 41
Table 2-29 SPI_NOR Interface Timing Parameter Table 42
Table 2-30 SPI NAND Input Direction Timing 43
Table 2-31 SPI NAND Output Direction Timing 43
Table 2-32 VI Interface Timing Parameter Table 45
Table 2-33 VO Interface Timing Parameter Table 46
Table 2-34 I2S/PCM Interface Timing Parameter Table 48
Table 2-35 I2C Interface Timing Parameter Table 49
Table 2-36 SPI Interface Timing Parameter Table 50
Table 2-37 Timing Parameters for MIPI Rx at 0.08Gbps≤1.5Gbps Data Speed 51
Sub-LVDS Timing Parameters Table 2-38. 52
HiSPi Timing Parameters Table 2-39. 53

Form 2-40 Data-Clock Timing Specifications for ≧ 0.08Gbps and ≦ 1 Gbps..... 54

Table 2-41 Data-Clock Timing Specifications for > 1Gbps and ≦ 1.5 Gbps 54
Form 2-42 Data-Clock Timing Specifications for > 1.5Gbps and ≦ 2.5 Gbps 54
Table 2-43 Transmitter Eye Diagram Specification..... 55
Table 2-44 SDIO/MMC Single Edge DS (default speed) Mode Timing Parameter Table 56
Table 2-45 SDIO/MMC Single Edge HS (High speed) Mode Timing Parameter Table 57
Table 2-46 SDIO/MMC Double Edge DDR50 Mode Timing Parameter Table..... 58
Table 2-47 SDIO/MMC HS200 and SDR104 Mode Output Parameter Table 2-47 SDIO/MMC HS200 and SDR104 Mode Output Parameters
Table 2-48 SDIO/MMC HS200 and SDR104 Mode Input Timing Parameter Table ... 59

1 Product Overview

1.1 summarize

SG2002 is a high-performance, low-power chip for edge intelligent surveillance IP cameras, smart cat-eye door locks, visual doorbells, home intelligence and other product areas, integrated with H.264 video compression codec, H.265 video compression encoder and ISP; support for HDR Wide Dynamic, 3D noise reduction, demisting, lens aberration correction and other image enhancement and correction algorithms, providing customers with professional-grade video image quality. customers with professional-grade video image quality.

The chip also integrates a self-developed TPU that delivers 1.0TOPS of arithmetic power at 8-bit integer operations. The specially designed TPU scheduling engine efficiently provides extremely high bandwidth data streams to all tensor processor cores. Powerful deep learning model compilers and software SDKs are also available for users. Mainstream deep learning frameworks, such as Caffe and Tensorflow, can be easily ported to its platform.

In addition, it also provides secure boot, secure update, secure encryption, etc. It provides a series of security solutions for users from development, mass production, and product application.

An 8-bit MCU subsystem is integrated into the chip, which can replace the external MCU to save BOM cost and power consumption.

1.2 build

1.2.1 summarize

Figure *1-1 SG2002* Block Diagram

1.2.2 processor core

- Main Processor RISCV C906 @ 1.0Ghz .
  - 32KB I-cache, 64KB D-Cache
  - Integrated Vector and Floating Point Unit (FPU) .
- Main Processor ARM Cortex-A53 @ 1.0GHz
  - 32KB I-cache, 32KB D-Cache
  - 128KB L2 cache
  - Neon and floating-point FPU support
- □o-processor RISCV C906 @ 700Mhz
  - Integrated Floating Point Unit (FPU) .

The main processor RISCV C906 @ 1.0Ghz and the main processor ARM Cortex-A53 @ 1.0Ghz can be used via the pins

GPIO_RTX EPHY_RTX is switched and the switching logic is:

Low ------ ARM Cortex-A53 @ 1.0GHz
High ----- RISCV C906 @ 1.0Ghz

1.2.3 TPU

- Built-in TPU with ~1.0TOPS INT8
- Support for mainstream neural network architectures: Caffe, Pytorch, TensorFlow(Lite), ONNX and MXNet
- Realizes Pedestrian Detection, Face Detection, Face recognition, Face anti-spoofing and other video structuring applications.

1.2.4 Video Codec

- H.264 Baseline/Main/High profile
- H.265 Main profile
- H.264/H.265 supports both I-frame and P-frame.
- MJPEG/JPEG baseline
- H.264 codec maximum resolution : 2880x1620 (5M)
- H.265 encoding max resolution : 2880x1620 (5M)
- H.264 codec performance
  - 2880x1620@30fps+720x576@30fps
  - 1920x1080@30fps Encoding + 1920x1080@30fps Decoding
- H.265 Encoding Performance
  - 2880x1620@30fps+720x576@30fps
- JPEG Maximum Codec Performance
  - 2880x1620@30fps
- Supports various bit rate control modes such as CBR/VBR/FIXQP.
- Support Region of Interest (ROI) Coding

1.2.5 Video Interface (SG2002)

- Input
  - Supports two simultaneous video inputs (mipi 2L+1L)

- Supports MIPI, Sub-LVDS, HiSPI and other serial interfaces.
- Supports 8/10/12 bit RGB Bayer video input.
- Support BT.656
- Supports the AHD multiplexed BT format.
- Supports SONY, OnSemi, OmniVision and other high-definition CMOS sensors
- Provides a programmable frequency output for the sensor to use as a reference clock.
- Supports a maximum width of 2880 , maximum resolution of 5M (2688x1944, 2880x1620)

- Output
  - Supports a wide range of serial and parallel display specifications.
  - Supports serial interfaces such as MIPI
  - Supports BT656, BT601(8bit), BT1120, 8080 and other parallel interfaces.
  - Supports SPI output interface.

1.2.6 ISP and Image Processing

- Image video 90 degree, 180 degree, 270 degree rotation
- Image Video Mirror, Flip Function
- Video 2-layer OSD overlay
- Video 1/32 to 32x zoom function
- 3A (AE/AWB/AF) algorithms
- Fixed mode noise cancellation, bad dot correction
- Lens shading correction, lens distortion correction, violet edge correction
- Orientation adaptive demosaic
- Gamma correction, (regional/full-area) dynamic contrast enhancement, color management and enhancement
- Zone Adaptive Defogging
- Bayer Noise Reduction, 3D Noise Reduction, Detail Enhancement and Sharpening Enhancement
- Local Tone mapping
- Sensor Self Wide Dynamic and 2 Frame Wide Dynamic
- 2-axis digital image stabilization
- Lens distortion correction
- Provide PC-side ISP tuning tools

1.2.7 CV Hardware Acceleration Engine

- Hardware and software mixed-mode support for some OpenCV libraries.
- Hardware and software mixing modes support some IVE libraries.

1.2.8 Audio codec (SG2002)

- Integrated Audio CODEC, supports 16 bit audio/voice input and output.
- Integrated mono microphone input.
- Integrated mono output. (Requires external amplifier to drive speakers)
- Another microphone is internally integrated to connect directly to the output channel, making it easy to realize AEC.
- Software audio codec protocols (G.711, G.726, ADPCM)
- The software supports Audio 3A (AEC, ANR, AGC) functions.

1.2.9 network interface

- The Ethernet module provides one Ethernet MAC to receive and send network data.
- Ethernet MAC with built-in 10/100Mbps Fast Ethernet Transceiver can work in 10/100Mbps full-duplex or half-duplex mode.

1.2.10 Security system module

- Hardware implementation of multiple encryption and decryption algorithms for AES/DES/SM4
- Hardware implementation of the HASH (SHA1/SHA256) hash algorithm
- Hardware implementation of a random number generator
- Internally integrated 2Kbit eFuse logic space

1.2.11 Intelligent and safe operating environment

- Support for Chain of Trust Establishment: Provides the foundation of a secure environment and is fundamental to a trusted environment, e.g., hardware security settings, root of trust
- Supports secure boot and provides secure hardware and software protection
- Support data encryption security: data encryption program, computing core encryption
- Supports software and firmware validation process: confirms software trustworthiness and integrity, including boot and load validation procedures

- Supports secure storage and transmission: protects external data storage and exchange
- Support security updates

1.2.12 Peripheral Interface (SG2002)

- Integrated POR, Power sequence
- 4 single-ended ADCs (3 no die domain)
- 6 I2C (1 no die domain)
- 3 SPI
- 5 UART groups (1 no die domain)
- 4 groups (15 channels) PWM
- 2 SDIO interfaces.

One SD 3.0 Card with 3V connectivity (supports up to SDXC 2TB, supports UHS-I speed)

One supports 1.8V/3.0V connection to other SDIO 3.0 devices. (Supports UHS-I speeds)

- 66 GPIO interface (14 no die domain)
- Integration with keyscan and Wiegand
- Integrated MAC PHY supports 10/100Mbps full or half duplex mode.
- One USB Host / device interface

1.2.13 external memory interface

- Internal DRAM
  - SG2002 DDR3 16bitx1, up to 1866Mbps, capacity 2Gbit (256MB)
- SPI NOR flash interface (1.8V / 3.0V)
  - Supports 1, 2, 4-wire modes.
  - Supports up to 256MByte.
- SPI Nand flash interface (1.8V / 3.0V)
  - Supports 1KB/2KB/4KB page (corresponding to maximum capacity 16GB/32GB/64GB)
  - Use the ECC module built into the device.
- eMMC 4.5 interface (1.8V/3.0V) SD0 EMMC co-power. Because the SD card defaults 3V, there is SD0 EMMC co-power.

  Not suitable for 1.8V eMMC card.
  - 4 bit interface.
  - Support HS200
  - Maximum Supported Capacity 2TB

1.2.14 SDK

- Linux-5.10-based SDK

1.2.15 Chip Physical Specifications

- Power Consumption
  - 1080P + Video encode + AI : ~ 500mW
  - The rest of the scene : TBD
- Operating Voltage
  - Kernel voltage is 0.9V
  - □□ □□□□□□□ □□ 1 □ 8 □ □□□ 3 □ 0 □□ IO Voltage 1.8V and 3.0V
  - DDR Voltage is shown in the table below.
    - SG2002 = 1.35V
- Encapsulation
  - QFN package, package size 9mmx9mmx0.9mm. pin pitch 0.35mm. total number of pins 88

1.3 Startup and upgrade modes

1.3.1 summarize

The chip is booted from the internal ROM (BOOTROM). During reset, the chip detects the presence of weak pull-ups or pull-downs on two pins (EMMC_DAT3, EMMC_DAT0) to confirm the type of memory device currently selected.

Secure boot chips are signed during boot-up and chip upgrades to ensure that the software being executed or upgraded is secure.

1.3.2 Correspondence between the startup mode and the corresponding signal latch value

- Supports booting from SPI Nor Flash (EMMC_DAT3 pull down, EMMC_DAT0 pull up)
- Supports booting from SPI Nand Flash (EMMC_DAT3 pull down, EMMC_DAT0 pull down)
- Supported by eMMC boot (EMMC_DAT3 pull up, EMMC_DAT0 pull up)

SG2002 because SD0 share IO power with eMMC domain. Because SD card default 3.0V, and eMMC is mostly 1.8V. So basically eMMC is not supported. Unless SD0 is not connected to SD card.

1.3.3 Mirror burn mode .

- supports burning images via SD card.
- supports burning images via USB device mode.
- If there is a mirror image in the flash, the software support is upgraded by the network upgrade software.

1.3.4 Secure Start

- Support for secure boot and upgrade
- AES/DES/SM4 hardware encryption and decryption.
- SHA/TRNG/Secure Efuse Security Hardware.

1.4 address space mapping

Starting address [31:0]	End address [31:0]	Space Function	Space Size (Byte)
0x01000000	0x017FFFFF	reservations	8M
0x01800000	0x018FFFFF	reservations	
0x01900000	0x01900FFF	ap_mailbox	4K
0x01901000	0x01901FFF	ap_system_ctrl	4K
0x01902000	0x019EFFFF	reservations	
0x01F00000	0x01F0FFFF	reservations	64K
0x01F10000	0x01FFFFFF	reservations	
0x02000000	0x02FFFFFF	reservations	64K
0x03000000	0x03000FFF	TOP_MISC Control Register	4K
0x03001000	0x03001FFF	PINMUX Control Register	4K
0x03002000	0x03002FFF	CLKGEN/PLL Control Register	4K
0x03003000	0x03003FFF	RSTGEN Control Register	4K
0x03004000	0x03005FFF	reservations	
0x03006000	0x03006FFF	reservations	4K
0x03007000	0x03008FFF	reservations	
0x03009000	0x03009FFF	reservations	4K
0x0300A000	0x0300AFFF	reservations	4K
0x0300B000	0x0300FFFF	reservations	
0x03010000	0x03010FFF	WATCH DOG0 Control Registers	4K
0x03011000	0x03011FFF	WATCH DOG1 Control Registers	4K
0x03012000	0x03012FFF	WATCH DOG2 Control Registers	4K
0x03020000	0x03020FFF	GPIO0 Control Register	4K
0x03021000	0x03021FFF	GPIO1 Control Register	4K
0x03022000	0x03022FFF	GPIO2 Control Register	4K
0x03023000	0x03023FFF	GPIO3 Control Register	4K
0x03024000	0x0302FFFF	reservations	
0x03030000	0x03030FFF	WGN0 Control Register	4K
0x03031000	0x03031FFF	WGN1 Control Register	4K
0x03032000	0x03032FFF	WGN2 Control Register	4K
0x03033000	0x0303FFFF	reservations	
0x03040000	0x0304FFFF	KEYSCAN Control Register	64K
0x03050000	0x0305FFFF	EFUSE Control Register	64K
0x03060000	0x03060FFF	PWM0 Control Register	4K
0x03061000	0x03061FFF	PWM1 Control Register	4K
0x03062000	0x03062FFF	PWM2 Control Register	4K
0x03063000	0x03063FFF	PWM3 Control Register	4K
0x03064000	0x0309FFFF	reservations	

0x030A0000	0x030AFFFF	TIMER Control Register	64K
0x030C0000	0x030CFFFF	reservations	
0x030D0000	0x030D0FFF	reservations	4K
0x030D1000	0x030D1FFF	reservations	4K
0x030D2000	0x030D2FFF	reservations	4K
0x030D3000	0x030DFFFF	reservations	
0x030E0000	0x030EFFFF	TEMPSEN Control Register	64K
0x030F0000	0x030FFFFF	SARADC Control Register	64K
0x04000000	0x0400FFFF	I2C0 Control Register	64K
0x04010000	0x0401FFFF	I2C1 Control Register	64K
0x04020000	0x0402FFFF	I2C2 Control Register	64K
0x04030000	0x0403FFFF	I2C3 Control Register	64K
0x04040000	0x0404FFFF	I2C4 Control Register	64K
0x04050000	0x0405FFFF	reservations	
0x04060000	0x0406FFFF	SPI_NAND Control Register	64K
0x04070000	0x0407FFFF	ETH0 Control Register	
0x04080000	0x040FFFFF	reservations	
0x04100000	0x04107FFF	I2S0 Control Register	64K
0x04108000	0x0410FFFF	I2S Global Control Register	64K
0x04110000	0x0411FFFF	I2S1 Control Register	64K
0x04120000	0x0412FFFF	I2S2 Control Register	64K
0x04130000	0x0413FFFF	I2S3 Control Register	64K
0x04140000	0x0414FFFF	UART0 Control Register	64K
0x04150000	0x0415FFFF	UART1 Control Register	64K
0x04160000	0x0416FFFF	UART2 Control Register	64K
0x04170000	0x0417FFFF	UART3 Control Register	64K
0x04180000	0x0418FFFF	SPI0 Control Register	64K
0x04190000	0x0419FFFF	SPI1 Control Register	64K
0x041A0000	0x041AFFFF	SPI2 Control Register	64K
0x041B0000	0x041BFFFF	SPI3 Control Register	64K
0x041C0000	0x041CFFFF	UART4 Control Register	64K
0x041D0000	0x041DFFFF	AUDSRC Control Register	64K
0x041E0000	0x042FFFFF	reservations	
0x04300000	0x0430FFFF	eMMC Control Registers	64K
0x04310000	0x0431FFFF	SD0 Control Register	64K
0x04320000	0x0432FFFF	SD1 Control Register	
0x04330000	0x0433FFFF	DMA Control Register	64K
0x04340000	0x0434FFFF	USB Control Register	64K
0x04350000	0x043FFFFF	reservations	
0x04400000	0x0441FFFF	ROM memory space	128K
0x04420000	0x04FFFFFF	reservations	

0x05000000	0x05000FFF	reservations	4KB
0x05020000	0x05020FFF	RTCSYS_Timer Control Registers	4KB
0x05021000	0x05021FFF	RTCSYS_GPIO Control Registers	4KB
0x05022000	0x05022FFF	RTCSYS_UART Control Registers	4KB
0x05023000	0x05023FFF	RTCSYS_INTR Control Registers	4KB
0x05024000	0x05024FFF	RTCSYS_MBOX Control Registers	4KB
0x05025000	0x05025FFF	RTCSYS_CTRL Control Registers	4KB
0x05026000	0x05026FFF	RTCSYS_CORE	4KB
0x05027000	0x05027FFF	RTCSYS_IO Control Registers	4KB
0x05028000	0x05028FFF	RTCSYS_OSC Control Registers	4KB
0x05029000	0x05029FFF	reservations	4KB
0x0502A000	0x0502AFFF	RTCSYS_32kless Control Registers	4KB
0x0502B000	0x0502BFFF	RTCSYS_I2C Control Registers	4KB
0x0502C000	0x0502CFFF	RTCSYS_SAR Control Registers	4KB
0x0502D000	0x0502DFFF	RTCSYS_WDT Control Registers	4KB
0x0502E000	0x0502EFFF	RTCSYS_IRRX Control Registers	4KB
0x05200000	0x053FFFFF	RTCSYS_SRAM	8KB
0x05400000	0x057FFFFF	RTCSYS_SPINOR	4MB
0x08000000	0x08001FFF	reservations	8K
0x08004000	0x08005FFF	DDR Controler Control Register	8K
0x08006000	0x08007FFF	reservations	8K
0x08008000	0x08009FFF	DDR AXI Monitor Control Registers	8K
0x0800A000	0x0800BFFF	DDR Global Control Register	8K
0x08010000	0x08011FFF	reservations	8K
0x08012000	0x08013FFF	reservations	8K
0x08014000	0x09FFFFFF	reservations	
0x0A000000	0x0A07FFFF	ISP Control Register	512K
0x0A080000	0x0A0803FF	sc_top Control Register	1K
0x0A080400	0x0A080BFF	reservations	2K
0x0A080C00	0x0A080CFF	osd enc control register	256B
0x0A080D00	0x0A080FFF	reservations	768B
0x0A081000	0x0A081FFF	reservations	4K
0x0A082000	0x0A082FFF	img_v Control Register	4K
0x0A083000	0x0A083FFF	img_d control register	4K
0x0A084000	0x0A084FFF	sc_d Control Register	4K
0x0A085000	0x0A085FFF	sc_v1 Control register	4K
0x0A086000	0x0A086FFF	sc_v2 Control Register	4K
0x0A087000	0x0A087FFF	sc_v3 Control Register	4K
0x0A088000	0x0A088FFF	DISP Control Register	4K
0x0A089000	0x0A089FFF	reservations	4K
0x0A08A000	0x0A08AFFF	dsi_mac Control Register	4K

0x0A08B000	0x0A08BFFF	cmdq control register	4K
0x0A08C000	0x0A08CFFF	reservations	4K
0x0A08D000	0x0A08DFFF	reservations	4K
0x0A08E000	0x0A09FFFF	reservations	72K
0x0A0A0000	0x0A0AFFFF	IVE Control Register	64K
0x0A0A0000	0x0A0BFFFF	reservations	64K
0x0A0C0000	0x0A0C1FFF	ldc control register	8K
0x0A0C2000	0x0A0C3FFF	VI0/MIPI_RX0 Control Registers	8K
0x0A0C4000	0x0A0C5FFF	VI1/MIPI_RX1 Control Registers	8K
0x0A0C6000	0x0A0C7FFF	VI2/MIPI_RX2 Control Registers	8K
0x0A0C8000	0x0A0C9FFF	VIPSYS Control Registers	8K
0x0A0CA000	0x0A0CFFFF	reservations	24K
0x0A0D0000	0x0A0D0FFF	CSI_PHY Control Registers	4K
0x0A0D1000	0x0A0D1FFF	DSI_PHY Control Registers	4K
0x0A0D2000	0x0AFFFFFF	reservations	
0x0B000000	0x0B00FFFF	JPEG codec control register	64K
0x0B010000	0x0B01FFFF	H.264 codec control registers	64K
0x0B020000	0x0B02FFFF	H.265 codec control registers	64K
0x0B030000	0x0BFFFFFF	reservations	
0x0C000000	0x0FFFFFFF	reservations	
0x10000000	0x1FFFFFFF	SPI_NOR Memory Space	256M
0x30000000	0x7FFFFFFF	reservations	
0x80000000	0xFFFFFFFF	DDR memory space	2G

*Read and write operations to reserved address space may produce unintended results.

2 Hardware Characteristics

2.1 Packages and Pinouts

2.1.1 Package SG2002

The SG2002 is available in a QFN package measuring 9mmx9mmx0.9mm with a pin pitch of 0.35mm and a total of 88 pins. Please refer to the following figure for detailed package dimensions.

		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.7	---
L/F THICKNESS		A3		0.152 REF	
LEAD WIDTH		b	0.13	0.18	0.23
BODY SIZE	X	D		9 BSC	
	Y	E		9 BSC	
LEAD PITCH		e		0.35 BSC	
EP SIZE	X	J	7.6	7.7	7.8
	Y	K	7.6	7.7	7.8
LEAD LENGTH		L	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

Figure *2-1 SG2002* Package Dimensions, Top View

		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.7	---
L/F THICKNESS		A3	0.152 REF		
LEAD WIDTH		b	0.13	0.18	0.23
BODY SIZE	X	D	9 BSC		
	Y	E	9 BSC		
LEAD PITCH		e	0.35 BSC		
EP SIZE	X	J	7.6	7.7	7.8
	Y	K	7.6	7.7	7.8
LEAD LENGTH		L	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa	0.1		
MOLD FLATNESS		bbb	0.1		
COPLANARITY		ccc	0.08		
LEAD OFFSET		ddd	0.1		
EXPOSED PAD OFFSET		eee	0.1		

Figure *2-2. SG2002* Package External Dimensions, Bottom View

2.1.2 Pinouts SG2002

		PAD_MIPI_TXP0	PAD_MIPI_TXM0	PAD_MIPI_TXP1	PAD_MIPI_TXM1	PAD_MIPI_TXP2	PAD_MIPI_TXM2	VDD18A_MIPI	PAD_MIPIRX0P	PAD_MIPIRX0N	PAD_MIPIRX1P	PAD_MIPIRX1N	PAD_MIPIRX2P	PAD_MIPIRX2N	PAD_MIPIRX3P	PAD_MIPIRX3N	PAD_MIPIRX4P	PAD_MIPIRX4N	VDDC	USB_DM	USB_DP	VDD18A_USB_PLL_ETH	GPIO_RTX___EPHY_RTX		
		88	87	86	85	84	83	82	81	80	79	78	77	76	75	74	73	72	71	70	69	68	67		
VSS18A_AUD	1																							66	VDD33A_ETH_USB
PAD_AUD_AINL_MIC	2																							65	PAD_ETH_RXM___EPHY_TXP
PAD_AUD_AVREF	3																							64	PAD_ETH_RXP___EPHY_TXN
PAD_AUD_AOUTR	4																							63	PAD_ETH_TXM___EPHY_RXP
VDD18A_AUD	5																							62	PAD_ETH_TXP___EPHY_RXN
SD0_CLK	6																							61	VDDC
SD0_CMD	7																							60	USB_VBUS_DET
SD0_D0	8																							59	ADC1
VDDC	9																							58	PWM0_BUCK
SD0_D1	10																							57	VDDIO_SD1
SD0_D2	11													VSSC (EPAD)										56	SD1_CLK
SD0_D3	12																							55	SD1_CMD
VDDIO_SD0_EMMC	13																							54	SD1_D0
SD0_CD	14																							53	SD1_D1
SD0_PWR_EN	15																							52	SD1_D2
VDDC	16																							51	SD1_D3
SPK_EN	17																							50	VDDC
UART0_TX	18																							49	PWR_GPIO2
UART0_RX	19																							48	PWR_GPIO1
EMMC_DAT2	20																							47	PWR_GPIO0
EMMC_CLK	21																							46	XTAL_XOUT
EMMC_DAT0	22																							45	XTAL_XIN
		23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44		
		EMMC_DAT3	EMMC_CMD	EMMC_DAT1	JTAG_CPU_TMS	JTAG_CPU_TCK	IIC0_SCL	IIC0_SDA	AUX0	VDDQ_DRAM	VDDQ	VDDQ	VDDQ_DRAM	GPIO_ZQ___PAD_ZQ	VDDIO_RTC	VDDC_RTC	PWR_VBAT_DET	PWR_RSTN	PWR_SEQ1	PWR_SEQ2	PTEST	PWR_WAKEUP0	PWR_BUTTON1		

Figure *2-3 SG2002* Pin Assignment Diagram.

2.2 Pin Information Description

Please refer to SG2002_PINOUT_CN.xlsx

2.3 Welding process recommendations

Refer to Figure 2-4 for lead-free reflow process curves SG2002 Refer to Pure Sn

Figure *2-4* Lead-Free Reflow Process Curve

Refer to Table 2-1 for lead-free reflow process parameters.

- The following parameters are only recommended values for reference, the client needs to make relative adjustments according to the actual production situation.

Table *2-1* Lead-Free Reflow Worker Cover Parameters

shore	timing	heating rate	peak temperature	cooling rate
Preheating zone (40~150° C)	60~120sc	1~2° C/sec		
Homogeneous zone (150~200° C)	60~90sec	< 1° C/sec		

reflux zone (>Melting point 20~30° C)	40~60sec	2~3° C/sec	Sn/Ag/Cu 237~247° C Sn/Cu 247~257° C Pure Sn 252~262 C°	
cooling zone (Tmax ~ Tamb)				1~4° C/sec

Due to environmental concerns, the parameters for leaded reflow soldering are not available at this time.

2.4 Parameters of Chiu Min

2.4.1 Calculated energy products moisture-proof packaging

This section establishes the principles to be used when storing and soldering chips (moisture-sensitive products). Related Terms

- Floor life (open storage time) : The maximum time allowed between unpacking and reflow in an environment < 30oC/60% RH.
- Shelf life : Normal storage time after sealing of the moisture-proof package.

2.4.1.1 Packaging Information

Moisture-proof vacuum bag containing (1) chip and tray. (2) Dry Pack (3) Humidity

Identification Card (HIC)

Figure *2-5* Vacuum Drying Packaging Information .

Figure *2-6* Dry Packs, Humidity Cards, Chips and Trays

2.4.1.2 Tide-sensitive product incoming inspection

After opening the vacuum bag before SMT, inspect the humidity card. There are many different types of humidity cards. However, if the card shows that it has been exposed to moisture, it must be baked before it can be used in SMT. It must be baked before SMT. See table 2-3 for baking time and temperature parameters.

If repackaged after opening. If the package has not been exposed to < 30° C/60% RH for more than 2 hours, the package may be vacuum dried by simply replacing the dryer pack. If more than 2 hours. It is recommended to re-seal the package after re-baking and replacing the dryer pack.

2.4.1.3 Storage and Use. (Reference JEDEC J-STD-033)

- Sealed storage time. (Shelf life)

  Sealed vacuum-proof packages, stored at 40° C/90% RH, can be stored for at least 12 months.

- Open and keep for a long time. (Floor life)

  Before SMT, the hygrometer shows that there is no moisture in the components after opening. At 30° C/60% RH, it is possible to use the chip without baking for a period of time as shown in Table 2-2, Level 3 (Floorlife rating for this chip is Level 3).

Table *2-2* Humidity Classification and its Opened Storage Time *(floor life)*

Moisture classification level and floor life

Level	Floor Life (out of bag) at factory ambient ≤ 30 °C/60% RH or as stated
1	Unlimited at ≤ 30 °C/85%RH
2	1 year
2a	4 weeks
3	168 hours
4	72 hours
5	48 hours
5a	24 hours
6	Mandatory bake before use. After bake, must be reflowed within the time limit specified on the label

2.4.1.4 Re-baking

If moisture is found after opening, it should be baked before SMT, or if it is to be re-packed into vacuum packs. The product should be baked first. Refer to Table 2-3 for baking temperature and time.

After baking and sealing against moisture, shelf life can be recalculated.

After baking, if not sealed against moisture, the storage time reference (floor life)

Table *2-3* Baking Temperature and Schedule

Package Thickness	Level	Bake @ 125 °C	Bake @ 40 °C ≤ 5% RH
≤ 1.4 mm	2a	4 h.	5 days
	3	7 h.	11 days
	4	9 h.	13 days
	5	10 h.	14 days
	5a	14 h.	19 days
≤ 2.0 mm	2a	18 h.	21 days
	3	24 h.	33 days
	4	31 h.	43 days
	5	37 h.	52 days
	5a	48 h.	68 days
≤ 4.0 mm	2a	48 h.	67 days
	3	48 h.	67 days
	4	48 h.	68 days
	5	48 h.	68 days
	5a	48 h.	68 days

2.5 Electrical Performance Parameters

2.5.1 Power consumption parameters

Typical Scene : 1080P + Video Encode + AI ~500mW
Other Scenarios : TBD

2.5.2 Temperature and thermal resistance parameters (SG2002)

Thermal Resistance ThetaJA, JB, JC values of the chip. Santalum album results according to JEDEC 2s2p PCB Table 2-4

Table *2-4 SG2002* Thermal Resistance Parameters

PCB Condition	Package Size(mm)	Theta JA (C/W)			Psi Jt (C/W)	Theta JC (C/W)	Theta JB (C/W)
		0 m/s	1 m/s	2 m/s			
JEDEC 2s2p PCB	9x9	20.3	15.9	14.8	0.17	6.9	5.32

The temperature-related parameters of the chip are shown in Table 2-5.

Table *2-5* Temperature-Related Parameters

	minimum value	maximum values	Note
Operating ambient temperature Tamb	-30 C°	70 C°	1
Chip Junction Temperature Tjunc Recommended	-30 C°	85° C ~ 105 C°	2
destructive coking temperature	-40 C°	+125 C°	3, 4

1. The maximum operating temperature, without violating the junction temperature, depends on the power consumption and heat dissipation conditions of the scene.
2. The recommended range of junction temperature for the chip is to consider that if the temperature is too high, it may cause thermal run-away

due to poor heat dissipation conditions. The recommended junction temperature range is to consider the possibility of thermal run-away and damage to the chip due to poor heat dissipation. In addition. Prolonged operation at high temperatures will also accelerate the aging of the chip. This will reduce the service life of the chip.

3. The guaranteed junction temperature of the DRAM used is only -40° C~115° C. The integrity of the content in the range dram is not guaranteed.
4. Chips operating at destructive junction temperatures may cause irreversible physical damage to the chip.

2.5.3 destructive voltage

The destructive voltage parameters are shown in Table 2-6. Operation at destructive voltages may cause irreversible physical damage.

Table *2-6* Destructive Voltage Parameters *(SG2002)*

Parameter		Max.	Unit
VDDC	Core power	1.05V	V
VDDC_RTC	Core power for RTC domain (own LDO)		
VDD18A_AUD	Analog power for Audio ADC/DAC	1.98	V
vdd18a_usb_pll_eth	Analog power for USB, PLL, ETH, efuse	1.98	V
VDD18A_MIPI	Analog power for MIPI	1.98	V
VDD33A_ETH_USB	Analog power for Ethernet PHY, USB PHY	3.465	V
VDDIO_SD0_EMMC	IO power for EMMC & SD0 domain	3.465	V
VDDIO_SD1	IO power for SD1 domain	3.465	V
VDDIO_RTC	IO power for RTC domain (backup power)	1.98	V
VDDQ **VDDQ_DRAM**	IO & DRAM Power for DDR2/DDR3L/DDR3	1.65	V

2.5.4 Power up/down sequence (SG2002)

In principle, chips can be divided into the following groups. The same group of power domains is powered up/down at the same time. Different groups. The power up/down times are separated according to the following conditions.

- Always on domain
  - VDDIO_RTC (1.8V)
  - VDDC_RTC (0.9V) (built-in LDO)
  - VDDIO_SD1
- Core power domain
  - VDDC
- 1.8V IO domain
  - vdd18a_aud (analog)
  - vdd18a_usb_pll_eth (analog)
  - VDD18A_MIPI (analog)
- 18OD33 IO domain (1.8V domain / 3V domain depending on voltage)
  - VDDIO_SD1 (also no die domain)
- 3V domain
  - VDDIO_SD0_EMMC
  - VDD33A_ETH USB

- DDR IO & DRAM domain
  - VDDQ

- VDDQ_DRAM

In principle, 0.9V and 1.8V can be powered up at the same time, or 0.9V first. 1.8V second, but 3V can only be powered up if 1.8V is already established. 1.8V first and 1.8V second, **but 3V can only be energized when 1.8V is already established. (Failure to do so may cause irreversible damage). The** power down sequence is the reverse of the power up sequence.

Up and down power behaviors that may pose a risk are.

1. At power up, if VDD3 > 2V, VDD18 is still not at 1.8V-10%. Possible damage to the 3V circuit.
2. When powering down, VDD3 < 2V before VDD18 is below 1.8V-10%.
3. When VDD18 > 0.7V at power-on, VDD09 is still below 0.5V, which may cause efuse malfunction.
4. When VDD09< 0.5V, VDD18 is still > 0.7V during power down, which may also cause efuse malfunction.

The chip provides two pins PWR_SEQ1, PWR_SEQ2 (VDDIO_RTC domain) to co-control the power switching. SEQ1 is preset to be 0.9V & 1.8V. SEQ2 controls 3V. Some plug-in systems may use RC to determine the switching for both 0.9V and 1.8V. Only the 3V to the chip needs to be controlled by SEQ2. To avoid burnout.

SEQ1 -> SEQ2 at power-up

SEQ2 -> SEQ1 on power off

PWR_VBAT_DET is used to detect the status of the main power supply. If the voltage is low, the software receives an interrupt (e.g. to stop writing flash to prevent file system corruption). If the voltage goes further down, the RTC module will initiate a power down program.

PWR_VBAT_DET also needs to be logic high in order to power on.

1. 1.8V IO

Parameter		Min	Typ	Max	Unit
V_{IL}	Input Low voltage	-0.3		0.35xVDDIO	V
V_{IH}	Input High voltage	0.65*VDDIO		1.98	V
V_T (no pull)	Threshold voltage when ST[1:0] = 00	0.75	0.91	1.09	
V_{T_PU}	(no schmit trigger)	0.74	0.90	1.08	V
V_{T_PD}		0.76	0.92	1.10	
V_{T+}		0.82	0.97	1.13	
V_{T-}		0.72	0.85	1.02	
V_{T+_PU}	Threshold voltage when ST[1:0] = 01	0.81	0.96	1.12	V
V_{T-_PU}		0.71	0.84	1.01	
V_{T+_PD}		0.82	0.98	1.14	
V_{T-_PD}		0.73	0.86	1.03	
V_{T+}		0.87	1.04	1.19	
V_{T-}		0.69	0.80	0.95	
V_{T+_PU}	Threshold voltage when ST[1:0] = 1X	0.86	1.03	1.18	V
V_{T-_PU}		0.68	0.79	0.94	
V_{T+_PD}		0.88	1.05	1.20	
V_{T-_PD}		0.69	0.81	0.96	

In practice. The following four conditions can be subdivided. The recommendations are as follows.

Power	Control	Plug-in applications (1) Ext RTC/no RTC	Plug-in applications (2) 32Kless
Main 0.9V	Always on	VDDC	VDDC
Main 1.8V	Always on	vdd18a_aud vdd18a_usb_pll_eth vdd18a_mipi vddio_sd1 vddio_rtc	vdd18a_aud vdd18a_usb_pll_eth vdd18a_mipi
Main 3.0V	SEQ2	vdd33a_eth_usb vddio_sd0_emmc vddio_sd1	vdd33a_eth_usb vddio_sd0_emmc
Main VDDQ	always on	VDDQ VDDQ_DRAM	VDDQ VDDQ_DRAM
VDDBACKUP	Coin Batt	For external RTC	
V18RTC (low iddq LDO)	Always on , from Coin batt	No need	VDDIO_RTC VDDIO_SD1

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Power	Control	Battery applications (3) **Ext RTC/no RTC**	Battery applications (4) **32Kless**
Main 0.9V	SEQ1	VDDC	VDDC
Main 1.8V	SEQ1	vdd18a_aud vdd18a_usb_pll_eth vdd18a_mipi	vdd18a_aud vdd18a_usb_pll_eth vdd18a_mipi
Main 3.0V	SEQ2	vdd33a_eth_usb vddio_sd0_emmc	vdd33a_eth_usb vddio_sd0_emmc
Main VDDQ	SEQ2 or 3	VDDQ VDDQ_DRAM	VDDQ VDDQ_DRAM
VDDBACKUP	Coin Batt	For external RTC	
V18RTC (low iddq LDO)	Always on , from Coin batt	No need	VDDIO_RTC
VAO18	from Main batt	WIFI other AO device VDDIO_RTC VDDIO_SD1	WIFI other AO device VDDIO_SD1
VAO33	from Main batt	WIFI other AO device	WIFI other AO device

2.5.5 Power supply DC/AC Electrical parameters

Table *2-7 SG2002* Power Supply Electrical Parameters *(*Recommended Operating Conditions*)*

Parameter		Min	Typ	Max.	Unit
VDDC	Core power	0.81	0.9	0.99	V
VDDC_RTC	Core power for RTC domain (Internal LDO, Cap only)	0.81	0.9	0.99	V
VDD18A_AUD	Analog power for Audio ADC/DAC	1.62	1.8	1.98	V
vdd18a_usb_pll_eth	Analog power for Ethernet PHY, USB PHY, PLL	1.62	1.8	1.98	V
VDD18A_MIPI	Analog power for MIPI	1.62	1.8	1.98	V
VDD33A_ETH_USB	Analog power for Ethernet PHY, USB PHY	2.97	3.3	3.465	V
					V

VDDIO_SD0_EMMC	IO power for SD0 & EMMC domain	1.71 2.85	1.8 3.0/3.3	1.89 3.15/3.465	V
VDDIO_SD1	IO power for SD1 domain	1.71 2.85	1.8 3.0/3.3	1.89 3.465	V

Parameter		Min	Typ	Max.	Unit
VDDIO_RTC	IO power for RTC domain IO & LDO	1.3V	1.8	+10%	V
VDDQ **VDDQ_DRAM**	IO & DRAM Power for DDR3L IO & DRAM Power for DDR3 IO & DRAM Power for DDR2	1.283 1.425 1.425	1.35 1.50 1.50	1.417 1.575 1.575	V
Tjunc	Junction Temperature (Max reduce from 125C due to DRAM)	-40	25	115 (note)	oC

Note. The DRAM used guarantees a junction temperature of only -40° C~115° C. The integrity of the content in the range dram is not guaranteed.

2.5.6 1.8V IO Electrical Parameters

Apply domain (VDDIO18_0, VDDIO18_1, VDDIO18_RM0, VDDIO_RTC)

Table *2-8 1.8V IO* Electrical Parameters

Parameter		Min	Typ	Max.	Unit
V_{IL}	Input Low voltage	-0.3		0.35xVDDIO	V
V_{IH}	Input High voltage	0.65*VDDIO		1.98	V
V_{T} (no pull) V_{T_PU} V_{T_PD}	Threshold voltage when ST[1:0] = 00 (no schmit trigger)	0.75 0.74 0.76	0.91 0.90 0.92	1.09 1.08 1.10	V
V_{T+} V_{T-} V_{T+_PU} V_{T-_PU} V_{T+_PD} V_{T-_PD}	Threshold voltage when ST[1:0] = 01	0.82 0.72 0.81 0.71 0.82 0.73	0.97 0.85 0.96 0.84 0.98 0.86	1.13 1.02 1.12 1.01 1.14 1.03	V
V_{T+} V_{T-} V_{T+_PU} V_{T-_PU} V_{T+_PD} V_{T-_PD}	Threshold voltage when ST[1:0] = 1X	0.87 0.69 0.86 0.68 0.88 0.69	1.04 0.80 1.03 0.79 1.05 0.81	1.19 0.95 1.18 0.94 1.20 0.96	V
I_{I}	Input leakage (V_{I} = 1.8V or 0V)			+/-10u	A
I_{OZ}	Tri-state output leakage current (VO=1.8V or 0V)			+/-10u	A
R_{PU}	Pull up resistor	55k	79k	121k	Ω
R_{PD}	Pull down resistor	51k	87k	169k	Ω
V_{OL}	Output low voltage			0.45	V
V_{OH}	Output high voltage	1.35			V
I_{OL}	Low level output current @ V_{OL} (max) DS[1:0] = 00 DS[1:0] = 01 DS[1:0] = 10 DS[1:0] = 11	 7.6 15.2 22.6 29.7	 12.8 25.3 37.4 49	 18.0 35.5 52.2 67.9	 mA mA mA mA
I_{OH}	High level output current @ V_{OH} (max) DS[1:0] = 00 DS[1:0] = 01 DS[1:0] = 10 DS[1:0] = 11	 4.8 9.5 14.3 18.9	 10.8 21.5 32.1 42.4	 18.9 37.4 55.9 73.9	 mA mA mA mA

2.5.7 18OD33 IO (VDDIO=1.8V) Electrical Parameters

Apply domain (VDDIO_EMMC, VDDIO_SD0)

Table *2-9 18OD33 IO (VDDIO=1.8V)* Electrical Parameters

Parameter		Min	Typ	Max.	Unit
V_{IL}	Input Low voltage	-0.3		0.58	V

Parameter		Min	Typ	Max.	Unit
VIH	Input High voltage	1.27		2.00	V
VT (no pull) VT_PU VT_PD	Threshold voltage when ST = 0 (no schmit trigger)	0.91 0.90 0.91	0.97 0.96 0.97	1.03 1.02 1.06	V
VT+ (no pull) VT- (no pull) VT+_PU VT-_PU VT+_PD VT-_PD	Threshold voltage when ST = 1	1.03 0.75 1.02 0.74 1.03 0.75	1.07 0.83 1.06 0.82 1.08 0.83	1.12 0.91 1.11 0.90 1.13 0.92	V
II	Input leakage (VI = 1.8V or 0V)			+/-10u	A
IOZ	Tri-state output leakage current (VO=1.8V or 0V)			+/-10u	A
RPU	Pull up resistor	33k	60k	92k	Ω
RPD	Pull down resistor	34k	61k	158k	Ω
VOL	Output low voltage			0.45	V
VOH	Output high voltage	1.40			V
IOL	Low level output current @ VOL (max) DS[2:0] = 000 DS[2:0] = 001 DS[2:0] = 010 DS[2:0] = 011 DS[2:0] = 100 DS[2:0] = 101 DS[2:0] = 110 DS[2:0] = 111	 4.9 7.4 9.8 12.2 14.6 17.0 19.4 21.7	 7.8 11.7 15.5 19.2 23.0 26.6 30.2 33.7	 11.1 16.4 21.7 26.7 31.9 36.8 41.6 46.2	 mA mA mA mA mA mA mA mA
IOH	High level output current @ VOH (max) DS[2:0] = 000 DS[2:0] = 001 DS[2:0] = 010 DS[2:0] = 011 DS[2:0] = 100 DS[2:0] = 101 DS[2:0] = 110 DS[2:0] = 111	 3.6 5.4 7.2 9.0 10.8 12.6 14.4 16.2	 6.2 9.3 12.4 15.4 18.5 21.6 24.6 27.7	 9.5 14.3 19.1 23.8 28.5 33.1 37.8 42.5	 mA mA mA mA mA mA mA mA

2.5.8 18OD33 IO (VDDIO=3.0V) Electrical Parameters

Apply domain (VDDIO_EMMC, VDDIO_SD0)

Table *2-10 18OD33 IO (VDDIO=3.0V)* Electrical Parameters

Parameter		Min	Typ	Max.	Unit
VIL	Input Low voltage	-0.3		0.25*VDDIO	V
VIH	Input High voltage	0.625*VDDIO		3.3	V
VT (no pull) VT_PU VT_PD	Threshold voltage when ST = 0 (no schmit trigger)	0.82 0.81 0.83	0.95 0.93 0.96	1.11 1.09 1.13	V
VT+ (no pull)	Threshold voltage when ST = 1	1.00	1.10	1.23	V

Parameter		Min	Typ	Max.	Unit
$_{VT-}$ **(no pull)** VT+_PU VT-_PU VT+_PD VT-_PD		0.75 1.00 0.73 1.01 0.75	0.90 1.09 0.88 1.11 0.91	1.08 1.21 1.05 1.25 1.09	
II	Input leakage ($_{VI}$ = 3.0V or 0V)			+/-10u	A
IOZ	Tri-state output leakage current (VO=3.0V or 0V)			+/-10u	A
RPU	Pull up resistor	33k	60k	93k	Ω
RPD	Pull down resistor	34k	62k	285k	Ω
VOL	Output low voltage			0.125*VDDIO	V
VOH	Output high voltage	0.75*VDDIO			V
IOL	Low level output current @ $_{VOL}$ (max) DS[2:0] = 000 DS[2:0] = 001 DS[2:0] = 010 DS[2:0] = 011 DS[2:0] = 100 DS[2:0] = 101 DS[2:0] = 110 DS[2:0] = 111	 3.1 4.7 6.2 7.7 9.3 10.8 12.3 13.8	 5.5 8.2 10.8 13.4 16.1 18.7 21.2 23.7	 8.6 12.7 16.9 20.8 24.9 28.8 32.6 36.3	 mA mA mA mA mA mA mA mA mA mA mA
IOH	High level output current @ $_{VOH}$ (max) DS[2:0] = 000 DS[2:0] = 001 DS[2:0] = 010 DS[2:0] = 011 DS[2:0] = 100 DS[2:0] = 101 DS[2:0] = 110 DS[2:0] = 111	 5.0 7.5 10.1 12.6 15.1 17.6 20.1 22.6	 7.5 11.2 14.9 18.6 22.3 26.0 29.8 33.4	 10.5 15.7 21.0 26.2 31.4 36.5 41.8 46.9	 mA mA mA mA mA mA mA mA mA mA mA

2.5.9 Audio GPIO Electrical Parameters

Table 2-11 *Audio GPIO* Electrical Parameters

Parameter		Min	Typ	Max.	Unit
V_{IL}	Input Low voltage	-0.3		0.55	V
V_{IH}	Input High voltage	1.2		1.98	V
V_{T+} V_{T-}	Threshold voltage with schmitt trigger	0.8 0.65	0.95 0.82	1.1 0.99	V
I_I	Input leakage (V_I = 1.8V or 0V)			+/-4u	A
I_{OZ}	Tri-state output leakage current (VO=1.8V or 0V)			+/-4u	A
V_{OL}	Output low voltage			0.4	V
V_{OH}	Output high voltage	1.4			V
I_{OL}	Low level output current @ V_{OL} (max)	4.9	9.9	18.4	mA
I_{OH}	High level output current @ V_{OH} (max)	11.3	17.1	26.1	mA

2.5.10 ETH GPIO Electrical Parameters

Table 2-12 *ETH GPIO* Electrical Parameters

Parameter		Min	Typ	Max.	Unit
V_{IL}	Input Low voltage	-0.3		0.3*VDD18A	V
V_{IH}	Input High voltage	0.7*VDD18A		1.98	V
V_{T+} V_{T-}	Threshold voltage with schmitt trigger	0.84 0.66	0.99 0.83	1.14 1.01	V
I_I	Input leakage (V_I = 1.8V or 0V)			+/-1.3u	A
I_{OZ}	Tri-state output leakage current (VO=1.8V or 0V)			+/-1.3u	A
V_{OL}	Output low voltage			0.4	V
V_{OH}	Output high voltage	VDD18A-0.4			V
I_{OL}	Low level output current @ V_{OL} (max) DS=0 Low level output current @ V_{OL} (max) DS=1	8.8 10.2	15.7 17.8	27.3 30.5	mA
I_{OH}	High level output current @ V_{OH} (max) DS=0 High level output current @ V_{OH} (max) DS=1	4.0 4.7	5.3 6.2	7.4 8.5	mA

2.5.11 MIPI Rx Electrical Parameters

The MIPI D-PHY High Speed (MIHS) electrical parameters are shown in Table 2-13 and Table 2-14.

The MIPI D-PHY Low Power (MILP) electrical parameters are shown in Table 2-15, Table 2-16.

MIPI D-PHY High Speed (MISH) Differential *DC* Electrical Parameters

參數	符號	資料速度	最小值	典型值	最大值	單位
Common Mode Voltage Range (VP+VM)/2	VCM(MIHS)	≤1.5Gbps	70	200	330	mV
		>1.5Gbps				
Internal Termination Resister Value	ZID(MIHS)	≤1.5Gbps	80	100	125	ohm
		>1.5Gbps				
Single-ended threshold for HS termination enable	VTERM-EN(MIHS)	≤1.5Gbps	--	--	450	mV
		>1.5Gbps				

MIPI D-PHY High Speed (MIHS) Differential *AC* Electrical Parameters

參數	符號	資料速度	最小值	典型值	最大值	單位
Differential Input Threshold Voltage (VP－VM)	VIDTH(MIHS)	≤1.5Gbps	-70	--	70	mV
		>1.5Gbps	-40	--	40	
Single-ended Input Voltage VP,VM	VIS(MIHS)	≤1.5Gbps	-40	--	460	mV
		>1.5Gbps				
Common-mode interface beyond 450MHz	ΔVCMRX	≤1.5Gbps	--	--	100	mV
		>1.5Gbps				
Common-mode interface 50MHz-450MHz	ΔVCMRX(LF)	≤1.5Gbps	-50	--	50	mV
		>1.5Gbps	-25	--	25	
Single-ended threshold for HS termination enable	VTERM-EN	≤1.5Gbps	--	--	450	mV
		>1.5Gbps				
Common-mode termination	CCM	≤1.5Gbps	--	--	60	pF
		>1.5Gbps				

Table *2-15 MIPI D-PHY Low Power (MILP)* Differential *DC* Electrical Parameters

參數	符號	最小值	典型值	最大值	單位
Logic 1 input voltage	VIHLP	740	--	--	mV
Logic 0 input voltage	VILLP	--	--	550	mV
Input hysteresis	VHYST	25	--	--	mV

Table *2-16 MIPI D-PHY Low Power (MILP)* Differential *AC* Electrical Parameters

参數	符號	最小值	典型值	最大值	單位
Input pulse rejection	eSPIKE	--	--	300	V·ps
Minimum pulse width response	TMIN-RX	20	--	--	ns
Peak interference amplitude	VINT	--	--	200	mV
Interference frequency	fINT	450	--	--	MHz

2.5.12 Sub-LVDS Electrical Parameters

The electrical parameters are shown in Table 2-17 and Table 2-18.

Table *2-17 Sub-LVDS(SL)* Differential *DC* Electrical Parameters

參數	符號	最小值	典型值	最大值	單位
Common Mode Voltage Range (VP+VM)/2	VCM(SL)	600	900	1200	mV
Internal Termination Resister Value	ZID(SL)	80	100	120	mV

Table *2-18 Sub-LVDS(SL)* Differential *AC* Electrical Parameters

參數	符號	最小值	典型值	最大值	單位
Differential Input Threshold Voltage (VP—VM)	VIDTH(SL)	-70	--	70	mV
Single-ended Input Voltage VP,VM	VIS(SL)	400	--	1400	mV

2.5.13 HiSPi Electrical Parameters

HiSPi is divided into SLVS (HSSL) and HiVCM (HSHI), and their respective electrical parameters are shown in Table 2-19 and Table 2-20.

Table *2-19 HiSPi* Differential *DC* Electrical Parameters

參數	符號	最小值	典型值	最大值	單位
Common Mode Voltage Range (VP+VM)/2	VCM(HSSL)	50	200	350	mV
	VCM(HSHI)	660	900	1170	
Internal Termination Resister Value	ZID(HSSL)	80	100	125	mV
	ZID(HSHI)	80	100	125	

Table 2-20 *HiSPi* Differential *AC* Electrical Parameters

參數	符號	最小值	典型值	最大值	單位
Differential Input Threshold Voltage (VP—VM)	VIDTH(HSSL)	-70	--	70	mV
	VIDTH(HSHI)	-100	--	100	
Single-ended Input Voltage VP,VM	VIS(HSSL)	-40	--	490	mV
	VIS(HSHI)	550	--	1350	

2.5.14 MIPI /LVDS Tx Electrical Parameters

Table 2-21 *MIPI HS Transmitter DC Specifications*

Symbol	Description	Min	Typ	Max.	Units	Notes
V_{CMTX}	HS transmit static common-mode voltage	150	200	250	mV	
$\lvert\Delta V_{CMTX(1,0)}\rvert$	VCMTX mismatch when output is Differential-1 or Differential-0	-	-	5	mV	
$\lvert V_{OD}$	HS transmit differential voltage	140	200	270	mV	
$\lvert\Delta V_{OD}\rvert$	VOD mismatch when output is Differential-1 or Differential-0	-	-	14	mV	
V_{OHHS}	HS output high voltage	-	-	360	mV	
Z_{OS}	Single ended output impedance	40	50	62.5	Ω	
ΔZ_{OS}	Single ended output impedance mismatch	-	-	20	%	

Table 2-22 *MIPI HS Transmitter AC Specifications*

Parameter	Description	Min	Typ	Max.	Units	Notes
$\Delta V_{CMTX(HF)}$	Common-level variations above 450MHz	-	-	15	mV_{RMS}	
$\Delta V_{CMTX(LF)}$	Common-level variation between 50-450MHz	-	-	25	mV_{PEAK}	
t_R and t_F	20%-80% rise time and fall time	-	-	0.3	UI	1, 2
		-	-	0.35	UI	1, 3
		100	-	-	ps	4

Note.

1. UI is unit interval. Example: 1UI = 1ns for 1Gbps speed.

2. Applicable when supporting maximum HS bit rates ≤ 1 Gbps (UI ≥ 1 ns).

3. Applicable when supporting maximum HS bit rates > 1 Gbps (UI ≤ 1 ns) but ≤ 1.5 Gbps (UI ≥ 0.667 ns).

4. Applicable when supporting maximum HS bit rates ≤ 1.5 Gbps. However, to avoid excessive radiation, bit rates < 1 Gbps (UI ≥ 1 ns), should not use values below 150 ps.

Table 2-23 *MIPI LP Transmitter DC Specifications*

Parameter	Description	Min	Typ	Max.	Units	Notes
V_{OH}	Thevenin output high level	1.1	1.2	1.3	V	1
		0.95	-	1.3	V	2

Parameter	Description	Min	Typ	Max.	Units	Notes
V_{OL}	Thevenin output low level	-50	-	50	mV	-
Z_{OLP}	Output impedance of LP transmitter	110	-	-	Ω	

Note.

1. Applicable in normal Low Power mode when the supported data rate ≤1.5 Gbps.

2. Applicable in normal Low Power mode when the supported data rate > 1.5 Gbps.

Form *2-24 MIPI LP Transmitter AC Specifications*

Parameter	Description	Min	Typ	Max.	Units	Notes
T_{RLP}/T_{FLP}	15%-85% rise time and fall time	-	-	25	ns	
T_{REOT}	30%-85% rise time and fall time	-	-	35	ns	
$T_{LP\text{-}PULSE\text{-}TX}$	Minimu pulse width	20	-	-	ns	
$\delta V/\delta t_{SR}$	Slew rate @ CLOAD = 0 to 70pF (Falling Edge Only)	30	-	300	mV/ns	1
		25	-	300	mV/ns	2
C_{LOAD}	Load capacitance	0	-	70	pF	

Note.

1. Applicable in normal Low Power mode when the supported data rate ≤1.5 Gbps.

2. Applicable in normal Low Power mode when the supported data rate > 1.5 Gbps.

Table *2-25 LVDS Transmitter DC/AC Specifications*

Symbol	Description	Min	Typ	Max.	Units	Notes
V_{OS}	LVDS common mode offset voltage	1.125	1.25	1.375	V	
$\lvert\Delta V_{OS(1,0)}\rvert$	VOS mismatch when output is Differential-1 or Differential-0	-			mV	
V_{OD}	LVDS transmit differential voltage	247	350	454	mV	
$\lvert\Delta V_{OD}\rvert$	VOD mismatch when output is Differential-1 or Differential-0	-	-	50	mV	
T_{RLP}/T_{FLP}	15%-85% rise time and fall time (DUT side)		-	0.3UI	ns	

2.5.15 SDIO Electrical Parameters

For EMMC / SD0 / SD1, please refer to 2.5.7 and 2.5.8.

2.5.16 VI RAW/BT.601/BT.656/BT.1120 Electrical Parameters

See 2.5.7 and 2.5.8 for the domain where the IO is located.

2.5.17 Electrical parameters BT.601/BT.656/8080 in VO (Video out)

See 2.5.7 and 2.5.8 for the domain where the IO is located.

2.5.18 AUDIO CODEC Electrical Parameters

Table 2-26 *Audio CODEC* Overall Indicator Table

parameters	minimum value	typical value	maximum values	unit (of measure)	clarification
Analog Circuit Power Supplies AVDD	1.62	1.8	1.98	V	
VREF		1.4/1.8 *VDD		V	

Table 2-27 *Audio DAC* Electrical Parameters

parameters	minimum value	typical value	maximum values	unit (of measure)	clarification
Full-width output amplitude		1.55		Vpp	Maximum output signal swing

Table 2-28 *Audio ADC* Electrical Parameters

parameters	minimum value	typical value	maximum values	unit (of measure)	clarification
Maximum Input Amplitude		1.75		Vpp	Maximum input signal swing

2.6 interface timing

2.6.1 SPI NOR Interface Timing

Figure 2-7 *SPI NOR* Interface Timing Chart

*IO input timing / IO output timing refers to the IO timing for each of the 1xI/O, 2xI/O, and 4xI/O for the transmission of SPI_NOR CMD/DATA, which includes SPINOR_SDI, SPINOR_SDO, SPINOR_HOLD_X, SPINOR_WP_X, SPINOR_HOLD_X, and SPINOR_WP_X.

Table 2-29 *SPI_NOR* Interface Timing Parameter Table

notation	descriptive	minimal	general	greatest	unit (of measure)
Tcss	CS Negative edge time from first clock edge	13.4	-	-	ns
Tclk	clock cycle	13.4	-	-	ns
Tsu	Input Signal Establishment Time Requirements	3.5	-	-	ns
Thd	Input Signal Hold Time Requirements	0	-	-	ns
Tov	Effective delay time of output signal	-	-	2.6	ns
TOX	Output signal hold time	-1.5	-	-	ns

2.6.2 SPI NAND Interface Timing

Figure 2-8 *SPI NAND* Input

Direction Timing Diagram Table

***2-30 SPI NAND* Input Direction**

Requirements					

Figure *2-9 SPI NAND* Output

Direction Timing Diagram Table

***2-31 SPI NAND* Output Direction**

Timing

triple	notation	minimum value	typical value	maximum values	unit (of measure)
clock cycle	Tck	10.66		170.56	ns

triple	notation	minimum value	typical value	maximum values	unit (of measure)
Clock High Level Period	Tck_h	5.33		85.28	ns
Clock Low Level Period	Tck_l	5.33		85.28	ns
Output CS Establishment Time	Tcs_su	10.66			ns
Output CS Hold Time	Tcs_hd	10.66			ns
Output signal delay	Tq_vld	-1.00		2.00	ns

2.6.3 VI Interface Timing

The VI interface timing is shown in Figure 2-10.

Figure *2-10 VI* Interface Timing Diagram

The VI interface timing parameters are shown in Table 2-32.

Table *2-32 VI* Interface Timing Parameter Table

	Symbol	Min	Typ	Max.	Unit
VICLK clock cycle	T	6.73			ns
VIDATA setup time	Tsu	1.9			ns
VIDATA hold time	Thd	0.8			ns

2.6.4 VO Interface Timing

The VO interface timing is shown in Figure 2-11.

Figure *2-11 VO* Interface Timing Diagram

where the VO interface timing parameters are shown in Table 2-33.

Table 2-33 VO Interface Timing Parameter Table

	Symbol	Min	Typ	Max.	Unit
VOCLK clock cycle	T		6.73		ns
VODATA delay time	Tov	T/2-1.5		T/2+1.5	ns

Figure 2-12 BT.656 Interface Timing Chart

Figure 2-13 BT.601 Interface Timing Chart

Figure 2-14 BT.1120 Interface Timing Chart

Figure *2-15 8080* Interface Timing Diagram

2.6.5 AIAO (I2S/PCM) Interface Timing

The external Audio Codec, I2S mode and PCM mode interface receive timing is shown in Figure 2-16.

Figure *2-16 I2S & PCM* Interface Receive Timing Chart

The I2S mode and PCM mode interface transmit timing is shown in Figure 2-17.

Figure *2-17 I2S & PCM* Interface Transmission Timing Chart

The interface timing parameters are shown in Table 2-34.

Table *2-34 I2S/PCM* Interface Timing Parameter Table

notation	parameters	minimum value	typical value	maximum values	unit (of measure)
TBL	BCLK Low Quasi-Pulse Width (Master and Slave Modes)	40	-	-	ns
TBH	BCLK high level quasi-pulse width (master and slave modes)	40	-	-	ns
TLS	Establishment time of LRCK relative to rising edge of BCLK (slave mode)	10	-	-	ns
TLH	LRCK hold time relative to BCLK rising edge (slave mode)	10	-	-	ns
TSS	SDI build-up time relative to BCLK rising edge (master and slave modes)	10	-	-	ns
TSH	SDI hold time relative to BCLK rising edge (master and slave modes)	10	-	-	ns
TTS	Clock skew of BCLK falling edge relative to LRCK (master mode)	0	-	10	ns
TSOD	Signal delay time of SDO relative to the falling edge of BCLK (master and slave modes)	0	-	10	ns

2.6.6 I2C Interface Timing.

Figure *2-18 I2C*

Interface Timing Diagram

Table *2-35 I2C* Interface

Timing Parameter Table

PARAMETER	SYMBOL	STANDARD-MODE		FAST-MODE		UNIT
		MIN.	MAX.	MIN.	MAX.	
SCL clock frequency	f_{SCL}	0	100	0	400	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated	$t_{HD;STA}$	4.0	–	0.6	–	µs
LOW period of the SCL clock	t_{LOW}	4.7	–	1.3	–	µs
HIGH period of the SCL clock	t_{HIGH}	4.0	–	0.6	–	µs
Set-up time for a repeated START condition	$t_{SU;STA}$	4.7	–	0.6	–	µs
Data hold time: for CBUS compatible masters (see NOTE, Section 10.1.3) for I²C-bus devices	$t_{HD;DAT}$	 5.0 0(2)	 – 3.45(3)	 – 0(2)	 – 0.9(3)	 µs µs
Data set-up time	$t_{SU;DAT}$	250	–	100(4)	–	ns
Rise time of both SDA and SCL signals	t_r	–	1000	$20 + 0.1C_b$(5)	300	ns
Fall time of both SDA and SCL signals	t_f	–	300	$20 + 0.1C_b$(5)	300	ns
Set-up time for STOP condition	$t_{SU;STO}$	4.0	–	0.6	–	µs
Bus free time between a STOP and START condition	t_{BUF}	4.7	–	1.3	–	µs
Capacitive load for each bus line	C_b	–	400	–	400	pF
Noise margin at the LOW level for each connected device (including hysteresis)	V_{nL}	$0.1V_{DD}$	–	$0.1V_{DD}$	–	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{nH}	$0.2V_{DD}$	–	$0.2V_{DD}$	–	V

2.6.7 SPI Interface Timing

Figure *2-19 SPI* Interface Timing Diagram

Table *2-36 SPI* Interface Timing Parameters.

notation	descriptive	minimum value	typical value	maximum values	unit (of measure)
Fclk	SCK Frequency		-	46.8	MHz
Tcss	CS Negative edge time from first clock edge	21.4	-	-	ns
Tclk	clock cycle	21.4	-	-	ns
Tsu	Input Signal Establishment Time Requirements	9.5	-	-	ns

Thd	Input Signal Hold Time Requirements	0	-	-	ns
Tov	Effective delay time of output signal	-	-	3	ns
TOX	Output signal hold time	-3	-	-	ns

2.6.8 MIPI Rx Interface Timing

The speed range for MIPI Rx is 0.08Gbps ≤ data speed ≤ 1.5Gbps.

A.0.08Gbps ≤ data speed ≤ 1.5Gbps

The timing diagram is shown in Figure 2-20 and the timing parameters are shown in Table 2-37.

Figure *2-20*. Clock Data Timing Diagram of *MIPI Rx at 0.08Gbps* ≤ Data Speed ≤ *1.5Gbps* Table *2-37* Timing Parameter Table of *MIPI Rx at 0.08Gbps* ≤ Data Speed ≤ *1.5Gbps*

參數	符號	資料速度區間	最小值	典型值	最大值	單位
資料速度	Data Rate	0.08G≤Data Rate≤1G	0.08		1	Gbps
		1G<Data Rate≤1.5G	1		1.5	
差分時鐘週期	Tclk	0.08G≤Data Rate≤1G	2		25	ns
		1G<Data Rate≤1.5G	1.33		2	
發射端資料到時鐘歪斜時間	T_{SKEW}	0.08G≤Data Rate≤1G	-0.15		0.15	UIHS *
		1G<Data Rate≤1.5G	-0.2		0.2	
接收端差分時鐘建立時間	T_{SETUP}	0.08G≤Data Rate≤1G	0.15			UIHS
		1G<Data Rate≤1.5G	0.2			
接收端差分時鐘保持時間	T_{HOLD}	0.08G≤Data Rate≤1G	0.15			UIHS
		1G<Data Rate≤1.5G	0.2			

* UIHS= 1/資料速度 = 差分時鐘週期/2

2.6.9 Sub-LVDS Interface Timing

The Sub-LVDS clock data timing diagram is shown in Figure 2-21, and the timing parameters are shown in Table 2-38.

Figure 2-21. *Sub-LVDS* Clock Data

Timing Diagram Table *2-38*.

參數	符號	最小值	典型值	最大值	單位
資料速度	Data Rate	--	--	1.5	Gbps
位元標準時間	UI	666.6	--	--	ns
差分時鐘週期	Tclk	1333.3	--	--	ns
接收端差分時鐘建立時間	T_{SETUP}	0.15	--	--	UI
接收端差分時鐘保持時間	T_{HOLD}	0.15	--	--	UI
Differential Input Threshold Voltage (VP－VM)	VIDTH(SL)	-70	--	70	mV

* UI= 1/資料速度 = 差分時鐘週期/2

2.6.10 HiSPi Interface Timing

The HiSPi clock data timing diagram is shown in Figure 2-22, and the timing parameters are shown in Table 2-39.

Figure 2-22. *HiSPi* Clock Data

Timing Chart Table *2-39*.

參數	符號	最小值	典型值	最大值	單位
資料速度	Data Rate	--	--	1.5	Gbps
位元標準時間	UI	666.6	--	--	ns
差分時鐘週期	Tclk	1333.3	--	--	ns
接收端差分時鐘建立時間	T_{SETUP}	0.15	--	--	UI
接收端差分時鐘保持時間	T_{HOLD}	0.15	--	--	UI
Differential Input Threshold Voltage (VP－VM)	VIDTH(HSSL)	-70	--	70	mV
	VIDTH(HSHI)	-100	--	100	

* UI= 1/資料速度 = 差分時鐘週期/2

2.6.11 MIPI Tx Interface Timing

Figure 2-23 *MIPI TX* Interface Data Pair Clock Timing Chart

Form 2-40 *Data-Clock Timing Specifications for 0.08Gbps and 1 Gbps*

Symbol	Description	Min	Nom	Max.	Units	Notes
TSKEW[TX]	TX Data to Clock Skew	-0.15		0.15	UIHS	

Form 2-41 *Data-Clock Timing Specifications for > 1Gbps and 1 .5 Gbps*

Symbol	Description	Min	Nom	Max.	Units	Notes
TSKEW[TX]	TX Data to Clock Skew	-0.2		0.2	UIHS	

Form 2-42 *Data-Clock Timing Specifications for > 1.5 Gbps and 2 .5 Gbps*

Symbol	Description	Min	Nom	Max.	Units	Notes
TSKEW[TX]	TX Data to Clock Skew	-0.2		0.2	UIHS	
TJTX	TX Data to Clock Total Jitter			0.3	UIHS	
DJTX	TX Data to Clock Deterministic Jitter			0.2	UIHS	
RJTX	TX Data to Clock Random Jitter			0.1	UIHS	

Figure *2-24 TX EYE Diagram Specification*

Table *2-43 Transmitter Eye Diagram Specification*

Bit Error Rate	TEYE_TX	VDIF_TX
10^{-12}	0.5UI	40mV
10^{-6} (Prorated for Validation)	0.53UI	47mV

Figure *2-25 Transmitter Eye Diagram Validation Setup*

2.6.12 SDIO/MMC Interface Timing

The data input/output direction timing for a single edge is shown in Figure 2-26.

Figure 2-26 Data Input/Output Timing Diagram for *SDIO/MMC* Single Edge *(SDR)*.

Table *2-44 SDIO/MMC* single-edge *DS (default speed)* mode timing parameter table

parameters	notation	minimum value	typical value	maximum values	unit (of measure)	note
Clock CLK						
Clock frequency Data transfer Mode	fPP	0	-	26	MHz	fpp=1/tpp CL≤30pF
Clock frequenyc Idenfification Mode	fOD	0	-	400	KHz	CL≤30pF
Clock high time	tWH	10	-	-	ns	CL≤30pF
Clock low time	tWL	10	-	-	ns	CL≤30pF

Clock rise time	tTLH	-	-	10	ns	CL≤30pF
Clock fall time	tTHL	-	-	10	ns	CL≤30pF
Inputs CMD, DAT (referred to CLK)						
Input set-up time	tISU	6	-	-	ns	CL≤30pF
Input hold time	tIH	8.3	-	-	ns	CL≤30pF
Outputs CMD, DAT (referenced to CLK)						

parameters	notation	minimum value	typical value	maximum values	unit (of measure)	note
Output set-up time	tOSU	5	-	-	ns	CL≤30pF
Output hold time	tOH	5	-	-	ns	CL≤30pF

Table *2-45 SDIO/MMC* Single Edge *HS (High speed)* Mode Timing Parameter Table

parameters	notation	minimum value	typical value	maximum values	unit (of measure)	note
Clock CLK						
Clock frequency Data transfer Mode	fpp	0	-	52	MHz	fpp=1/tpp CL≤30pF
Clock high time	tWH	6.5	-	-	ns	CL≤30pF
Clock low time	tWL	6.5	-	-	ns	CL≤30pF
Clock rise time	tTLH	-	-	3	ns	CL≤30pF
Clock fall time	tTHL	-	-	3	ns	CL≤30pF
Inputs CMD, DAT (referred to CLK)						
Input set-up time	tISU	6	-	-	ns	CL≤30pF
Input hold time	tIH	2.5	-	-	ns	CL≤30pF
Outputs CMD, DAT (referenced to CLK)						
Output set-up time	tOSU	6	-	-	ns	CL≤30pF
Output hold time	tOH	3	-	-	ns	CL≤30pF

The data input/output direction timing of the double edge is shown in Figure 2-27.

m

n (VIH)

i

max (VIL)

Figure *2-27* Timing Diagram of Data Input/Output Direction of *SDIO/MMC* Dual Edge *DDR50* Mode

Table *2-46 SDIO/MMC* Dual Edge *DDR50* Mode Timing Parameter Table

parameters	notation	minimal (be) worth	typical value	greatest (be) worth	unit (of measure)	note
Clock CLK						
Clock frequency Data transfer Mode	fP	0	-	52	MHz	fpp=1/tpp CL≤30pF
Inputs DAT (referenced to CLK)						
Input delay time during data transfer	tIDLYddr	1.5	-	7	ns	CL≤20pF
Outputs DAT (referenced to CLK)						
Output set-up time	tOSU	3	-	-	ns	CL≤20pF
Output hold time	tOH	2.5	-	-	ns	CL≤20pF

The data input and output direction timing of HS200 and SDR104 is shown in Figure 2-28.

Figure *2-28* Data Command Output Direction Timing Diagram for

parameters	notation	minimal (be) worth	typical value	maximum values	unit (of meas	note

Parameter Table for *SDIO/MMC HS200* and *SDR104* Modes

Table *2-47* Output *SDIO/MMC HS200* and *SDR104* Modes

parameters	notation	minimal (be) worth	typical value	maximum values	unit (of measure)	note
Output hold time	tOH	0.8	-	-	ns	

Table *2-48 SDIO/MMC HS200* a n d *SDR104* Mode Input Timing Parameter Table

parameters	notation	minimum value	typical value	maximum values	unit (of measure)	note
Phase difference between device TX CMD/DAT and RX CLK	tPH	0	-	2	UI	Unit Interval (UI) is one bit nominal time. For 200Mhz, UI=5ns
Input valid data window	tVW	0.575	-	-	UI	TVW=2.88ns at 200MHz