*SAMPLE INFORMATION*

PRODUCT: SHI

DEVICE TYPE: EKTA0200

LOT NO: J434Q

Testing Date: 2020/08/21

測試檢驗項目(Testing/Inspection Items)

## 1. ESD Test

HBM: PASS (2KV)

## 2. Latch-up Test

Non-power pin: PASS (400mA)

Power pin: PASS (2*Vmax)

| APPROVED BY: | CHECK BY: | Original: |
|---|---|---|
| 詹建文 | 李青青 | 吳吉順 |

## 1. ESD Test

### 1.1 Purpose:

Electrostatic discharge sensitivity tests are designed to measure the sensitivity of each device pin to electrostatic discharges that may occur during device handling.

### 1.2 Test Instrument:

Keytek ESD Auto Tester Zapmaster

### 1.3 Test Method:

(1) Human Body Model(HBM), refer to MIL-STD-883H Method 3015.8:
Charge built up on the human body is discharged when a part of the body touches a pin of the device. The device is damaged by discharged current if a pin of the device is grounded.

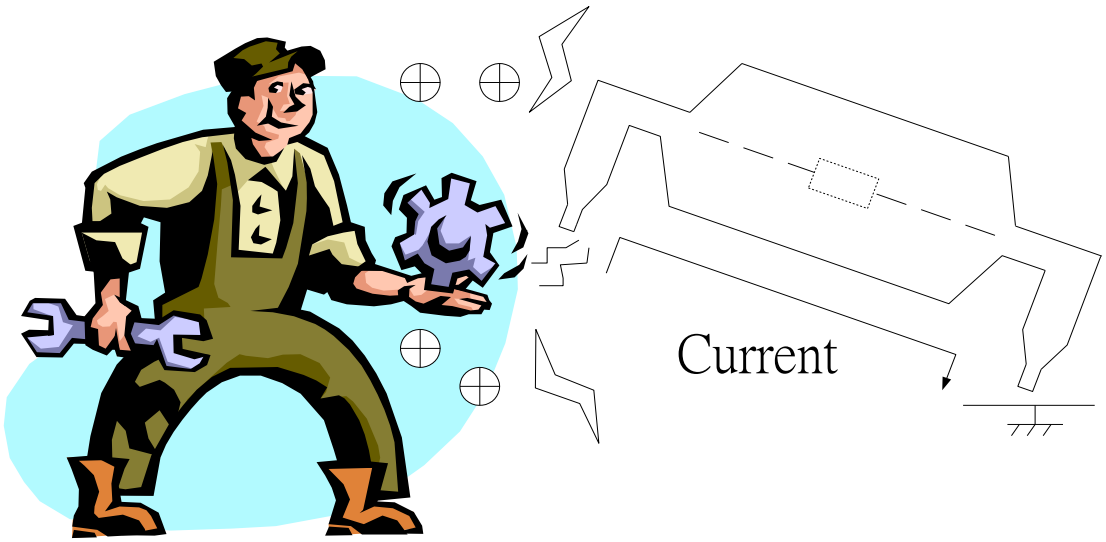
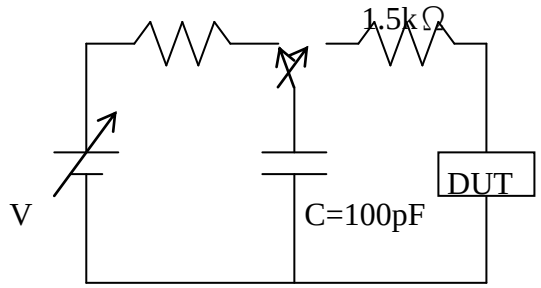



Fig. 1 Human Body Model (HBM)

**1.4 Test Circuit:**




(1) HBM

**1.5 Test Condition:**

1.5.1 HBM:

- HBM stresses devices by sudden application of a high voltage supplied by a 100pf capacitor through 1.5Kohms resistance. 3 pulses (Zapping interval 1 sec) are used with respect to Vdd, Vss, and all other pins.
- Voltage Stress, From ±1000V to ±4000V, step ±1000V

**1.6 Record:**

(1) Test results are the step before the failure.

(2) Owing to the Elan's criterion is HBM≧2KV, so the test would be stopped at HBM : 2KV, if there are any test mode fail before it.

**1.7 Test Results:** (See page 8,9)

## 2. Latch-up Test (Static)

### 2.1 Purpose:

The latch-up test is special test used with CMOS processes to detect parasitic bipolar circuits that can short the power and ground nodes when they are activated, Elan adopts JEDEC-JC-78C standards: The current is applied to each I/O pin in steps while the power supply current is monitored . The current into the test pin must rise to a minimum of 100 mA without latch-up occurring

### 2.2 Test Instrument:

Keytek Auto Tester Zapmaster

### 2.3 Test Method:

Refer to JEDEC 78C

### 2.4 Test Condition:

- Zapmaster is used to source or sink current from a device pin while Icc is monitored. The forcing currents and voltages required to initiate latch-up is measured for each device pin.
- Current Trigger (Non-power pin):
  2.4.1 Positive trigger: From 50mA to 400mA, step 50mA
  2.4.2 Negative trigger: From -50mA to -400mA, step –50mA
- A device will be considered to have failed latch-up test if the Icc, after pulsing current or voltage, exceed the 1.4 times respect to Inormal, measured before pulsing.

### 2.5 Record:

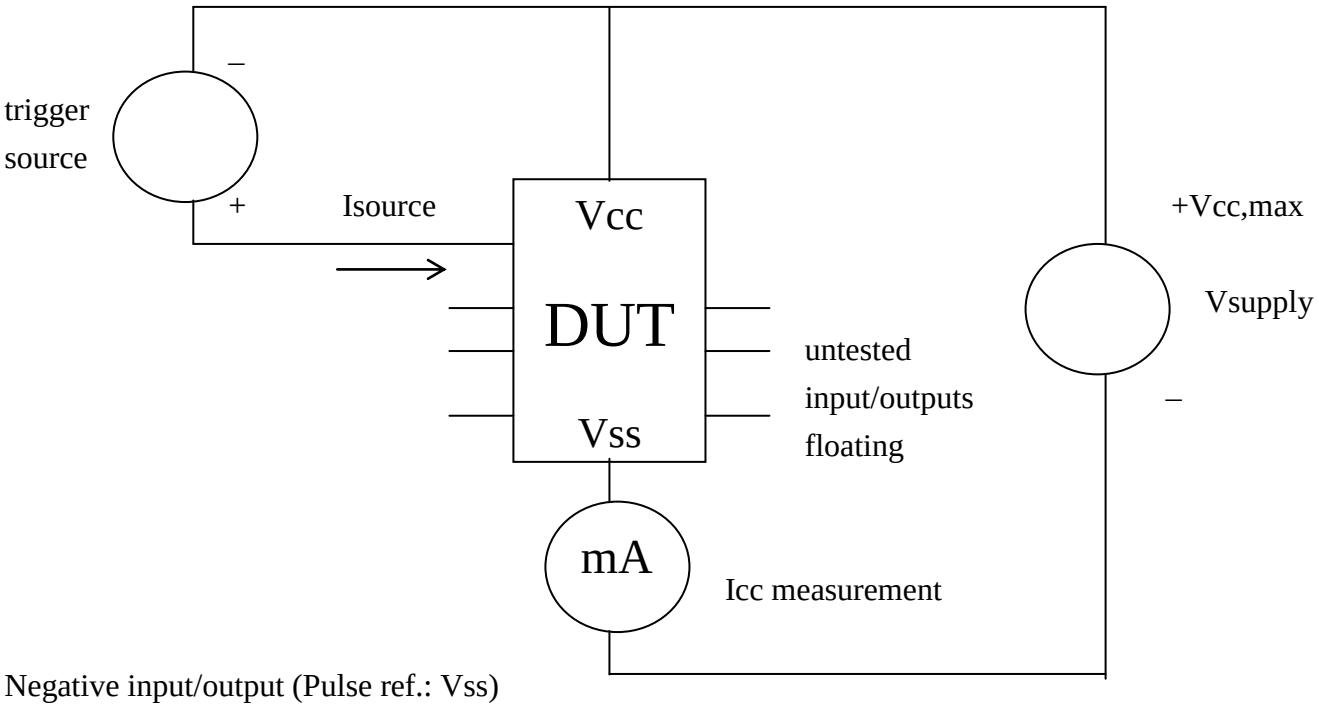
The results are the step before the failure.

**2.6 Test Circuit:** (See page 6,7)

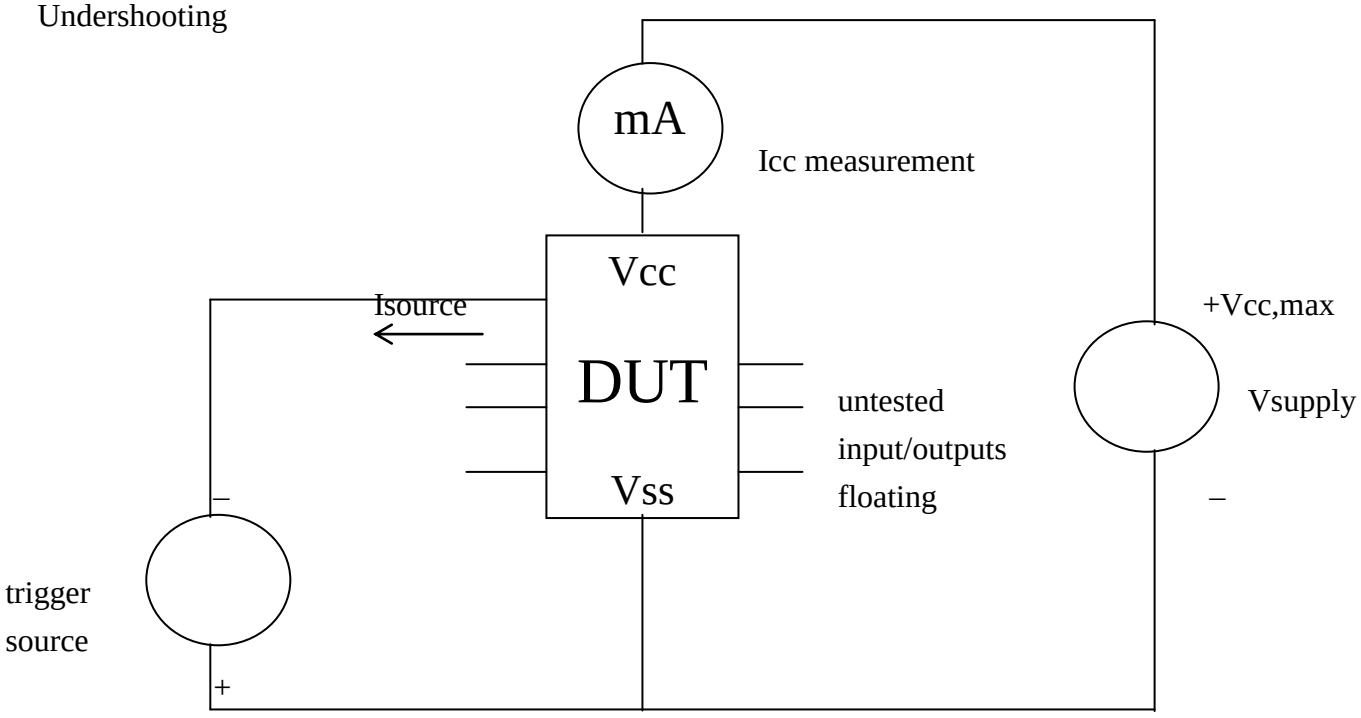
**2.7 Test Results:** (See page 9)

- **Input/Output Over-current Test**

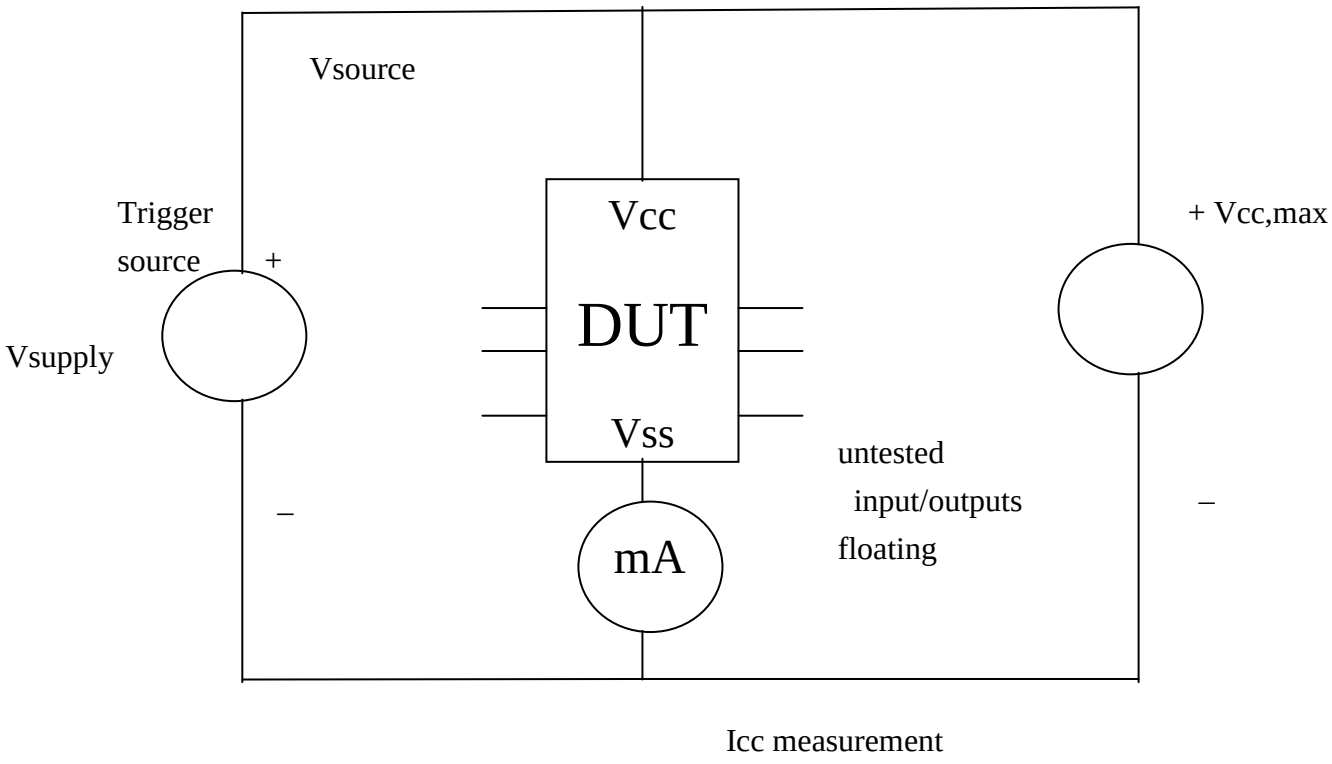
Positive input/output (Pulse ref.: Vcc)
Overshooting




Negative input/output (Pulse ref.: Vss)
Undershooting



Power pin (Pulse ref.: Vss)
Overshooting




Icc measurement

**3. Test Results:**

➢ ESD:

(1) Human Body Model

(Unit: Volt)

| Test Mode | PASS ESDV | | | | Remark |
|---|---|---|---|---|---|
| | PIN | #1 | #2 | #3 | |
| ND | IO | ≧4KV | ≧4KV | ≧4KV | |
| NS | IO | ≧4KV | ≧4KV | ≧4KV | |
| PD | IO | ≧4KV | ≧4KV | ≧4KV | |
| PS | IO | 2KV | 2KV | ≧4KV | |
| VDD-VSS(-) | VDD | ≧4KV | ≧4KV | ≧4KV | |
| VDD-VSS(+) | VDD | ≧4KV | ≧4KV | ≧4KV | |
| VDD-VDD(-) | VDD | ≧4KV | ≧4KV | ≧4KV | |
| VDD-VDD(+) | VDD | ≧4KV | ≧4KV | ≧4KV | |

- Latch-up:

| Pin Group | Mode | Pass current/voltage | Remark |
|---|---|---|---|
| Input/output | I＋ | ≧400mA | |
| | I－ | ≧400mA | |
| Power | V＋ | ≧2*Vmax | |