Alexander Phillips

■ alexander@keemail.me | 🛘 (765) 543 9657 | 🕈 San Jose, California | 🗞 alexphillips.xyz

Education _____

University of Leicester MS IN COMPUTER SCIENCE

Leicester, England, UK

Aug 2017 - Present

Purdue University

West Lafayette, Indiana, USA

BS IN COMPUTER ENGINEERING, MINOR IN PHYSICS

Aug 2010 - Dec 2015

Experience _____

Jabil Circuit Inc.

San Jose, California

TEST ENGINEER II Apr 2016 - Present

- Designed and built the infrastructure for automated testing of the customer's Enterprise Emulation Platform in Python, Bash and C shell on the GNU + Linux command line.
- Wrote tests for the customer's Enterprise Emulation Platform to ensure quality and maintained the tests with updates.
- Developed and launched a data parser in Python for collection and upload of test results into Jabil's MES system.
- Suggested, designed and implemented a neural network to identify human errors on the manufacturing floor.
- Developed a visual test progress monitor in Python which is now on display on the manufacturing floor.
- · Determined design flaws for individual customer FRUs and worked with the customers to ensure that the issues are closed.
- Developed scripts to analyze performance and telemetric data of customer products.

Purdue University Physics Department

West Lafayette, Indiana

Undergraduate Research Assistant

Aug 2013 - Aug 2014

• Developed and implemented methods using data received from XENON100 detector to determine possible Dark Matter interaction. Also set up and created hardware to work with neutron generator.

Skills

Programming Languages: Python, C, Go, Bash, Matlab, Assembly (Motorola HCS12), Java

Hardware Description Languages: System Verilog, ABEL Web Development: HTML5, CSS, Javascript

Software: Catia, AutoCAD, ModelSim, QuestaSim, Eagle, GNU + Linux Operating System

Certifications: Qualified Sealed Radioactive Source Handler, LEAN Bronze

Projects _____

32-bit MIPS Microprocessor

System Verilog

DESIGNED FROM SCRATCH AS A SINGLE CYCLE, PIPELINE AND EVENTUALLY MULTICORE STRUCTURE. https://github.com/Tatsuonline/ECE-437

Micro Programming Language Compiler

https://github.com/Tatsuonline/Micro-

UTILIZED ANTLR TO CREATE A COMPILER FOR THE MICRO PROGRAMMING LANGUAGE.

Compiler

Scintillator-Photomultiplier Output Pulse Discriminator

Python, System Verilog

USES ALGORITHMS DESIGNED IN PYTHON AND IMPLEMENTED IN SYSTEM VERILOG TO PERFORM PULSE SHAPE DISCRIMINATION ON NEUTRON AND GAMMA RECOILS IN SCINTILLATORS.

https://github.com/Tatsuonline/Dark-

Matter-Research

Awards _____

Jun 2017	Jabil Star Award Recepient , Recognized for contributions to the company, directly leading to	Jabil Circuit Inc.
	revenue increases.	Jubii Circuit iric.
May 2018	Jabil Respect, Recognize, Reward Recepient , Contributions to the company were recognized	Jabil Circuit Inc.
	and honoured on the Jabil website.	

1st First Place Winner: Continental Jabil Best Practices Competition, Submitted project won Nov 2018

Jabil Circuit Inc.

first place in the competition to improve efficiency.