1. Description

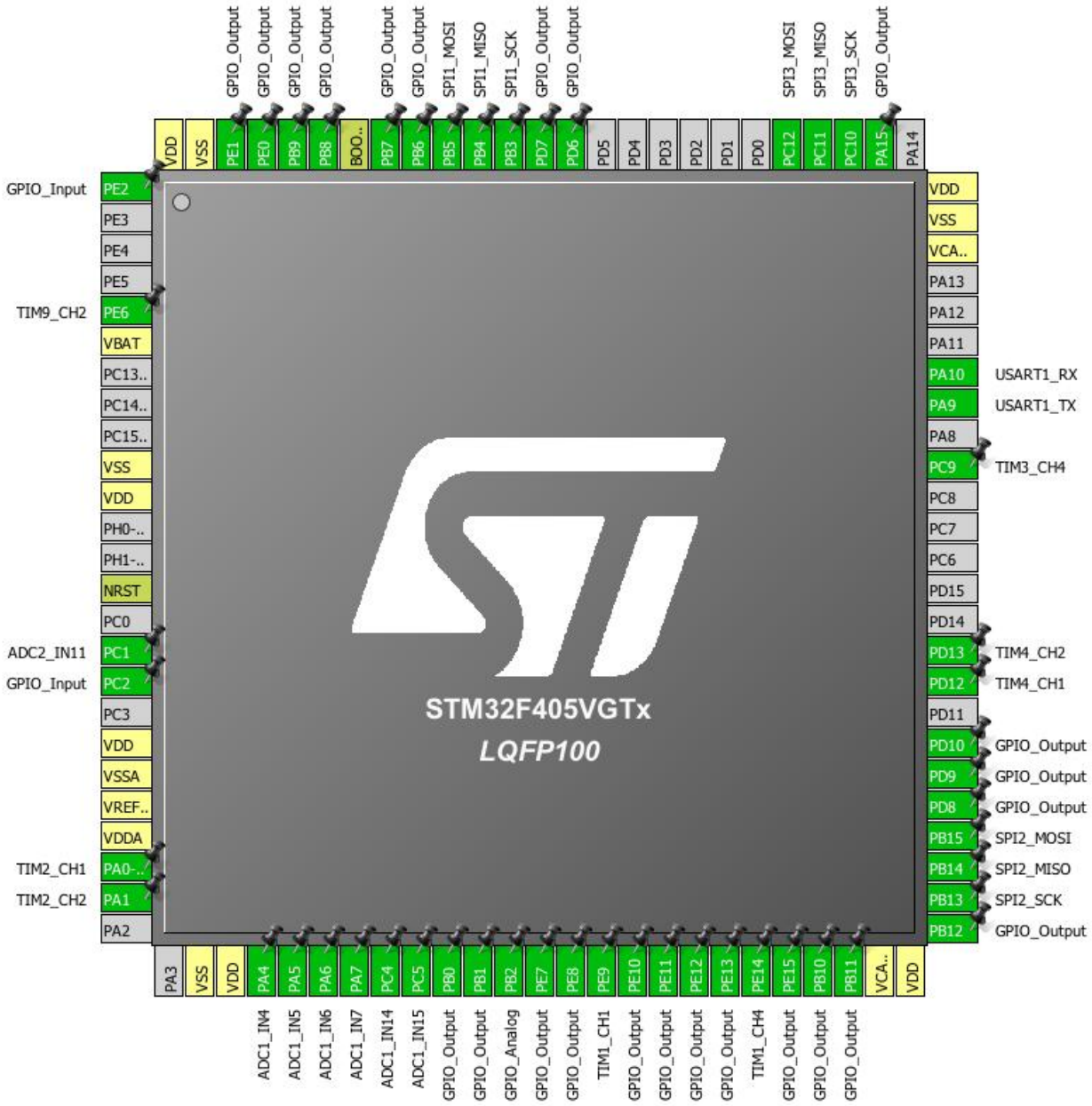
1.1. Project

Project Name	pimelodia_line
Board Name	pimelodia_line
Generated with:	STM32CubeMX 4.22.0
Date	02/12/2018

1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F405/415
MCU name	STM32F405VGTx
MCU Package	LQFP100
MCU Pin number	100

2. Pinout Configuration



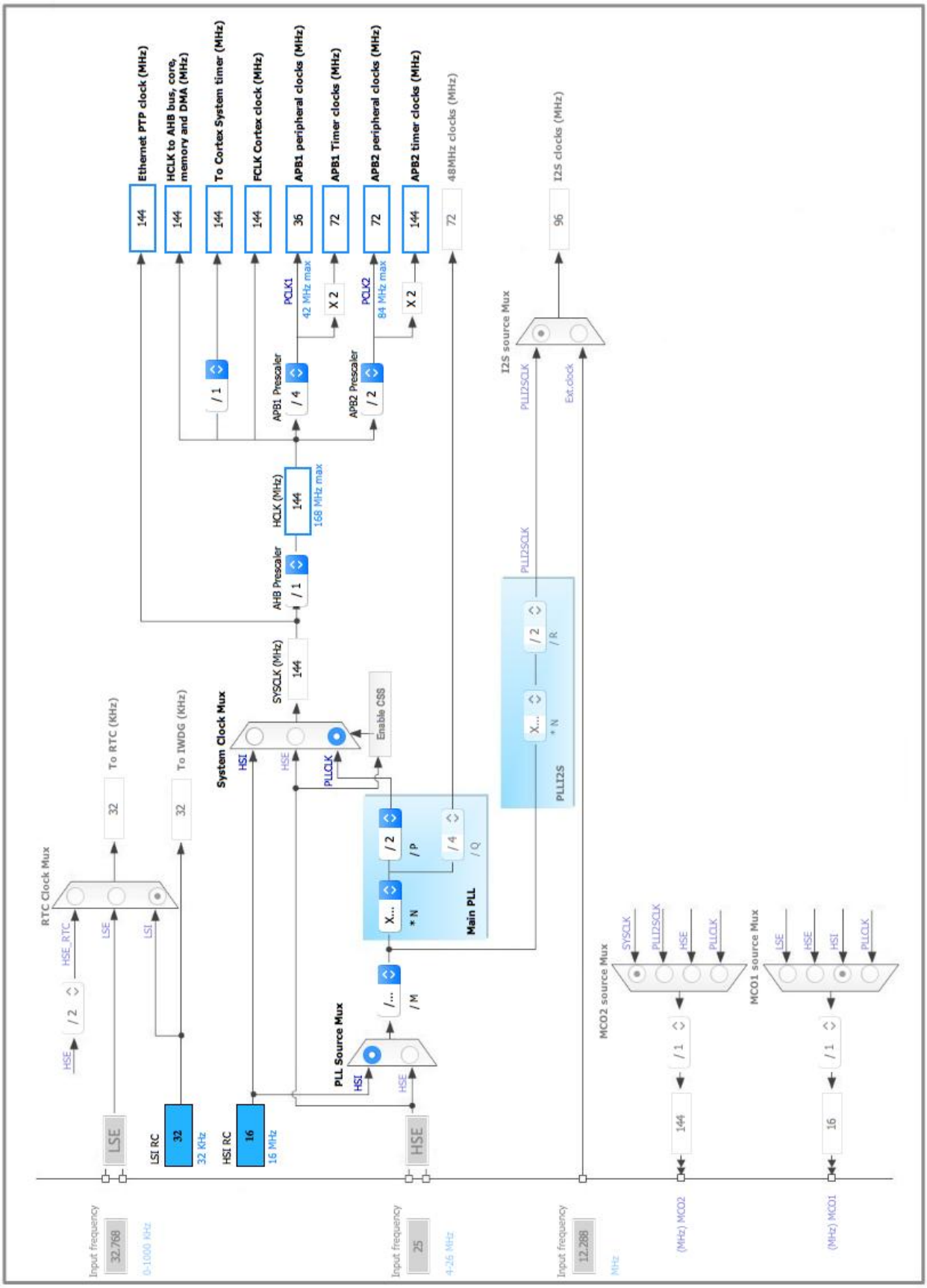
3. Pins Configuration

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	PE2 *	I/O	GPIO_Input	
5	PE6	I/O	TIM9_CH2	
6	VBAT	Power		
10	VSS	Power		
11	VDD	Power		
14	NRST	Reset		
16	PC1	I/O	ADC2_IN11	
17	PC2 *	I/O	GPIO_Input	
19	VDD	Power		
20	VSSA	Power		
21	VREF+	Power		
22	VDDA	Power		
23	PA0-WKUP	I/O	TIM2_CH1	
24	PA1	I/O	TIM2_CH2	
27	VSS	Power		
28	VDD	Power		
29	PA4	I/O	ADC1_IN4	
30	PA5	I/O	ADC1_IN5	
31	PA6	I/O	ADC1_IN6	
32	PA7	I/O	ADC1_IN7	
33	PC4	I/O	ADC1_IN14	
34	PC5	I/O	ADC1_IN15	
35	PB0 *	I/O	GPIO_Output	
36	PB1 *	I/O	GPIO_Output	
37	PB2 *	I/O	GPIO_Analog	
38	PE7 *	I/O	GPIO_Output	
39	PE8 *	I/O	GPIO_Output	
40	PE9	I/O	TIM1_CH1	
41	PE10 *	I/O	GPIO_Output	
42	PE11 *	I/O	GPIO_Output	
43	PE12 *	I/O	GPIO_Output	
44	PE13 *	I/O	GPIO_Output	
45	PE14	I/O	TIM1_CH4	
46	PE15 *	I/O	GPIO_Output	
47	PB10 *	I/O	GPIO_Output	
48	PB11 *	I/O	GPIO_Output	

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
49	VCAP_1	Power		
50	VDD	Power		
51	PB12 *	I/O	GPIO_Output	
52	PB13	I/O	SPI2_SCK	
53	PB14	I/O	SPI2_MISO	
54	PB15	I/O	SPI2_MOSI	
55	PD8 *	I/O	GPIO_Output	
56	PD9 *	I/O	GPIO_Output	
57	PD10 *	I/O	GPIO_Output	
59	PD12	I/O	TIM4_CH1	
60	PD13	I/O	TIM4_CH2	
66	PC9	I/O	TIM3_CH4	
68	PA9	I/O	USART1_TX	
69	PA10	I/O	USART1_RX	
73	VCAP_2	Power		
74	VSS	Power		
75	VDD	Power		
77	PA15 *	I/O	GPIO_Output	
78	PC10	I/O	SPI3_SCK	
79	PC11	I/O	SPI3_MISO	
80	PC12	I/O	SPI3_MOSI	
87	PD6 *	I/O	GPIO_Output	
88	PD7 *	I/O	GPIO_Output	
89	PB3	I/O	SPI1_SCK	
90	PB4	I/O	SPI1_MISO	
91	PB5	I/O	SPI1_MOSI	
92	PB6 *	I/O	GPIO_Output	
93	PB7 *	I/O	GPIO_Output	
94	BOOT0	Boot		
95	PB8 *	I/O	GPIO_Output	
96	PB9 *	I/O	GPIO_Output	
97	PE0 *	I/O	GPIO_Output	
98	PE1 *	I/O	GPIO_Output	
99	VSS	Power		
100	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. IPs and Middleware Configuration

5.1. ADC1

mode: IN4

mode: IN5

mode: IN6

mode: IN7

mode: IN14

mode: IN15

5.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	**PCLK2 divided by 8 ***
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	**Enabled ***
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	**EOC flag at the end of all conversions ***

ADC_Regular_ConversionMode:

Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 4
Sampling Time	3 Cycles
Rank	**2 ***
Channel	**Channel 5 ***
Sampling Time	3 Cycles
Rank	**3 ***
Channel	Channel 4
Sampling Time	3 Cycles
Rank	**4 ***

Channel	Channel 4
Sampling Time	3 Cycles
Rank	**5 ***
Channel	Channel 4
Sampling Time	3 Cycles
Rank	**6 ***
Channel	Channel 4
Sampling Time	3 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

5.2. ADC2

mode: IN11

5.2.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	**PCLK2 divided by 8 ***
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 11
Sampling Time	3 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

5.3. SPI1

Mode: Full-Duplex Master

5.3.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	8 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**4 ***
Baud Rate	**18.0 MBits/s ***
Clock Polarity (CPOL)	**High ***
Clock Phase (CPHA)	**2 Edge ***

Advanced Parameters:

CRC Calculation	Disabled
NSS Signal Type	Software

5.4. SPI2

Mode: Full-Duplex Master

5.4.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	8 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	**18.0 MBits/s ***
Clock Polarity (CPOL)	**High ***
Clock Phase (CPHA)	**2 Edge ***

Advanced Parameters:

CRC Calculation	Disabled
NSS Signal Type	Software

5.5. SPI3

Mode: Full-Duplex Master

5.5.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	8 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	**18.0 MBits/s ***
Clock Polarity (CPOL)	**High ***
Clock Phase (CPHA)	**2 Edge ***

Advanced Parameters:

CRC Calculation	Disabled
NSS Signal Type	Software

5.6. SYS

Timebase Source: SysTick

5.7. TIM1

Channel1: PWM Generation CH1
Channel4: PWM Generation CH4

5.7.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**1 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**500 ***

Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

PWM Generation Channel 4:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

5.8. TIM2

Combined Channels: Encoder Mode

5.8.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	**65535 ***
Internal Clock Division (CKD)	No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Encoder:

Encoder Mode	**Encoder Mode TI1 and TI2 ***
____ Parameters for Channel 1 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	**5 ***
____ Parameters for Channel 2 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	**5 ***

5.9. TIM3

Channel4: PWM Generation CH4

5.9.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**10 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**100 ***
Internal Clock Division (CKD)	No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 4:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

5.10. TIM4

Combined Channels: Encoder Mode

5.10.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**65535 ***
Internal Clock Division (CKD)	No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Encoder:

Encoder Mode	**Encoder Mode TI1 and TI2 ***
____ Parameters for Channel 1 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	**5 ***
____ Parameters for Channel 2 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	**5 ***

5.11. TIM5

mode: Clock Source

5.11.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**3600 ***
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	**1 ***
Internal Clock Division (CKD)	No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

5.12. TIM6

mode: Activated

5.12.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**36000 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**1 ***

Trigger Output (TRGO) Parameters:

Trigger Event Selection	Reset (UG bit from TIMx_EGR)

5.13. TIM7

mode: Activated

5.13.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**36000 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**1 ***

Trigger Output (TRGO) Parameters:

Trigger Event Selection	Reset (UG bit from TIMx_EGR)

5.14. TIM9

Channel2: PWM Generation CH2

5.14.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**120 ***
Counter Mode	Up

Counter Period (AutoReload Register - 16 bits value)	**100 ***
Internal Clock Division (CKD)	No Division

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

5.15. USART1

Mode: Asynchronous

5.15.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

*** User modified value**

6. System Configuration

6.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA4	ADC1_IN4	Analog mode	No pull-up and no pull-down	n/a	
	PA5	ADC1_IN5	Analog mode	No pull-up and no pull-down	n/a	
	PA6	ADC1_IN6	Analog mode	No pull-up and no pull-down	n/a	
	PA7	ADC1_IN7	Analog mode	No pull-up and no pull-down	n/a	
	PC4	ADC1_IN14	Analog mode	No pull-up and no pull-down	n/a	
	PC5	ADC1_IN15	Analog mode	No pull-up and no pull-down	n/a	
ADC2	PC1	ADC2_IN11	Analog mode	No pull-up and no pull-down	n/a	
SPI1	PB3	SPI1_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PB4	SPI1_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PB5	SPI1_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
SPI2	PB13	SPI2_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PB14	SPI2_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PB15	SPI2_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
SPI3	PC10	SPI3_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PC11	SPI3_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PC12	SPI3_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
TIM1	PE9	TIM1_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE14	TIM1_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM2	PA0-WKUP	TIM2_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA1	TIM2_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM3	PC9	TIM3_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM4	PD12	TIM4_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD13	TIM4_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
TIM9	PE6	TIM9_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USART1	PA9	USART1_TX	Alternate Function Push Pull	Pull-up	**Very High ***	
	PA10	USART1_RX	Alternate Function Push Pull	Pull-up	**Very High ***	
GPIO	PE2	GPIO_Input	Input mode	**Pull-down ***	n/a	
	PC2	GPIO_Input	Input mode	**Pull-down ***	n/a	
	PB0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB2	GPIO_Analog	Analog mode	No pull-up and no pull-down	n/a	
	PE7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PE8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PE10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PE11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PE12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PE13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PE15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PD8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PD9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PD10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PA15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PD6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PD7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PE0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PE1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	

6.2. DMA configuration

DMA request	Stream	Direction	Priority
ADC1	DMA2_Stream0	Peripheral To Memory	**High ***

ADC1: DMA2_Stream0 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

6.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
ADC1, ADC2 and ADC3 global interrupts	true	0	0
TIM2 global interrupt	true	0	0
TIM4 global interrupt	true	0	0
SPI1 global interrupt	true	0	0
SPI2 global interrupt	true	0	0
TIM5 global interrupt	true	0	0
SPI3 global interrupt	true	0	0
TIM6 global interrupt, DAC1 and DAC2 underrun error interrupts	true	0	0
TIM7 global interrupt	true	0	0
DMA2 stream0 global interrupt	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
TIM1 break interrupt and TIM9 global interrupt	unused		
TIM1 update interrupt and TIM10 global interrupt	unused		
TIM1 trigger and commutation interrupts and TIM11 global interrupt	unused		
TIM1 capture compare interrupt	unused		
TIM3 global interrupt	unused		
USART1 global interrupt	unused		
FPU global interrupt	unused		

*** User modified value**

7. Power Consumption Calculator report

7.1. Microcontroller Selection

Series	STM32F4
Line	STM32F405/415
MCU	STM32F405VGTx
Datasheet	022152_Rev8

7.2. Parameter Selection

Temperature	25
Vdd	3.3

8. Software Project

8.1. Project Settings

Name	Value
Project Name	pimelodia_line
Project Folder	/Users/tattaka/Documents/workspace/pimelodia_liner_1_5
Toolchain / IDE	Makefile
Firmware Package Name and Version	STM32Cube FW_F4 V1.16.0

8.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No