# A Simulation Circuit to Characterize Transistors

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***Abstract*—I present a simple simulation schematic to extract transistor parameters relevant for analog circuit design: transconductance $g_m$, transconductance per current $g_m/I_d$, and voltage gain $g_m/g_o$.**

***Keywords*-SPICE, LT spice, MOSFET, process characterization, $g_m/I_d$ design method**

## I. The Circuit

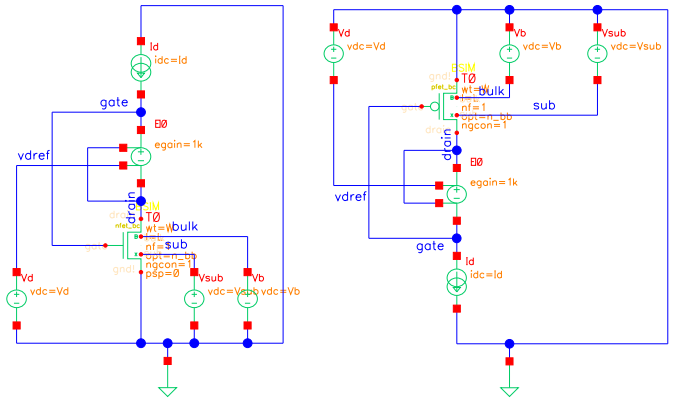


Fig. 1. Simulation schematics to characterize MOSFETs

The main design parameters for dimensioning MOSFETs are their drain current $I_d$, which controls transconductance, and the drain-to-source voltage $V_{ds}$, which controls output conductance $g_o$. However, the operating point of the transistor is controlled mostly by the gate-to-source voltage $V_{gs}$.

I solve this by regulating the gate voltage by a feedback loop that adjusts $V_g$ to set the drain voltage $V_d$ to a reference $V_{d,ref}$ by an ideal voltage controlled voltage source (VCVS) with voltage gain $A$. The schematics for the NMOS and PMOS simulation circuits are shown in Figure 1.

Kirchhoff's Current Law yields the small-signal equations

$$\begin{aligned} I_d &= g_m V_g + g_o V_d \\ V_g &= V_d + A\,(V_d - V_{d,ref}) \end{aligned} \tag{1}$$

which lead to

$$V_g = \frac{I_d - g_o\,V_{d,ref}\;A/\,(1+A)}{g_m + g_o/\,(1+A)} \tag{2}$$

and

$$V_d = \frac{I_d + A\,g_m\,V_{d,ref}}{(1+A)\,g_m + g_o}\,. \tag{3}$$

In the ideal case of $A \to \infty$,

$$V_g = \frac{I_d - g_o\,V_{d,ref}}{g_m} \tag{4}$$



and

$$V_d = V_{d,ref}\,. \tag{5}$$

## II. Parameter Extraction

### A. Transconductance

The transconductance $g_m$ as function of drain current can be obtained by sweeping $I_d$ for fixed $V_d$, as

$$1/\left(\frac{\partial V_g}{\partial I_d}\right) = g_m + g_o/\,(1+A) \overset{A\to\infty}{\approx} g_m\,. \tag{6}$$

### B. $g_m/I_d$

The specific transconductance $g_m/I_d$ is a useful design parameter for setting the bias point of a transistor. $g_m/I_d$ is maximal in subthreshold operation. It is obtained by sweeping $I_d$ for fixed $V_d$ and calculating

$$1/\left(\frac{\partial V_g}{\partial I_d}\,I_d\right) = \frac{g_m + g_o/\,(1+A)}{I_d} \overset{A\to\infty}{\approx} \frac{g_m}{I_d}\,. \tag{7}$$

### C. $g_m/g_o$

While $g_m$ or $g_m/I_d$ is the most important design criterion for dimensioning a transistor, the next most important criterion is setting the output conductance $g_o$. With the circuits in Figure 1, the intrinsic voltage gain $g_m/g_o$ can be extracted by sweeping $V_{d,ref}$ for constant $I_d$.

$$-\left(\frac{\partial V_d}{\partial V_{d,ref}}\right)/\left(\frac{\partial V_g}{\partial V_{d,ref}}\right) = \frac{\frac{A\,g_m}{(1+A)g_m+g_o}}{\frac{A\,g_o}{(1+A)g_m+g_o}} = \frac{g_m}{g_o}\,. \tag{8}$$

## III. Parameter Sweeps

### A. Transconductance

Even when MOS transistor models are too complicated for hand calculations, the specific transconductance $g_m/I_d$ indicates the operating region of the transistor.

In the weak inversion region, $I_d$ is an exponential function of $V_g$,

$$I_d = I_{d0}\exp\left(\frac{q}{n\,k\,T}\,(V_g - V_t)\right) \tag{9}$$

with $V_t$ the threshold voltage, $q$ the electron charge, $k$ the Boltzmann constant, $T$ the absolute temperature, $n > 1$ a process dependent factor, and $I_{d0}$ a proportionality constant depending on geometry, so

$$\frac{g_m}{I_d} = \frac{\frac{\partial I_d}{\partial V_g}}{I_d} = \frac{\frac{q}{n\,k\,T} I_{d0}\exp\left(\frac{q}{n\,k\,T}\,(V_g - V_t)\right)}{I_{d0}\exp\left(\frac{q}{n\,k\,T}\,(V_g - V_t)\right)} = \frac{q}{n\,k\,T}\,. \tag{10}$$

In the strong inversion region, $I_d$ depends quadratically on $V_g$,

$$I_d = \frac{\kappa}{2}\,(V_g - V_t)^2 \tag{11}$$

with the threshold voltage $V_t$ and a geometry and process dependent factor $\kappa$, so

$$\frac{g_m}{I_d} = \frac{\kappa\,(V_g - V_t)}{\frac{\kappa}{2}\,(V_g - V_t)^2} = \frac{2}{V_g - V_t} \tag{12}$$

where $V_g - V_t > 2\,\frac{n\,k\,T}{q}$ for the transistor to be above weak inversion.

With a logarithmic dc sweep of $I_d$ at a given $V_d$, the transition between weak and strong inversion can be seen by $g_m/I_d$ falling from its essentially constant value for weak inversion at the onset of strong inversion. $g_m$ is obtained by taking the derivative with respect to the dc sweep variable $I_d$ of both $V_g$ and $I_d$. This is shown in LT Spice IV for two different processes (TSMC 250 nm and TSMC 180 nm) in Figures 2 and 3.

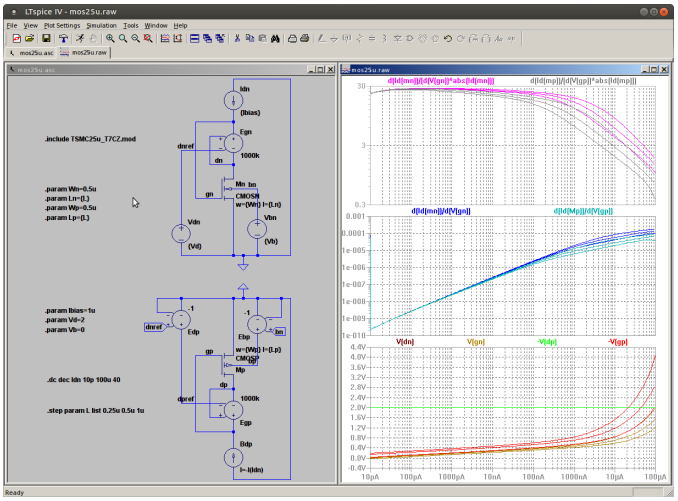

Fig. 2. Transconductance characterization for 250 nm process

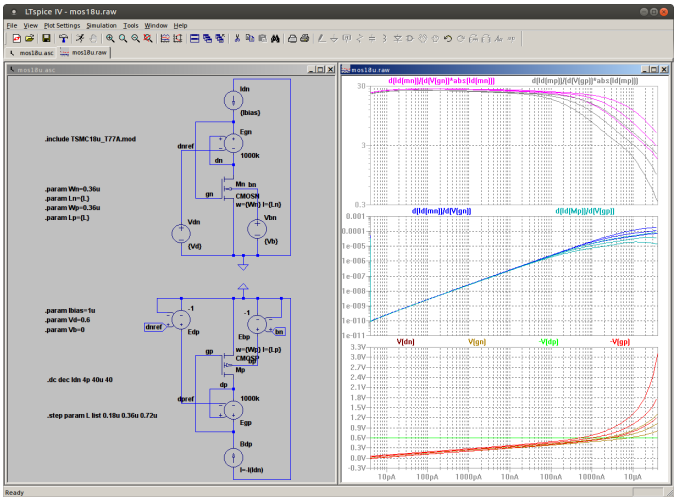

Fig. 3. Transconductance characterization for 180 nm process

For smaller $W/L$ ratios, $g_m/I_d$ starts dropping at lower $I_d$, and for the same $W/L$ ratio, the $g_m/I_d$ of PMOS transistors starts dropping at lower $I_d$ than NMOS due to the lower mobility of holes vs. electrons.

For low-power, low noise circuits, the signal amplifying transistors should be dimensioned and biased in weak inversion near the onset of moderate inversion.

## B. Voltage gain

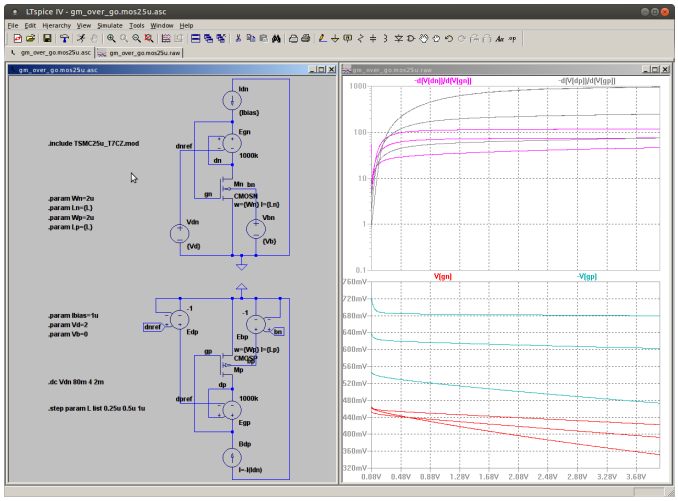

Fig. 4. Voltage gain characterization for 250 nm process

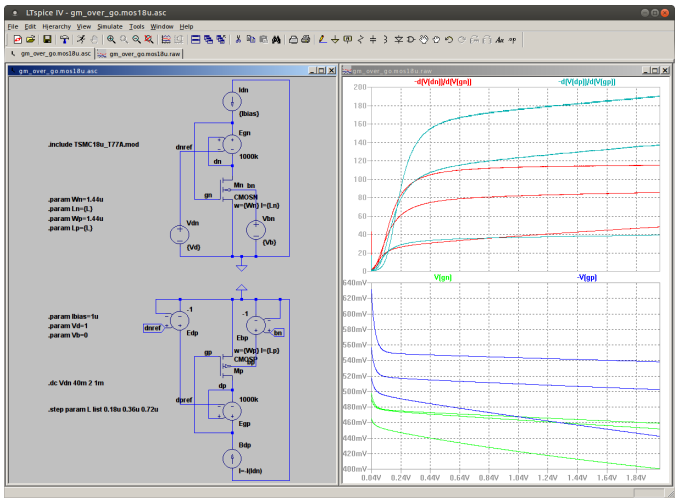

Fig. 5. Voltage gain characterization for 180 nm process

For the dc voltage gain of a transistor stage, the transconductance to output conductance ratio $g_m/g_o$ is the key figure of merit. $g_o$ depends on transistor length and drain-to-source voltage $V_{ds}$ in a way too complicated for hand calculations.

A linear sweep of $V_d$ at constant $I_d$ allows to optimize transistor length and minimum required $V_{ds}$ to achieve the best possible voltage gain within design constraints for the process. $g_m$ and $g_o$ are obtained by taking the derivatives of $V_g$ and $V_d$ with respect to the dc sweep variable $V_d$, and calculating the ratio

$$\frac{g_m}{g_o} = -\frac{\mathrm{d}\,(V_d)}{\mathrm{d}\,(V_g)} \tag{13}$$

due to the implicit relation for constant $I_d$

$$g_o\,\mathrm{d}\,(V_d) + g_m\,\mathrm{d}\,(V_g) = 0\,. \tag{14}$$

Figures 4 and 5 show LT Spice IV linear $V_d$ dc sweeps at different transistor lengths for two different processes (TSMC 250 nm and TSMC 180 nm).

Longer transistors have a higher $g_m/g_o$, PMOS can achieve higher $g_m/g_o$ than NMOS, and the process with larger minimum feater size has higher maximal $g_m/g_o$.

## IV. Conclusion

I present a single transistor simulation circuit, first published in the LT Spice Yahoo group in 2008[1] with feedback control of the gate voltage $V_g$ together with a method to dc sweep both $I_d$ for constant $V_d$ and $V_d$ for constant $I_d$ and a method to compute

$$g_m = \frac{\mathrm{d}\left(I_d\right)}{\mathrm{d}\left(V_g\right)} \quad \text{and} \quad \frac{g_m}{I_d} = \frac{\frac{\mathrm{d}(I_d)}{\mathrm{d}(V_g)}}{I_d} \tag{15}$$

from the $I_d$ sweep, and

$$\frac{g_m}{g_o} = -\frac{\mathrm{d}\left(V_d\right)}{\mathrm{d}\left(V_g\right)} \tag{16}$$

from the $V_d$ sweep.

This simulation circuit is suitable

- to get a quick overview of the properties of an unfamiliar IC process
- to set the dimension and bias points of transistors
- to design circuits using the $g_m/I_d$ methodology.

[1] https://groups.yahoo.com/neo/groups/LTspice/files/Badenke%20und%20Klee/