A Simulation Circuit to Characterize Transistors

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***Abstract*—I present a simple simulation schematic to extract transistor parameters relevant for analog circuit design: transconductance g_m, transconductance per current g_m/I_d, and voltage gain g_m/g_o.**

I. The circuit

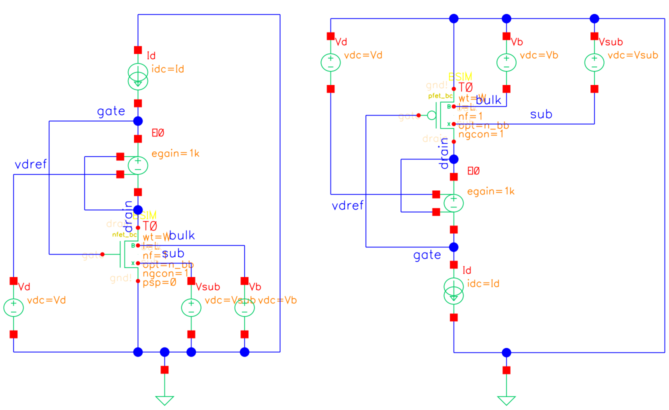

Fig. 1. Simulation schematics to characterize MOSFETs

The main design parameters for dimensioning MOSFETs are their drain current I_d, which controls transconductance, and the drain-to-source voltage V_{ds}, which controls output conductance g_o. However, the operating point of the transistor is controlled mostly by the gate-to-source voltage V_{gs}.

I solve this by regulating the gate voltage by a feedback loop that adjusts V_g to set the drain voltage V_d to a reference $V_{d,ref}$ by an ideal voltage controlled voltage source (VCVS) with voltage gain A. The schematics for the NMOS and PMOS simulation circuits are shown in Figure 1.

Kirchhoff's Current Law yields the small-signal equations

$$\begin{aligned} I_d &= g_m V_g + g_o V_d \\ V_g &= V_d + A\left(V_d - V_{d,ref}\right) \end{aligned} \tag{1}$$

which lead to

$$V_g = \frac{I_d - g_o\, V_{d,ref}\, A/\left(1+A\right)}{g_m + g_o/\left(1+A\right)} \tag{2}$$

and

$$V_d = \frac{I_d + A\, g_m\, V_{d,ref}}{\left(1+A\right) g_m + g_o}\,. \tag{3}$$

In the ideal case of $A \to \infty$,

$$V_g = \frac{I_d - g_o\, V_{d,ref}}{g_m} \tag{4}$$

and

$$V_d = V_{d,ref}\,. \tag{5}$$

II. Parameter extraction

A. Transconductance

The transconductance g_m as function of drain current can be obtained by sweeping I_d for fixed V_d, as

$$1/\left(\frac{\partial V_g}{\partial I_d}\right) = g_m + g_o/\left(1+A\right) \overset{A\to\infty}{\approx} g_m\,. \tag{6}$$

B. g_m/I_d

The specific transconductance g_m/I_d is a useful design parameter for setting the bias point of a transistor. g_m/I_d is maximal in subthreshold operation. It is obtained by sweeping I_d for fixed V_d and calculating

$$1/\left(\frac{\partial V_g}{\partial I_d}\, I_d\right) = \frac{g_m + g_o/\left(1+A\right)}{I_d} \overset{A\to\infty}{\approx} \frac{g_m}{I_d}\,. \tag{7}$$

C. g_m/g_o

While g_m or g_m/I_d is the most important design criterion for dimensioning a transistor, the next most important criterion is setting the output conductance g_o. With the circuits in Figure 1, the intrinsic voltage gain g_m/g_o can be extracted by sweeping $V_{d,ref}$ for constant I_d.

$$-\left(\frac{\partial V_d}{\partial V_{d,ref}}\right)/\left(\frac{\partial V_g}{\partial V_{d,ref}}\right) = \frac{\frac{A\, g_m}{(1+A) g_m + g_o}}{\frac{A\, g_o}{(1+A) g_m + g_o}} = \frac{g_m}{g_o}\,. \tag{8}$$