MII / RMII | SDMMC | DP, DM, STP, MXT, ULPI:CK | DP, DM, ID, DT, UD, STP, DT, ULPI:CK | DP, DM, ID, DT, UD, UR, VBUS To APB1-2 peripherals D-TCM D-TCM 64KB PHY PHY ETHER OTG_FS DMA1 DMA2 SDMMC2 OTG HS 1) 1 MAC Arm CPU Cortex-M7 480 MHz DMA FIFO DMA/ FIFO AXI/AHB12 (240MHz) JTRST, JIDA,
JTCK/SWCLK
JTDO/SWD, JTDO JTRST, JTDI, JTAG/SW 1 MB FLASH $\overline{\mathbb{U}}$ $\overline{\mathbb{U}}$ $\hat{\mathbb{I}}$ TRACECK 1 MB FLASH TRACED[3:0] I-Cache 16KB D-Cache 16KB 384 KB VAI DMA Mux1 SRAM1 32 KB SRAM2 16 KB SRAM FMC MDMA RNG ADC1 FMC_signals Ξ CHROM-ART (DMA2D) ADC2 FIFO Quad-SPI CLK, CS,D[7:0] TIM2 4 channels, ETR as AF TIM6 TIM3 WWDG TIM7 16b TIM4 SDMMC_D[7:0],SDMMC_D[7:3,1]Dir SDMMC_D0dir, SDMMC_D2dir CMD, CMDdir, CK, Ckin, CKio as AF ζŢ SWPMI SDMMC1 FIFO \square TIM12 Σ Delay block AHB2 (240MHz) Μ HSYNC, VSYNC, PIXCLK, D[13:0]

HRTIM1_CH[A, EX|
HRTIM1_FLT[5:1],
DFSDM1_CKOUT,
DFSDM1_CKNUOT,
DFSDM1_CKNUOT,
DFSDM1_CKNUOT,
SD, SCK, FS, MCLK, DICK[4:1] as AF T RX, TX, SCK, CTS, RTS as AF

RX, TX, SCK

RTS as AF

RX, TX, SCK

CTS, RTS as AF

RX, TX as AF USART2 HRTIM1 DFSDM1 UART4 RX, TX as AF SAI3 UART5 SD, SCK, FS, MCLK, CK[2:1] as AF \square UART7 SD, SCK, FS, MCLK, D[3:1] ידג UART8 RX, TX as Ar

MOSI, MISO, SCK, NSS /
BDO, SDI, CK, WS, MCK, as AF

MOSI, MISO, SCK, NSS /
SDO, SDI, CK, WS, MCK, as AF RX, TX as AF SPI MOSI, MISO, SCK, NSS as AF SPI2/I2S2 1 compl. chan.(TIM17_CH1N), 1 chan. (TIM17_CH1, BKIN as AF_ 1 compl. chan.(TIM16_CH1N), 1 chan. (TIM16_CH1, BKIN as AF_ TIM17 SPI3/I2S3 TIM16 I2C1/SMBUS SCL, SDA, SMBAL as AF DMA SRAM SCL, SDA, SMBAL as AF TIM15 Mux2 I2C2/SMBUS \mathbb{T} DAP 10 KB (I2C3/SMBUS SCL, SDA, SMBAL as AF ж **Î** MDIOs MDC, MDIO TX, RX ardUSART6 32-bit AHB BUS-MATRIX ardUSART1 I/F FDCAN2 4 compl. chan. (TIM1_CH1[1:4]N) 4 chan. (TIM1_CH1[1:4]ETR, BKIN as AF 4 compl. chan. (TIM8_CH1[1:4]N), 4 chan. (TIM8_CH1[1:4], ETR, BKIN as AF, TIM1/PWM 16b €4 KB SRAM USBCR HSEM Up to 17 analog inputs common to ADC1 and 2 PA...J[15.0] GPIO PORTA. J SPDIFRX1 TIM8/PWM 16b CEC as AF IN[1:4] as AF CRC HDMI-CEC \equiv DAC_OUT1, DAC_OUT2 as AF DAC LPTIM1 RCC OPAMPx_VINM OPAMPx_VINP OPAMPx_VOUT as AF OPAMP1&2 SD, SCK, FS, MCLK, D[3:1], CK[2:1] as AE
COMPx_INP, COMPx_INM, COMPx_OUT as AE VDDMMC33 = 1.8 to 3.6 V VDDUSB33 = 3.0 to 3.6 V VDD = 1.8 to 3.6 V VSS VCAP COMP1&2 LPTIM5_OUT as AF LPTIM5 VREF LPTIM3_OUT as AF LPTIM3 EXTI WKUP S RTC_TS RTC_TAMP[1:3] RTC_OUT RTC_REFIN SCL, SDA, SMBAL as AF < 12C4 SCL, SDA, SMBAL as AF
MOSI, MISO, SCK, NSS /
SDO, SDI, CK, WS, MCK, as AF
RX, TX, CK, CTS, RTS as AF
LPTIM2_IN1, LPTIM2_IN2 and
LPTIM2_OUT IWDG Backup registe SPI6/I2S6 S Temperature sensor LPUART1 LPTIM2 ®VDD SUPPLY SUPERVISION VDDA, VSSA NRESET WKUP[5:0] MSv48805V5

Figure 1. STM32H742xl/G block diagram

