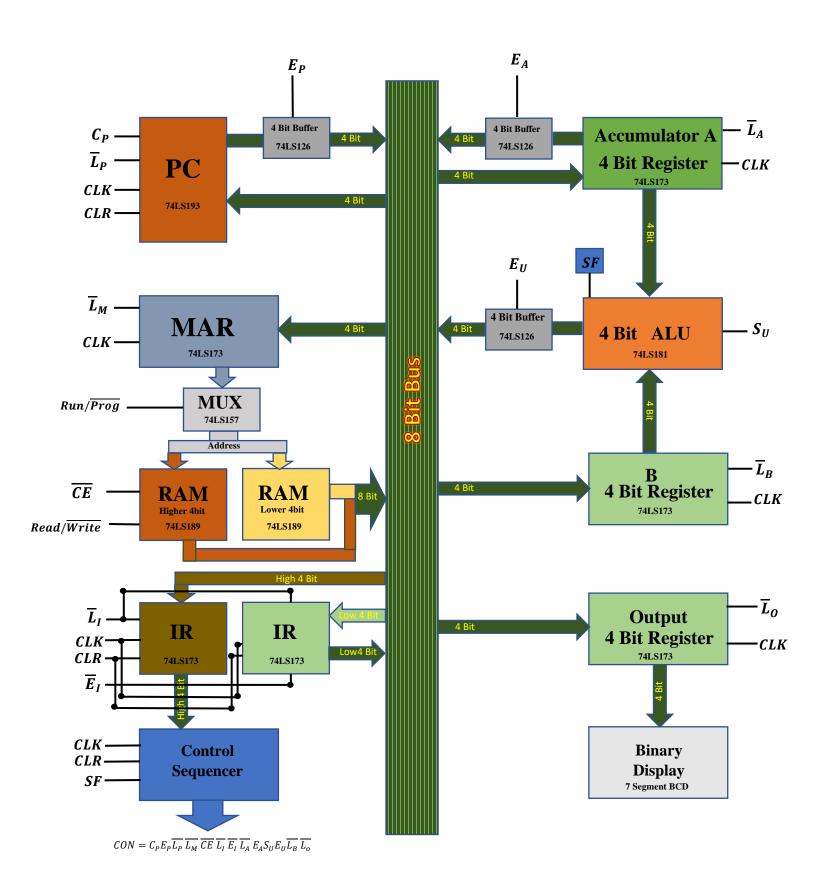


4-BIT MICROPROCESSOR

MARA KHA



LOW BUDGET INTEL 420, Downtown, London



Control word format:

$$CON = C_P E_P \overline{L_P} \overline{L_M} \overline{CE} \overline{L_I} \overline{E_I} \overline{L_A} E_A S_U E_U \overline{L_B} \overline{L_o}$$

Macro	State	CON(HEX)	Active
Fetch	T_1	DE3	E_P , $\overline{L_M}$
	T_2	1663	$C_P, \overline{CE}, \overline{L_I}$
LDA	T_3	05A3	$\overline{E_I}, \overline{L_M}$
	T_4	06C3	\overline{CE} , $\overline{L_A}$
MOV	T_3	07F1	$E_A, \overline{L_B}$
	T_4	07E3	NOP
INR	T_3	07C7	$E_U, \overline{L_A}$
	T_4	07E3	NOP
AND	T_3	07CF	$S_U, E_U, \overline{L_A}$
	T_4	07E3	NOP
JM When SF=1	T_3	03A3	$\overline{E_I},\overline{L_P}$
	T_4	07E3	NOP
OUT	T_3	07F2	$E_A, \overline{L_o}$
	T_4	07E3	NOP
HALT	T_3	07E3	NOP
	T_4	07E3	NOP

Control matrix design:

$$\begin{split} \operatorname{LDA} &= \overline{I_6} \ \overline{I_5} \ \overline{I_4} \\ \operatorname{MOV} &= \overline{I_6} \ \overline{I_5} \ I_4 \\ \operatorname{INR} &= \overline{I_6} \ I_5 \ I_4 \\ \operatorname{AND} &= \overline{I_6} \ I_5 \ I_4 \\ \operatorname{JM} &= \overline{I_1} + T_3 . LDA \\ \operatorname{JM} &= \overline{I_1} + T_3 . LDA \\ \operatorname{JM} &= \overline{I_2} \\ \operatorname{OUT} &= I_6 \ \overline{I_5} \ \overline{I_4} \\ \operatorname{DUT} &= I_6 \ \overline{I_5} \ I_4 \\ \operatorname{HALT} &= I_6 \ I_5 \ \overline{I_4} \\ \operatorname{HALT} &= I_6 \ I_5 \ \overline{I_4} \\ \operatorname{E}_I &= \overline{I_3} . LDA + T_3 . INR + T_3 . AND \\ \operatorname{E}_A &= T_3 . MOV + T_3 . OUT \\ \operatorname{S}_U &= T_3 . INR + T_3 . AND \\ \overline{L_B} &= \overline{T_3} . \overline{MOV} \\ \overline{L_0} &= \overline{T_3} . \overline{OUT} \\ \end{split}$$