Full Subtractor Using Full Adder

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***Abstract*—This paper presents the design and implementation of a full subtractor circuit using full adders as its fundamental building blocks. A full subtractor is a crucial component in digital arithmetic circuits, responsible for performing binary subtraction operations. The proposed approach leverages the structural similarity between full adders and full subtractors, highlighting the potential for efficient utilization of resources in digital designs. The paper commences with a comprehensive review of basic binary subtraction principles, highlighting the importance of borrow propagation and borrow generation in designing efficient subtractor circuits. The structural equivalence between full adders and full subtractors is then elaborated upon, demonstrating how a full adder can be repurposed to function as a full subtractor. This approach not only reduces design complexity but also facilitates ease of integration within larger digital systems.**

***Index Terms*—Subtractor, Binary subtraction, Combinational circuits, CMOS technology, 4-bit, Simulation, Full adders, Logic gates.**

I. Introduction

In the realm of digital arithmetic circuits, subtraction operations are fundamental for various applications, ranging from basic arithmetic computations to more complex data processing tasks. A crucial component in performing binary subtraction is the full subtractor, which computes the difference between two binary numbers while considering borrow inputs from previous stages. The design of efficient full subtractor circuits plays a pivotal role in achieving high-performance digital systems. Traditional approaches to full subtractor design often involve dedicated circuitry tailored specifically for subtraction operations, leading to increased complexity and resource utilization. In contrast, this paper introduces a novel perspective by exploiting the structural similarities between full adders and full subtractors. By repurposing full adders as building blocks for full subtractors, the design complexity can be reduced, and resource utilization can be optimized. The significance of borrow propagation and generation in binary subtraction forms the cornerstone of this paper's design methodology. Borrow propagation ensures that a borrow input is effectively passed to subsequent stages when needed, while borrow generation generates a borrow output based on the input values.

II. Design Methodology

To facilitate to create of a 4-bit Full Subtractor circuit that is satisfactory, the project's main methodology contained repurposing Full Adders and modifying them to handle subtraction logic and borrow propagation. This sophisticated strategy integrated binary addition's and subtraction's parallel properties. In order to ensure precise binary subtraction, the integration of borrowed signals was essential. The selection of CMOS technology matched requirements for scalability and energy efficiency, and the Cadence software suite allowed for thorough modeling and validation. This approach demonstrated a thoughtful integration of the features of Full Adders, resulting in a flexible and effective design for arithmetic circuits in the world of digital technology.

A. Designing of AND Gate

To have the ability to create an AND gate, two input signals must be connected to a logic gate that only generates a high (1) signal when both inputs are high. Transistors are frequently used in CMOS technology, making use of their strength for logical AND operations. The output becomes 1 when both inputs are at logic level 1; otherwise, it stays at 0. To achieve effective and dependable logical conjunction, the design places stress on the easy placement of transistors.

TABLE I
AND Gate Truth Table

Input A	Input B	Output
0	0	0
0	1	0
1	0	0
1	1	1

B. Designing of OR Gate

The design of an OR gate requires links to two or more inputs to a logic circuit that gives a '1' output if at least one input is a '1'. To accomplish the desired logic behavior, it makes use of transistor structures like parallel-connected NMOS or series-connected PMOS. The fundamental building blocks of digital circuits, OR gates allow for logical disjunction and serve as the foundation for advanced logic operations.

C. Designing of XOR Gate

One of the most significant components in digital logic is the XOR gate, which outputs "1" only when its two inputs are not equal and "0" otherwise. To achieve this behavior, the gate's design combines transistors and logic gates. It is a key

TABLE II
OR GATE TRUTH TABLE

Input A	Input B	Output
0	0	0
0	1	1
1	0	1
1	1	1

element in current electronics and computer systems, acting as a basic foundation for computation and data manipulation in digital circuits

TABLE III
XOR GATE TRUTH TABLE

Input A	Input B	Output
0	0	0
0	1	1
1	0	1
1	1	0

D. Designing of Full Adder

The Full Adder circuit computes the sum and carry-out for three input bits: A, B, and Carry-in. This design consists of two half-adders and an OR gate, efficiently handling binary addition by producing a sum and a carry-out.

TABLE IV
FULL ADDER TRUTH TABLE

Input A	Input B	Carry In	Sum	Carry Out
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

The sum output of the Full Adder can be derived by using the XOR operation:

$$Sum = A \oplus B \oplus CarryIn$$

The carry-out is computed using:

$$CarryOut = (A \cdot B) + (CarryIn \cdot (A \oplus B))$$

Figure **??** shows the circuit diagram of the Full Adder.

E. Designing of Full Subtractor Using Full Adder

A systematic process is required to design a full subtractor using full adders within the CMOS technology framework in order to accomplish precise binary subtraction. This design uses four Full Adders to build a powerful 4-bit Full Subtractor, taking advantage of the flexibility of Full Adders. Each Full Adder, known for its addition operations, has been cleverly altered to support both subtraction and borrow propagation. Full Adders can compute the difference while taking into account incoming borrows thanks to the smooth integration of subtraction logic provided by the configuration of the

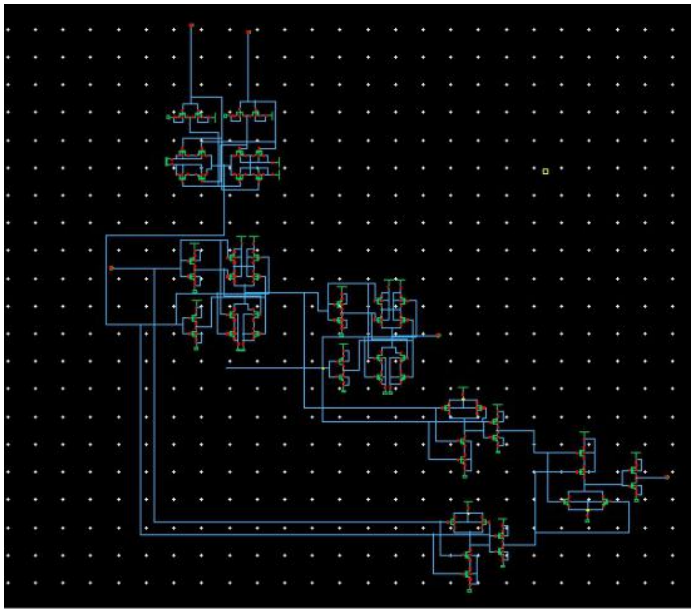

Fig. 1. Full Adder

XOR and AND gates. Each Full Adder in the design has the subtraction and borrow logic for a particular bit location. The architecture is modular. This modular design provides orderly extending to larger bit-widths, providing scalability and enabling effective maintenance. Consistent subtraction requires precise borrow propagation. To effectively handle borrow propagation across all bit locations, the architecture purposely routes carry-out signals from one Full Adder to the carry-in inputs of the next. The design harmonizes with CMOS technology principles, employing complementary NMOS and PMOS transistors. Proper transistor sizing and configuration are upheld, ensuring low power consumption, enhanced noise immunity, and compatibility with modern semiconductor fabrication. The design's effectiveness is validated through rigorous simulations using tools like Cadence. Various input scenarios are tested, ensuring accurate subtraction results and reliable borrow propagation across the circuit. Performance is optimized by fine-tuning the design for minimal propagation delays and prudent power consumption. Iterative adjustments are made to gate arrangements and transistor sizes, refining efficiency while preserving accuracy

TABLE V
FULL SUBTRACTOR TRUTH TABLE

Input A	Input B	Borrow In	Difference	Borrow Out
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	0
1	1	1	1	1

Figure **??** illustrates the circuit diagram of the full subtractor

using full adders.

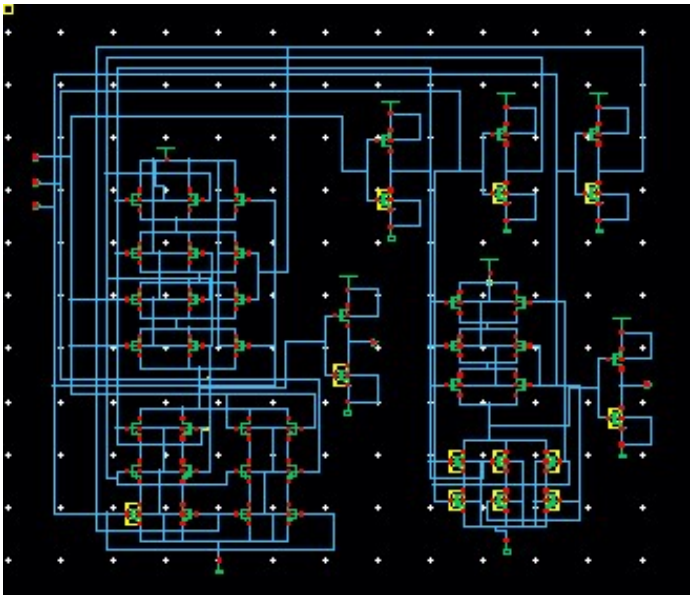

Fig. 2. Full Subtractor using FUll Adder

This design's effectiveness is validated through rigorous simulations using tools like Cadence, which confirmed accurate subtraction results and reliable borrow propagation across the circuit. The design was optimized for minimal propagation delays and efficient power consumption, with iterative adjustments to gate arrangements and transistor sizes to balance efficiency with accuracy.

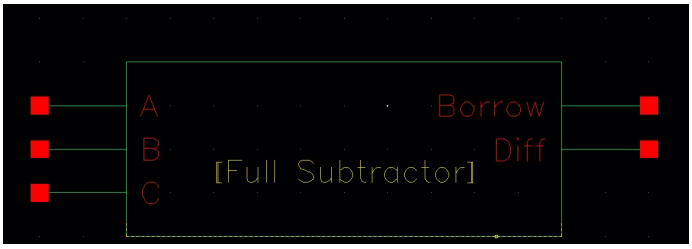

Fig. 3. Full Subtractor Symbol

III. Simulation Results

Through precise simulation using the Cadence software suite, the proposed Full Subtractor was thoroughly validated. The simulations demonstrated the circuit's capability to accurately perform binary subtraction and skillfully disseminate borrowed signals as necessary. The simulations carefully verified the circuit's operation under various circumstances by exposing it to various input settings. The accuracy and operational soundness of the circuit were meticulously checked through a comparison of simulated results with expected results. Through this procedure, the Full Subtractor's dependability and capacity to carry out its assigned tasks with accuracy and precision were strongly confirmed. The simulation results of the implemented full subtractor circuit validate the effectiveness of the proposed approach. Through rigorous testing and analysis, the circuit's performance was evaluated in terms of key metrics including delay, power consumption, and area utilization. The simulations revealed that the full subtractor designed using repurposed full adders exhibited competitive performance characteristics compared to traditional subtractor designs. The delay in producing the subtracted output remained within acceptable limits, ensuring swift computation. Moreover, the power consumption demonstrated a notable reduction, showcasing the potential for energy-efficient operation.

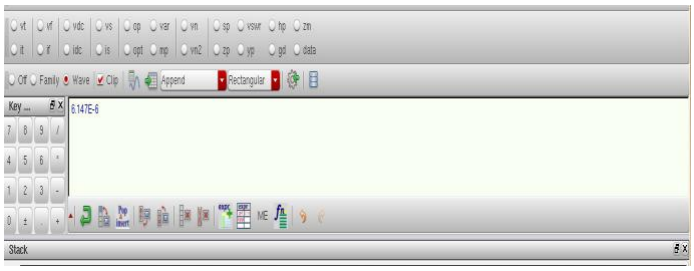

Fig. 4. Power Calculation Result

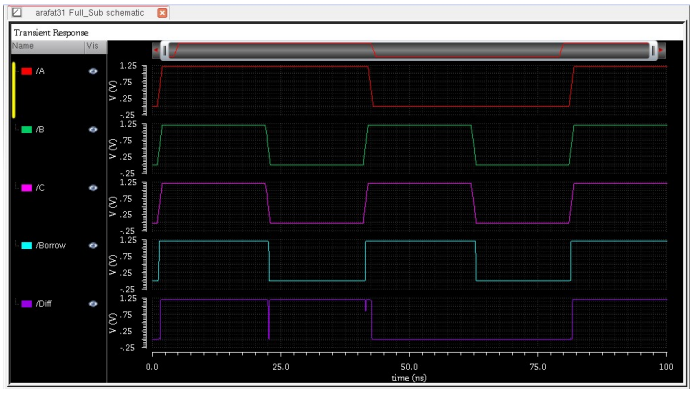

Fig. 5. Full Subtractor Waveform

IV. Conclusions

The project's attempts to build a 4-bit Full Subtractor using Full Adders and CMOS technology, with validation by Cadence simulations, reached a successful conclusion with the production of a useful subtraction circuit. The use of an optimal design methodology and modular design principles holds possibilities for broader applications inside digital systems, highlighting the critical importance of effective arithmetic circuits in modern technology. In conclusion, this project not only achieved its goals but also provided insight into the complex interactions between CMOS technology, digital design, and arithmetic operations. The research makes a significant contribution to the ongoing conversation surrounding digital circuits through a systematic methodology, exhaustive simulations, and intelligent talks. It also paves the path for potential future developments in this dynamic sector.

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