

CSE 3015 DIGITAL LOGIC DESIGN TERM PROJECT

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PHASE 1 – Assembler

In the first step of the project we had to create an assembler. To do this we designed an instruction set architecture. Then we wrote an assembler that will convert the instructions contained in this ISA into machine code that the CPU can understand. We preferred java language to write the assembler.

Here is our ISA:

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
AND	0	0	0	0	DST	DST	DST	SR1	SR1	SR1	0	0	0	SR2	SR2	SR2
ADD	0	0	0	1	DST	DST	DST	SR1	SR1	SR1	0	0	0	SR2	SR2	SR2
ANDI	0	0	1	0	DST	DST	DST	SR1	SR1	SR1	Imm	lmm	lmm	lmm	Imm	Imm
ADDI	0	0	1	1	DST	DST	DST	SR1	SR1	SR1	Imm	lmm	lmm	lmm	Imm	Imm
LD	0	1	0	0	DST	DST	DST	ADDR								
ST	0	1	0	1	SR1	SR1	SR1	ADDR								
CMP	0	1	1	0	0	0	0	OP1	OP1	OP1	0	0	0	OP2	OP2	OP2
JMP	0	1	1	1	0	0	ADDR									
JE	1	0	0	0	0	0	ADDR									
JA	1	0	0	1	0	0	ADDR									
JB	1	0	1	0	0	0	ADDR									
JBE	1	0	1	1	0	0	ADDR									
JAE	1	1	0	0	0	0	ADDR									

In our assembler we get instructions from a .txt file then convert them to hex codes and print them out a .txt file.

Since we have a total of 13 instructions, the allocation of 4 bits for each opcode will suffice.

Here are some code parts from our assembler:

toBinary Method:

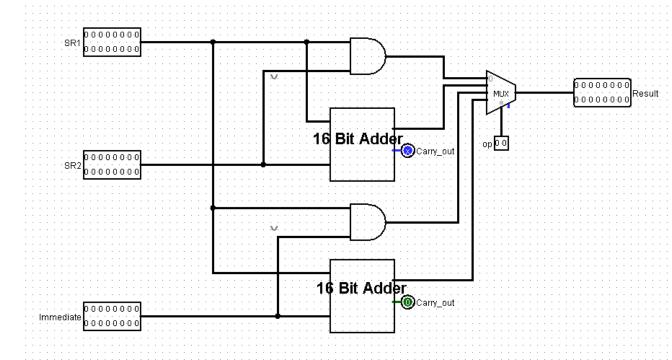
instructions method:

toHexadecimal method:

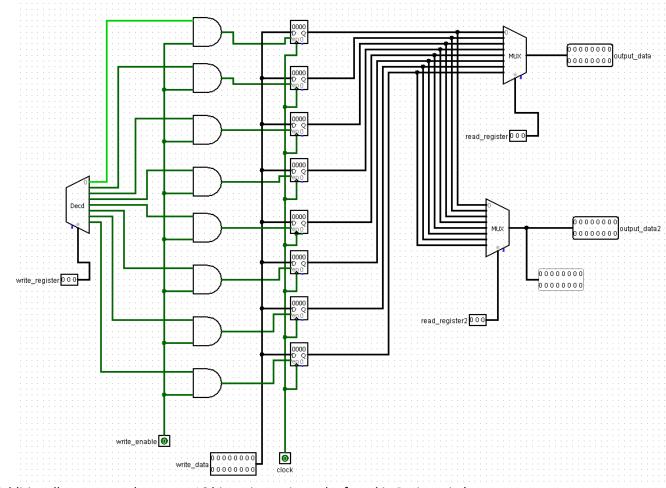
PHASE 2 – Logisim Component Design

In this phase of the project, we are supposed to design our components on the datapath except Control Unit.

Arithmetic Logic Unit:

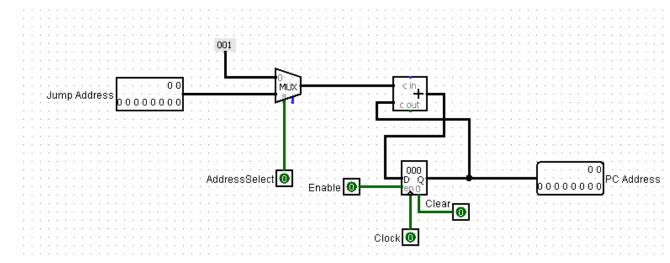


Register File:



(Additionally we created our own 16 bit registers, it can be found in Project.circ)

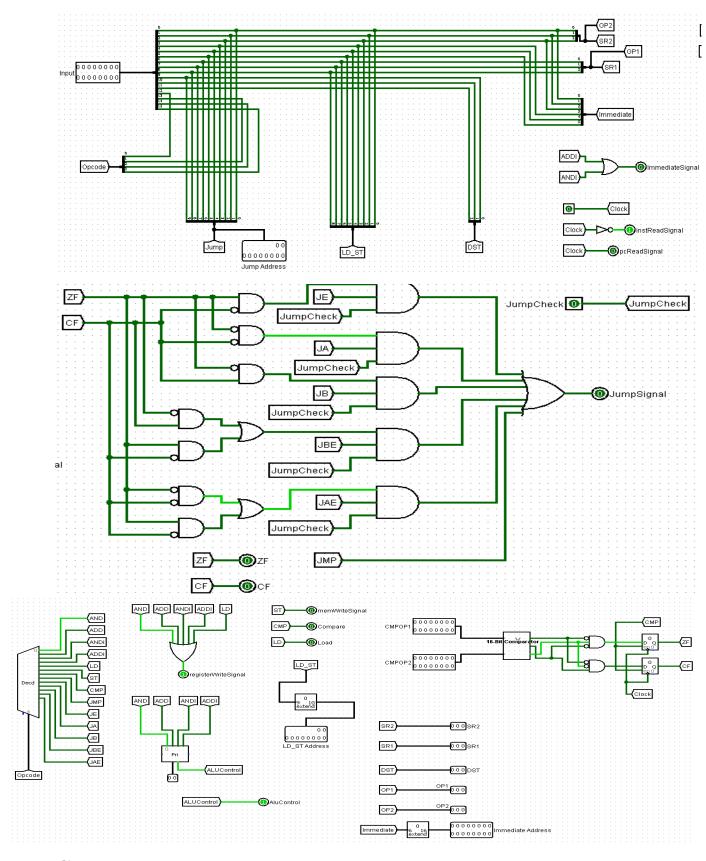
Pc Register:



PHASE 3 – Logisim Design with Control Unit

In this phase of the project, we are supposed to design our Control Unit.

Control Unit:



CPU:

