CMPSC473 Project3
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Project Overview:

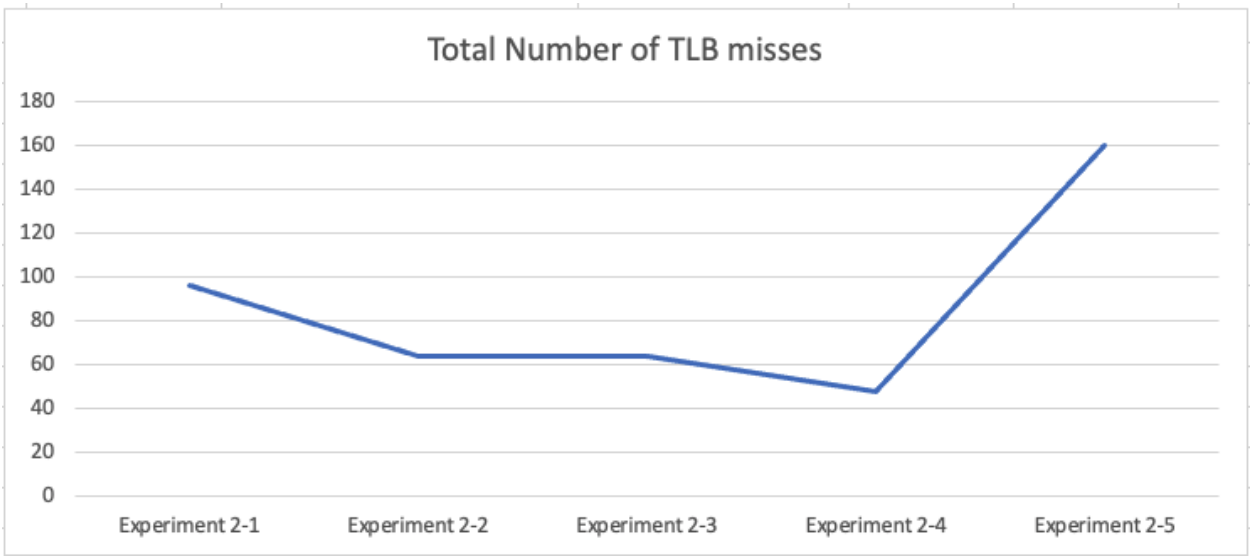
The project of implementing a Virtual Memory Management Simulation proved to be a very difficult but interesting task. The idea was to implement the typical virtual memory hierarchy and simulate how an MMU would handle a series of instructions delivered to it.

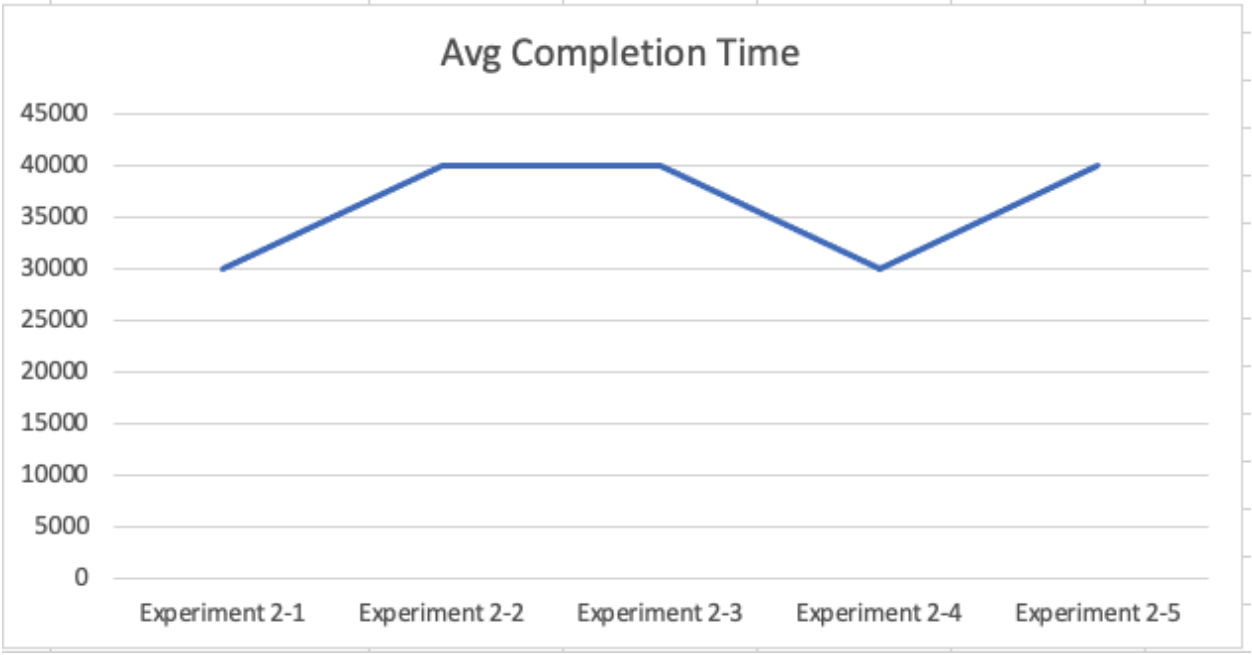
To do this we created a variety of data structures that acted as a TLB, a DRAM, and a Page Table. Each demonstrating the events and states created from things like hits, misses, and even overall page faults. All of this information being displayed in the below statistics. But we also had to implement the correct outcomes of each event, including maintaining timings and creating an LRU algorithm for TLB entry replacement and page-replacement.

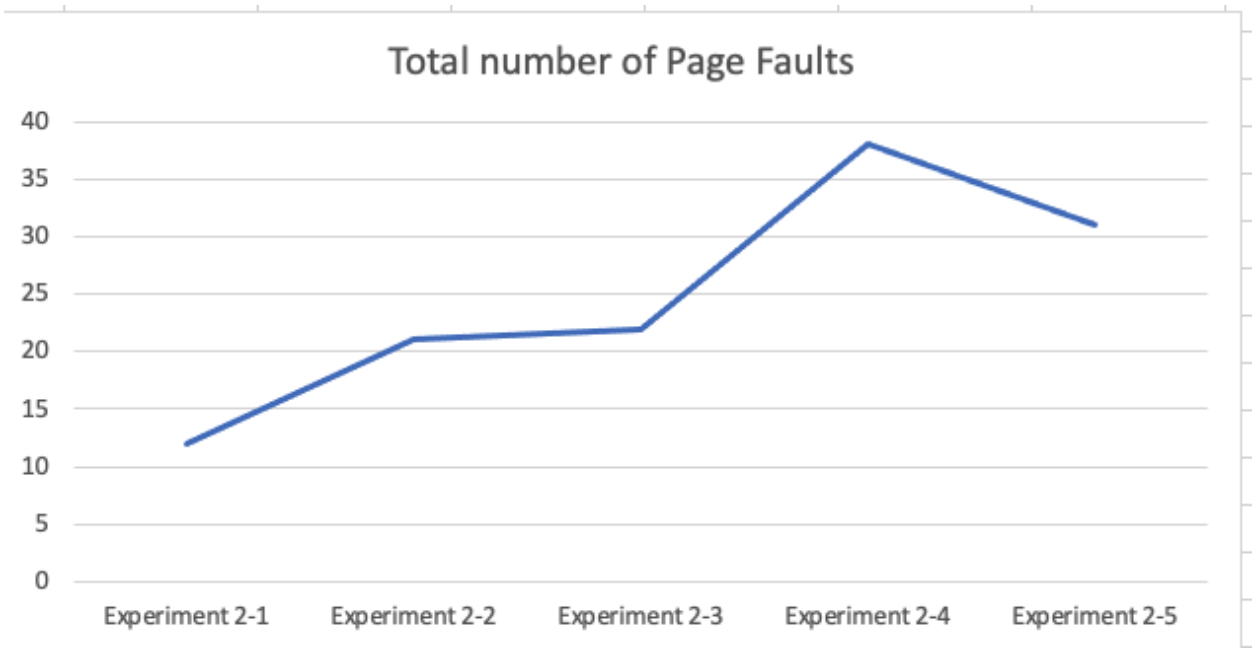
Experiment Type 1

Input	total number of context switches	total number of disk interrupts	total number of TLB misses	% of TLB misses	total number of page faults	% of page faults	total fraction of time in blocked state	total amount of time spent in OS mode	total amount of time spent in user mode
5	10	35	128	100%	35	25%	33%	18446744073639552616	0
6	-	-	-	-	-	-	-	-	-
7	-	-	-	-	-	-	-	-	-
8	-	-	-	-	-	-	-	-	-
9	21	82	304	100%	82	30%	37%	18798348993298849843	7

Experiment Type 2







Project Final Report

From the above data, I am incredibly perplexed by what is happening and how this data could have come about. From my research in the lectures and textbooks, the data in my findings does not line up much at all. The trend I had expected from researching this topic is that as the page tables reduce in size or even in number, we should be seeing far more page faults, and thus penalty time associated with that. We don't see much change in our page faults numbers and also correlated OS time in our findings and it can be assumed that there may be issues with the way we implemented our page table.