ESE532 Project P2 Report

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November 6, 2019

1 Design Space Axes

1. **Axis:** S, Number of SHA-256 hardware units
   Challenge: Improving throughput of hashing step
   Opportunity: Send chunks to rotating SHA unit index to allow for parallel execution
   Continuum: Anywhere from 1 to however many of our hardware SHA units will fit on the FPGA
   Equation for Benefit: $\texttt{Throughput}(S) = S * \texttt{singleSHAUnitThroughput}$

2. **Axis:** L, Number of LZW hardware units
   Challenge: Improving throughput of LZW step
   Opportunity: Send chunks to rotating LZE unit index to allow for parallel execution
   Continuum: Anywhere from 1 to however many of our hardware LZW units will fit on the FPGA (BRAM likely limiting factor)
   Equation for Benefit: $\texttt{Throughput}(L) = S * \texttt{singleLZWUnitThroughput}$

3. **Axis:** Z, Design choice for LZW hash table unit
   Challenge: Allow for efficient access of code-table for LZW step while fitting within hardware specifications
   Opportunity: Use trees or associative memories (or both) to allow for low cycle count for finding relevant table entry
   Continuum: $Z \in \{$Tree with Dense RAM, Tree with Fully Associative Memory, Tree with Tree, Tree with Hybrid$\}$
   Equation for Benefit: Slide 65 from Day 17 has the relevant tradeoff chart, with implied `implementation_complexity` parameter to consider.

4.

5.

2 Teamwork