Order of Operations List
*Assumes NOR Bit Array

Step #	General Step Description	Write Operation	Search Operation
1	Incoming initial control + data signals	i_WENB -> Low Write Address onto WA lines Write Data onto WD lines	i_WENB -> High Search Data onto SD lines
2	CLK rises Before precharge, correct?	-	-
3	Precharging	Need to Precharge WL -> 0? Precharge BLs -> Vdd/2? No SL precharge? No ML precharge?	Precharge SLs -> 0 Precharge ML -> 1 No BL precharge? No WL precharge?
4	Drive Data	Drive write data onto BL pairs (one high, other low, depending on write 1 or 0)	Drive search value onto SL pairs (one high, other low, depending on write 1 or 0)
5	Trigger Action	Raise the WL of desired write address to trigger write cycle (Low BL line will then write stored value to bit cell)	What triggers ML evaluate? (No ML discharge = Match. Yes ML discharge = no match)
6	End of Action Events + Final Outputs	None? No “write success” feedback. When are we officially donewriting? Assumed complete after some hold time?	Found -> High if match Return match address onto MA lines if match
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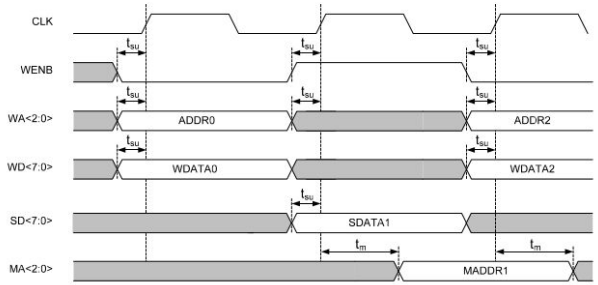
- **Inputs**
  - **WA<2:0>** – write-address
  - **WD<7:0>** – write data
  - **SD<7:0>** – search data
  - **WENB** – write-enable bar (low = write, high = match)
  - **CLK** – clock
- **Outputs**
  - **MA<2:0>** – match-address
  - **FOUND** – (high = match found, low = no match)

System Timing



- Output data must be stored until next value arrives
- t_{su} – Setup time for your input vectors
- t_m – Match time