Taylor Templeton

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SUMMARY

Engineer with semiconductor fabrication experience (process, product, quality) reskilling for a design verification or hardware engineering-related role near Raleigh, North Carolina. US citizen; no sponsorship required.

SKILL

Certifications/Recent Coursework:

- Fundamentals of Logic Design - ECE212 NC State Univ. — In progress - ECD Dec 2023
- C++ Data Structures and Algorithms - Coursera/Univ. Of Illinois — In progress - ECD Sept 2023
- Intro C Programming Specialization - Coursera/Duke Univ. — Jan 2023
- Cadence Certifications:
  - SystemVerilog for Design and Verification v21.10 Exam — Feb 2023
  - SystemVerilog Accelerated Verification with UVM v1.2.5 Exam — Feb 2023
  - SystemVerilog Assertions v5.1 Exam — Feb 2023

Self-Assigned Projects:

- Project #3: Cache Hierarchy Simulator — In progress - ECD Sept 2023
  - https://github.com/taylortempleton/CacheHierarchySimulator
  - Goal: Build understanding of cache hierarchy principles: replacement, inclusion, mapping, set-associativity
  - Output: Simulator to estimate miss rate of various cache configurations
  - Tools: C++
- Project #2: Open-Source RISC-V CPU Verification Testbench — August 2023
  - https://github.com/taylortempleton/SimpleCPU_RISC-V
  - Goal: Build understanding of RISC-V instruction set via attempted verification of RISC-V CPU
  - Output: Create verification testbench using open-source tools (Verilator)
  - Tools: C/C++, Verilog, Verilator, GTKwave
- Project #1: UVM Verification of Simple CPU — May 2023
  - https://github.com/taylortempleton/VerificationPractice_SimpleCPU
  - Goal: Build understanding of functional verification tools and concepts
  - Output: Drafted block-level verification plan, created testbench to execute plan and report coverage
  - Tools: SystemVerilog, UVM, assertions, coverpoints/groups, SynopsisVCS(via EDAPlayground)

EXPERIENCE

Qorvo, Greensboro, NC

Customer Quality Engineer — Mar 2021 - Aug 2022

- Served as lead quality contact for multinational smartphone manufacturers purchasing RF Front End ICs
- Led global, cross-functional 8D-team investigation of complex quality excursions: mined and analyzed data to guide hypothesis generation, lead/hosted team meetings, presented investigation findings before customer
- Planned and led high-visibility customer interactions, including quarterly customer review

Wolfspeed (Cree), Durham, NC

RF Product Engineer II — May 2019 - Mar 2021

- Conducted equipment/product/process qualification while establishing GaN-on-SiC device production line

Process Engineer I — Sept 2018 - May 2019

- Responsible for SPC monitoring and response, process improvement projects for etch process area

Process Engineering Technician III — July 2015 - Sept 2018

- Investigated tool failures and product anomalies for sputter, evaporation, anneal, etch, and CVD process areas

EDUCATION

New York University, New York, NY — Sept 2012 - May 2015

B.S., Chemical and Biomolecular Engineering, magna cum laude, 3.64 GPA

University Honors Scholar, Tau Beta Pi Honor Society, Omega Chi Epsilon Chemical Engineering Honor Society

PERSONAL

I enjoy reading biography and business history (most recently, *DEC is Dead, Long Live DEC: The Lasting Legacy of Digital Equipment Corporation*) and working on my house, which refuses to stop slowly falling apart.