# Taylor Kent Templeton

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## SUMMARY

Engineer with semiconductor fabrication background reskilling for an entry-level verification engineering role.

## SKILLS

Projects:

- Labs from Cadence Certification Training: March 2023
  - https://github.com/taylortempleton/CadenceSystemVerilogTraining
  - Projects completed while completing below cited certifications
- Simple CPU Verification Practice May 2023
  - https://github.com/taylortempleton/VerificationPractice_SimpleCPU
  - Drafted verification plan, created UVM testbench, and verified simple CPU and each component
  - Quantified verification with functional coverage and SystemVerilog Assertions
- OoO CPU Verification Practice **ECD July 2023**
  - Project definition in progress. Project to include block-level verification plan and hierarchically reusable UVM/SV testbench architecture for some aspect of Berkley's OoO risc-v BOOMcore.

Certifications:

- Cadence Training Certifications:
  - SystemVerilog for Design and Verification v21.10 Exam
  - SystemVerilog Accelerated Verification with UVM v1.2.5 Exam
  - SystemVerilog Assertions v5.1 Exam
- Coursera/Duke University: Introductory C Programming Specialization

Languages: C/C++, Systemverilog
Methodologies: UVM, SVA

## EXPERIENCE

**Qorvo, Inc.**, Greensboro, NC

Customer Quality Engineer, Advanced Cellular Group March 2021 – August 2022

- Served as quality contact for multinational manufacturers purchasing Qorvo RF front end modules
- Lead cross-functional 8D investigations to investigate and resolve customer-reported quality issues

**Wolfspeed (Cree)**, Durham, NC

RF Product Engineer II May 2019 – March 2021

- RF Development Team participant, tasked establishing GaN-on-SiC device production line
- Participated in production line planning, equipment purchases, product qualification

Process Engineer I; Dry and Wet Etch September 2018 – May 2019

- Responsible for NCM disposition, SPC monitoring and response, process improvement projects
- Solved highest yield-impacting fab defect: Si implant defectivity caused by operator mishandling

Process Engineering Technician III; Metal, Dielectric, Etch July 2015 – September 2018

- Investigated tool failures, product anomalies, misprocess events
- Supported sputter, evaporation, bond, anneal, dry etch, wet etch, and CVD process areas

## EDUCATION

**New York University**, New York, NY Sept. 2012 – May 2015

B.S., Chemical and Biomolecular Engineering, magna cum laude, 3.64 GPA
University Honors Scholar, Tau Beta Pi Honor Society, Omega Chi Epsilon Chemical Engineering Honor Society

## PERSONAL INTERESTS

I enjoy reading about history, fitness, and working on my house, which refuses to stop slowly falling apart.