Taylor Templeton

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SUMMARY

Engineer with semiconductor fabrication background reskilling for a design verification-related engineering role.

SKILL

Projects:

- Verification Practice Project #2: Simple CPU RISC-V   In Progress - July 2023
  - https://github.com/taylortempleton/SimpleCPU_RISC-V
  - Goal: Improve verification skill and understanding of RISC-V CPU architecture by verifying data and control paths of a pipelined RISC-V CPU
  - Completed random instruction generator for all RISC-V instructions
  - Created Verilator/C++ verification testbench

- Verification Practice Project #1: Simple CPU   May 2023
  - https://github.com/taylortempleton/VerificationPractice_SimpleCPU
  - Goal: Develop understanding of how verification tools and concepts work together by verifying a simple CPU, using available tools (EDAPlayground/Synopsys VCS)
  - Drafted block-level functional verification plan, capturing each block's requirements, stimulus required to fully exercise requirement and method of capturing DUT pass/fail
  - Created SV/UVM testbench, including scoreboard, SystemVerilog Assertions, coverpoints/groups

- Labs from Cadence Certification Training: Mar 2023
  - https://github.com/taylortempleton/CadenceSystemVerilogTraining

Certifications:

- Cadence Training Certifications:
  - SystemVerilog for Design and Verification v21.10 Exam
  - SystemVerilog Accelerated Verification with UVM v1.2.5 Exam
  - SystemVerilog Assertions v5.1 Exam
- Coursera/Duke University: Intro C Programming Specialization
- Coursera/Rice University: Intro to Scripting in Python Specialization (In progress. ECD August 2023)

Languages/OS: Systemverilog, C/C++, Linux, Mac

EXPERIENCE

Qorvo, Greensboro, NC

Customer Quality Engineer, Advanced Cellular Group   Mar 2021 - Aug 2022
- Served as quality contact for multinational manufacturers purchasing Qorvo RF front end modules
- Lead cross-functional team investigations of product quality issues

Wolfspeed (formerly Cree), Durham, NC

RF Product Engineer II   May 2019 - Mar 2021
- RF Development Team participant, tasked with establishing new GaN-on-SiC device production line
- Participated in production line planning, equipment purchases, product qualification

Process Engineer I; Dry and Wet Etch   Sept 2018 - May 2019
- Responsible for SPC monitoring and response, process improvement projects

Process Engineering Technician III; Metal, Dielectric, Etch   July 2015 - Sept 2018
- Supported sputter, evaporation, bond, anneal, dry etch, wet etch, and CVD process areas
- Investigated tool failures, product anomalies, misprocess events

EDUCATION

New York University, New York, NY   Sept 2012 - May 2015

B.S., Chemical and Biomolecular Engineering, magna cum laude, 3.64 GPA
University Honors Scholar, Tau Beta Pi Honor Society, Omega Chi Epsilon Chemical Engineering Honor Society

PERSONAL

I enjoy reading about history, fitness, and working on my house, which refuses to stop slowly falling apart.