Taylor Templeton

1125 Ralph Drive, Cary, North Carolina, 27511 | 919.538.2666 | taylor.templeton@gmail.com

SUMMARY

Engineer with semiconductor fabrication background reskilling for a design verification-related engineering role.

SKILL

Self-Assigned Projects:

- Project #3: Out-of-Order RISC-V CPU Verification — Next Project - ECD Nov 2023
- Project #2: Pipelined RISC-V CPU Verification — In Progress - ECD August 2023
  - https://github.com/taylortempleton/SimpleCPU_RISC-V
  - Goal: Verify data and control paths of cpu to develop bit-level understanding of risc-v isa and build understanding of pipelined risc-v cpu
  - Output:
    i. Create Verilator/C++ testbench for verification, debug and waveform review (Complete)
    ii. Debug and update existing random instruction sequence generator to support all RV32I base instructions (In progress. ECD 8/4)
    iii. Draft and execute verification plan (Pending. ECD 8/31)
  - Tools: C/C++, Verilog, Verilator, GTKwave
- Project #1: UVM Verification of Simple CPU — May 2023
  - https://github.com/taylortempleton/VerificationPractice_SimpleCPU
  - Goal: Build understanding of verification fundamentals with verification of simple CPU
  - Output: Drafted block-level verification plan, created testbench to execute plan and report coverage
  - Tools: SystemVerilog, UVM, assertions, coverpoints/groups, SynopsisVCS(EDAPlayground)
- Assorted Cadence Certification Labs: — Mar 2023
  - https://github.com/taylortempleton/CadenceSystemVerilogTraining

Certifications/Coursework:

- NCSU: ECE748 Advanced Verification with UVM (Enrolled for Fall 2023 Semester. ECD Dec 2023.)
- Coursera/Rice University: Intro to Scripting in Python Specialization (In progress. ECD Sept 2023.)
- Coursera/Duke University: Intro C Programming Specialization
- Cadence Certification: SystemVerilog for Design and Verification v21.10 Exam
- Cadence Certification: SystemVerilog Accelerated Verification with UVM v1.2.5 Exam
- Cadence Certification: SystemVerilog Assertions v5.1 Exam

EXPERIENCE

Qorvo, Greensboro, NC

Customer Quality Engineer — Mar 2021 - Aug 2022

- Mined and analyzed data, lead cross-functional team investigations during product quality excursions
- Planned and led formal interactions with phone manufacturers purchasing RF Front End integrated circuits

Wolfspeed (Cree), Durham, NC

RF Product Engineer II — May 2019 - Mar 2021

- Conducted equipment/product/process qualification while establishing GaN-on-SiC device production line

Process Engineer I — Sept 2018 - May 2019

- Responsible for SPC monitoring and response, process improvement projects for etch process area

Process Engineering Technician III — July 2015 - Sept 2018

- Investigated tool failures and product anomalies for sputter, evaporation, anneal, etch, and CVD process areas

EDUCATION

New York University, New York, NY — Sept 2012 - May 2015

B.S., Chemical and Biomolecular Engineering, magna cum laude, 3.64 GPA

University Honors Scholar, Tau Beta Pi Honor Society, Omega Chi Epsilon Chemical Engineering Honor Society

PERSONAL

I enjoy reading (most recently *DEC is Dead, Long Live DEC: The Lasting Legacy of Digital Equipment Corporation* by Schein), fitness and working on my house, which refuses to stop slowly falling apart.