



## EE1005 – Digital Logic Design Quiz# 5

**Instructor:** Muhammad Adeel Tahir    **Section:** SE-A

**Time:** 60 Minutes

**Name:** \_\_\_\_\_

**Roll No:** \_\_\_\_\_

**Total:** 20+15+30=65 marks

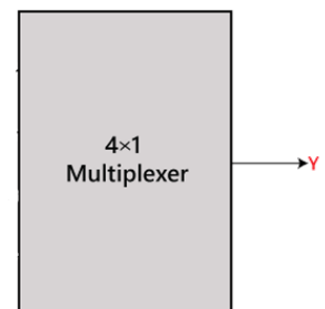
**Instructions:** Make sure the handwriting is neat and clean while drawing the circuit, quiz will be marked as 0 if attempted in a writing that is not readable at all.

### PART (a)

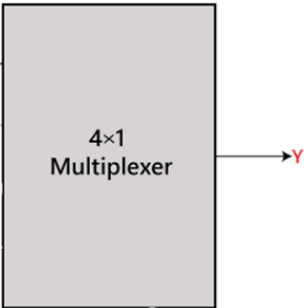
**Question 1:** Design a circuit that takes a 3-bit binary input and outputs a 2-bit binary number representing the count of '1's in the input. Use a 3-to-8 decoder, OR gates, and a 4-to-2 encoder for implementation. **[5 marks]**


**Question 2:** Implement the following Boolean function with 4X1 MUX and external gates where AB are select lines and C D are data lines. **[10+10 marks =20 marks]**

a)  $F(A,B,C,D) = \sum(1,3,4,11,12,13,14,15)$

b)  $F(A,B,C,D) = \sum (1,2,5,7,8,10,11,13,15)$

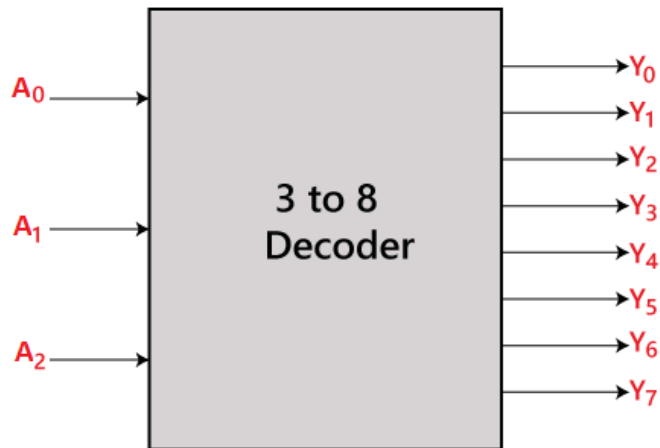


Part (b)

**Question 3:** Design a combinational circuit with a decoder to accept a 3-bit number and generate the output binary number equal to the square of the input number. Implement this using 8:4 decoder. **[15 marks]**


Working (if any):

(No cutting allowed)



**PART (c)**

**Question 4:** A sequential circuit with two D flip-flops A and B, two inputs, x and y ; and one output z is specified by the following next-state and output equations. **[15 Marks]**

$$A(t + 1) = xy' + xB$$

$$B(t + 1) = xA + xB'$$

$$z = A$$

Implement the following:

- Draw the logic diagram of the circuit.
- List the state table for the sequential circuit.
- Draw the corresponding state diagram.

**5 marks**

**6 marks**

**4 marks**

**Logic Diagram of the circuit (diagram must be neat and clean with proper connections, a 0 will be awarded in case the connections are not labelled and drawn properly)**



**Bonus Question:**

**(2 marks)**

1. In a car race, Alex finishes before Ben and Carl, but behind Dave. Ben finishes before Carl but behind Emma. Who finishes the race first? \_\_\_\_\_