EE1005 – Digital Logic Design
Assignment – 4
Combinational Circuits Spring 2024
Solution Manual

Students who followed the same design in Question 4 will have 0 marks since this is nothing but copy paste. Since this was a question where each student would implement his own design which can be different from each other although the gate implementation was same.

Note: Some questions may follow binary checking incase similarity is found.

Question 1: (5+5+5= 15 marks)

Design a combination circuit with N inputs and 3 outputs, X, Y, Z. The inputs represent a binary number, and the outputs represent characteristics of the numbers. Specifically. X should be true if the number is divisible by 3; Y should be true if the number is divisible by 4; and Z should be true if the number is divisible by 7. Suppose N = 4:

(a) Design the truth table for this problem.
(b) Implement the circuit with AND gates, OR gates, and NOT gates separately. Use k-map to simplify the output equations.
(c) Can this be reduced or simplified further using XOR gates? If yes, how? You do not need to implement the circuit but show proper working.

Solution:

A_3	A_2	A_1	A_0	X	Y	Z
0	0	0	0	1	1	1
0	0	0	1	0	0	0
0	0	1	0	0	0	0
0	0	1	1	1	0	0
0	1	0	0	0	1	0
0	1	0	1	0	0	0
0	1	1	0	1	0	0
0	1	1	1	0	0	1
1	0	0	0	0	1	0
1	0	0	1	1	0	0
1	0	1	0	0	0	0
1	0	1	1	0	0	0
1	1	0	0	1	1	0
1	1	0	1	0	0	0
1	1	1	0	0	0	1
1	1	1	1	1	0	0

The equations from truth table is :

For X, $\Rightarrow \sum m(0, 3, 6, 9, 12, 15)$

$$X = \bar{A}_3\bar{A}_2\bar{A}_1\bar{A}_0 + \bar{A}_3\bar{A}_2A_1A_0 + \bar{A}_3A_2A_1\bar{A}_0 + A_3\bar{A}_2\bar{A}_1A_0 + A_3A_2\bar{A}_1\bar{A}_0 + A_3A_2A_1A_0$$

A_3A_2 \ A_1A_0	$\bar{A}_1\bar{A}_0$ 00	$\bar{A}_1A_0$ 01	A_1A_0 11	$A_1\bar{A}_0$ 10
$\bar{A}_3\bar{A}_2$ 00	1 0	1	1 3	2
$\bar{A}_3A_2$ 01	4	5	7	1 6
A_3A_2 11	12 1	13	15 1	14
$A_3\bar{A}_2$ 10	8	1 9	11	10

$\Rightarrow$ We will get the same expression from k-map as well.

For Y, $\Rightarrow \sum m(0, 4, 8, 12)$

$$Y = \bar{A}_3\bar{A}_2\bar{A}_1\bar{A}_0 + \bar{A}_3A_2\bar{A}_1\bar{A}_0 + A_3\bar{A}_2\bar{A}_1\bar{A}_0 + A_3A_2\bar{A}_1\bar{A}_0$$

A_3A_2 \ A_1A_0	$\bar{A}_1\bar{A}_0$ 00	$\bar{A}_1A_0$ 01	A_1A_0 11	$A_1\bar{A}_0$ 10
$\bar{A}_3\bar{A}_2$ 00	1 0	1	3	2
$\bar{A}_3A_2$ 01	1 4	5	7	6
A_3A_2 11	1 12	13	15	14
$A_3\bar{A}_2$ 10	1 8	9	11	10

We can group :

- (0, 4, 8, 12) $\Rightarrow \bar{A}_1\bar{A}_0$

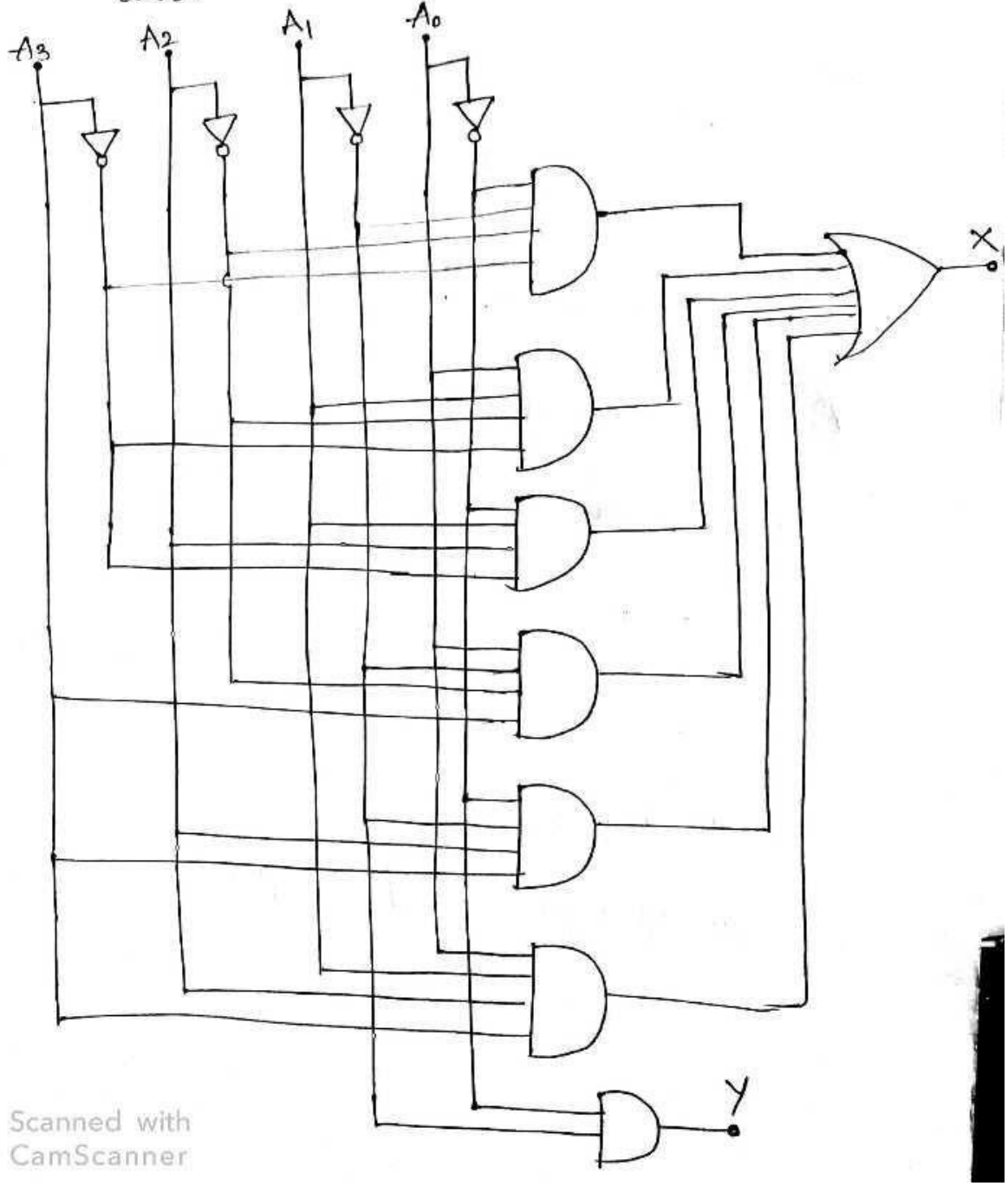
$\therefore$ Simplified form of $Y = \bar{A}_1\bar{A}_0$

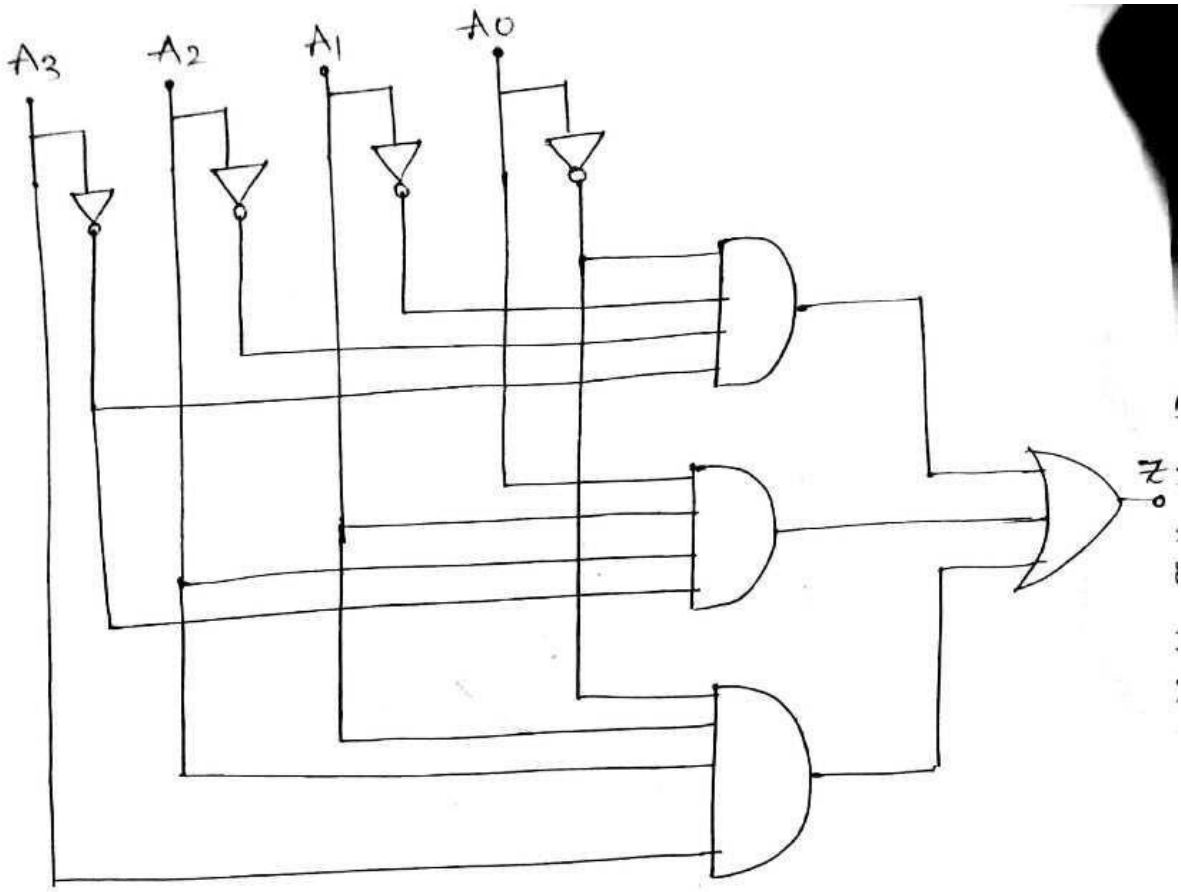
For Z, $\Rightarrow \sum m(0, 7, 14)$

$Z = \bar{A}_3 \bar{A}_2 \bar{A}_1 \bar{A}_0 + \bar{A}_3 A_2 A_1 A_0 + A_3 A_2 A_1 \bar{A}_0$

We will get the same after using K-maps also.

a)





b)

b) We got,

$$x = \bar{A}_3\bar{A}_2\bar{A}_1\bar{A}_0 + \bar{A}_3\bar{A}_2A_1A_0 + \bar{A}_3A_2A_1\bar{A}_0 + A_3\bar{A}_2\bar{A}_1A_0 + A_3A_2\bar{A}_1\bar{A}_0 + A_3A_2\bar{A}_1A_0$$

$$= \bar{A}_3\bar{A}_2(\bar{A}_1\bar{A}_0 + A_1A_0) + \bar{A}_3A_2A_1\bar{A}_0 + A_3\bar{A}_2\bar{A}_1A_0 + A_3A_2(\bar{A}_1\bar{A}_0 + A_1A_0)$$

$$= (\bar{A}_3\bar{A}_2 + A_3A_2)(\bar{A}_1\bar{A}_0 + A_1A_0) + \bar{A}_3A_2A_1\bar{A}_0 + A_3\bar{A}_2\bar{A}_1A_0$$

$$x = (A_2 \odot A_3)(A_1 \odot A_0) + \bar{A}_3A_2A_1\bar{A}_0 + A_3\bar{A}_2\bar{A}_1A_0$$

$$y = \bar{A}_1\bar{A}_0$$

$$z = \bar{A}_3\bar{A}_2\bar{A}_1\bar{A}_0 + A_2A_1(\bar{A}_3A_0 + A_3\bar{A}_0)$$

$$= \bar{A}_3\bar{A}_2\bar{A}_1\bar{A}_0 + A_2A_1(A_3 \oplus A_0)$$

Question 2: (3+3+4 = 10 marks)

Before take-off, the pilot and co-pilot of an aircraft carry out preflight safety checks. When all checks have been completed, they each move a switch from the up to the down position.

- When both switches are up, a red indicator on the instrument panel is on.
- This changes to yellow when at least one of them operates their switch.
- When both have operated their switches, a green indicator comes on.
- The engines can only be started when the green indicator is on.

Assume that the switches provide logic level 0 in the up position and logic level 1 in their down position. The LED indicators operate on logic level 1.

a) Write truth table for this circuit.
b) Make circuit diagram for individual outputs, then show a combined circuit. Properly label each question carefully.

c) Explain the assumptions/understanding of the problem in your own words, how did you approach the above problem, what sequence of steps did you take to justify your truth table. **Only 4-5 points which are precise and clear cut.**

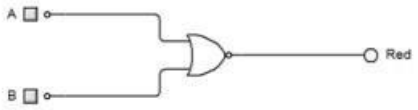
Solution

a) Check the completed truth table for the system.

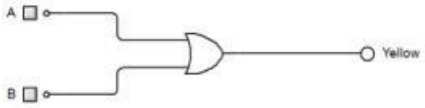
Inputs		Outputs		
B	A	R	Y	G
0	0	1	0	0
0	1	0	1	0
1	0	0	1	0
1	1	0	1	1

b) Now we need the logic system that can produce these outputs. Take each one in turn.

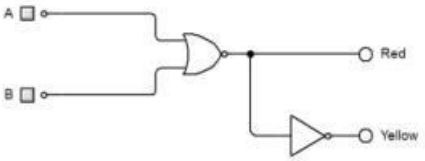
For the RED output – there is a standard gate that can produce this output – a NOR gate.



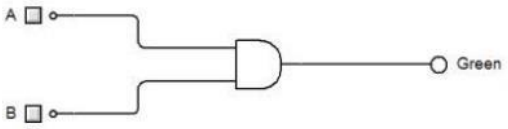
For the YELLOW output – there are actually two ways of generating the YELLOW output. First is a standard gate that can produce the output – an OR gate using inputs A and B.



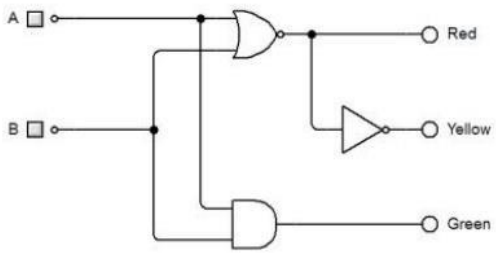
Alternatively the output Y is the opposite of the RED output. So we could achieve the same by just inverting the RED output



For GREEN output – again a standard gate can produce this output – an AND gate.



The complete system therefore is:



Question 3: **(4+4+2 = 10 marks)**

You are tasked with the design of a combination circuit, operating on certain principles of digital logic. This circuit is characterized by three inputs and three outputs. The inputs are denoted as x, y, and z, while the outputs are represented as A, B, and C. The functionality of this circuit is defined by a specific set of rules based on the binary input values. When the binary input, represented by the combination of x, y, and z, is either 0, 1, 2, or 3, the output is designed to be 1 greater than the input. This means that the circuit performs an increment operation on the input in these cases. On the other hand, when the binary input is 4, 5, 6, or 7, In these cases, the circuit performs a decrement operation on the input. The value is decremented by 2. Handle the don't care conditions carefully.

a) Draw truth table of the above circuit.
b) Implement the circuit diagram.
c) Explain why and how you chose the DON'T CARE conditions as implemented in part (a). Answering this wrong will lead to 50% deduction in the overall obtained marks in this question.

Example Solution:

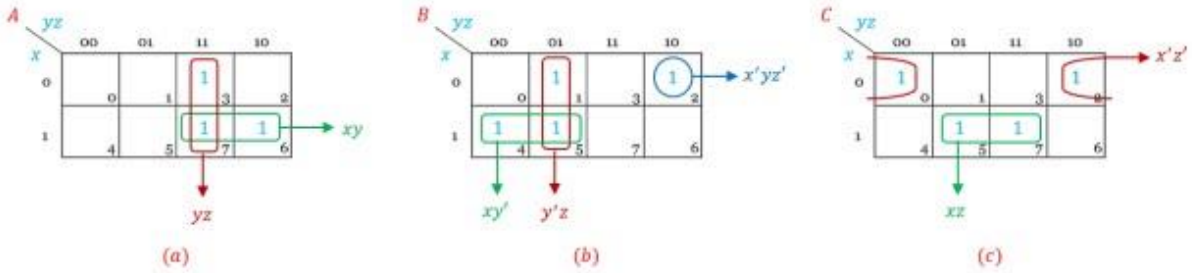
Based on the given description, we build the following truth table:

Input value	x	y	z	output value	A	B	C
0	0	0	0	$0+1=1$	0	0	1
1	0	0	1	$1+1=2$	0	1	0
2	0	1	0	$2+1=3$	0	1	1
3	0	1	1	$3+1=4$	1	0	0
4	1	0	0	$4-2=2$	0	1	0
5	1	0	1	$5-2=3$	0	1	1
6	1	1	0	$6-2=4$	1	0	0
7	1	1	1	$7-2=5$	1	0	1

Hence, the outputs can be expressed by

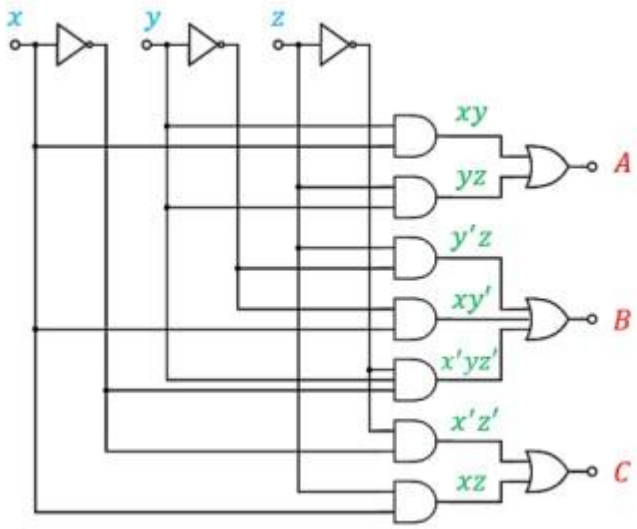
$$A = \sum(3,6,7)$$
$$B = \sum(1,2,4,5)$$
$$C = \sum(0,2,5,7)$$

The maps of the output functions A, B and C are plotted as shown below.



Based on the k-maps, we can write the simplified expressions of the output functions as

A = xy + yz
B = xy' + y'z + x'yz'
C = xz + x'z'



C) No don’t care conditions exist as the problem does not require it.

Question 4: **(5+3+2 = 10 marks)**

Devise a sophisticated combinational circuit aimed at determining the equality between two sets of 4-bit numbers. The circuit should yield an output of 1 when the two numbers are identical and 0 otherwise. For this purpose, only the most feasible and to-the-point solution will be marked as correct. Solving it without using **atleast one** of the following gates (XNOR, NAND, NOR) will lead to a straight 0.

a) Draw Truth table for this question in steps, direct steps will lead to a straight 0.
b) Choose the most suitable gate implementation for this question (all gates must be 2-input at the first level). Only the best one will be marked as correct.
c) Why did you choose the above gate implementation?

Solution:

For this question, you were required to follow specific steps when completing your design These steps included:

1. **Showing the truth table of XNOR itself and how it works**
2. **Demonstrating the selection of inputs to elaborate your design.**
3. **Displaying a sample truth table with an example output. (when the input numbers are not equal and when they are equal).**

Failure to adhere to these guidelines would result in a mark deduction.
Furthermore, students who neglected to include AND at the last output labeled as "E" would receive a zero for the circuit diagram, as the circuit would be unable to implement the provided design because that was the only step where the numbers would actually be equal or not.

a) Assume the two 4-bit binary numbers are

$$\boldsymbol{x} = x3.\,x2.\,x1.\,x0 \;and\; \boldsymbol{y} = y3.\,y2.\,y1.\,y0$$

We need to design a circuit that generates 1 when $x = y\,(x0 = y0,\ x1 = y1,\ x2 = y2,\ x3 = y3,\ x4 = y4)$ otherwise it generates 0.

Alternatively, we can use a truth table to identify the required function. We construct the following truth table to compare the two bits x_i and y_i, where $i = 0, 1, 2, 3$. The output bit should be 1 if the two inputs are equal and 0, otherwise.

x_i	y_i	z_i
0	0	1
0	1	0
1	0	0
1	1	1

Thus, the output function is

$$\begin{aligned} z_i &= x_i' y_i' + x_i y_i \\ &= (x_i \oplus y_i)' \quad \Rightarrow \quad \text{(XNOR)} \end{aligned}$$

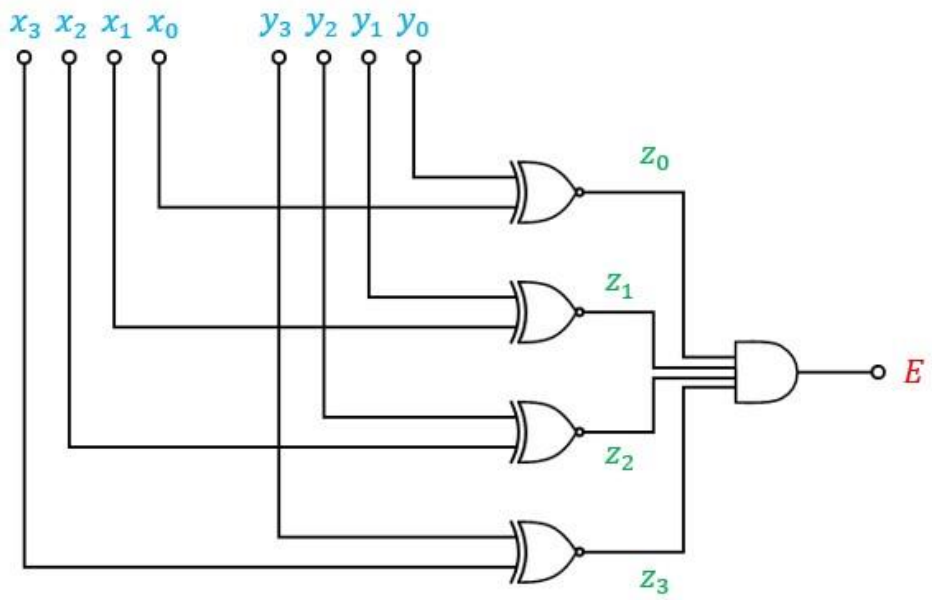
Where $xi\ XOR\ yi$ will be used for the 4 bit numbers in each x and y. See circuit diagram for better understanding.

Sample Table that was needed to showcase this (since the table was too big, only some parts were to be shown) including the last output E (where the gates will be ANDed together)

X (x3×2×1×0)	Y (y3y2y1y0)	z0 (XNOR)	z1 (XNOR)	z2 (XNOR)	z3 (XNOR)	E (AND)
0000	0000	1	1	1	1	1
0000	0001	0	1	1	1	0
0000	0010	1	0	1	1	0
...	...	...	...	...	...	...
1111	1110	0	1	1	1	0
1111	1111	1	1	1	1	1

Note: This is only an example truth table, students who attempted it in the above format with changed labelling and other columns , they will be given marks for it. There was no requirement of Don't care in this design.

b)



c) The equivalence function (XNOR gate) is suitable for this task because equivalence is a function that is 1 when the two binary variables are equal (i.e., when both are 0 or both are 1).

Question 5: **(5+5 = 10 marks)**

A combinational switching circuit has four inputs (A, B, C, D) and one output (F). F=0 iff three or four of the inputs are 0.

(a) Write the maxterm expansion for F.

(b) Using AND, OR gates, find a minimum three-level circuit to realize F. *(2-input gates at first level, 3 input gates at second level, 2 input gates at third level)* **Solution:**

a)

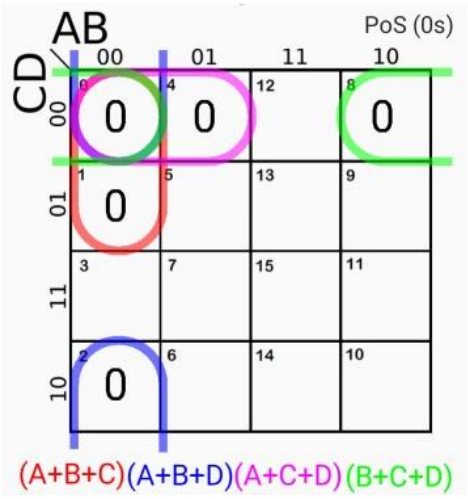
Given,

$F(A, B, C, D) = 0$ iff three or four of the inputs are 0.

Truth table for the above function is given below:-

A	B	C	D	F
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

We will use the above truth table to calculate K-map and Using that K-map we will derive the function F.



b) To

$F = (A+B+C)(A+B+D)(A+C+D)(B+C+D)$

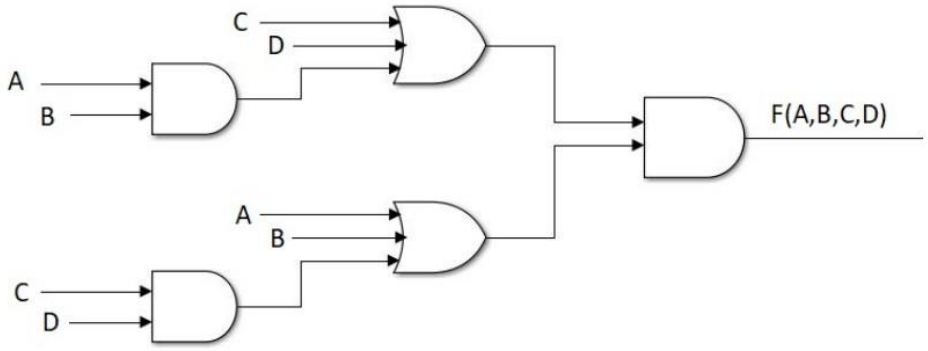
$=[A(C+D)+(C+D)(C+D)+AB+(C+D)B][(A+B)(A+B)+C(A+B)+(A+B)D+CD]$

$=[A(C+D)+(C+D)+(C+D)B+AB][(A+B)+C(A+B)+(A+B)D+CD]$

$=[(A+1+B)(C+D)+AB][(A+B)(1+C+D)+CD]$ *(Since A+1= 1, B+1 = 1, C+1 = 1, D+1 = 1)*

$=[C+D+AB][A+B+CD]$

$=[C+D+AB][A+B+CD]$



Question 6: (5+5+5 = 15 marks)

Imagine a sophisticated switching circuit, an intricate network of electronic components, that is fed by four distinct inputs. These inputs are not random but carry significant information. Inputs A and B are not merely binary digits, but together they represent the first and second bits of an unsigned binary number, which we shall refer to N1. Similarly, inputs C and D, while individually representing binary digits, collectively form the first and second bits of another unsigned binary number, denoted as N2.

The circuit is designed with a specific functionality in mind. It is tasked with producing an output of 1, but this output is contingent on a particular condition being met: the mathematical product of N1 and N2 must be less than or equal to 3. If this condition is not satisfied, the circuit defaults to an output of zero. Your challenge is to decipher the conditions under which this output is realized.

a) Implement the truth table of the above circuit.
b) Draw the circuit diagram using no more than 2 gates.
c) Explain your design in 3-4 lines including your assumptions, incase the explanation of the implemented circuit is wrong, the question will receive a straight 0.

A) TRUTH TABLE

N1		N2		
A	B	C	D	F
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	0
1	1	1	1	0

Minterm

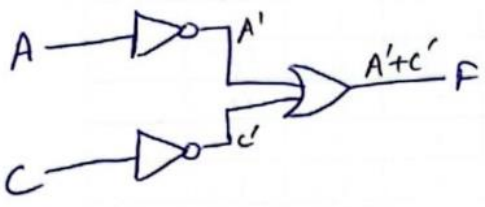
$\therefore F = \sum_m(0,1,2,3,4,5,6,7,8,9,12,13)$

B)

AB \ CD	00	01	11	10
00	1	1	1	1
01	1	1	1	1
11	1	1	0	0
10	1	1	0	0

$F = \bar{A} + \bar{C}$ ← simplified expression

C)



Question 7 **(5+5+5 = 15)**

You are tasked with the design of a combinational circuit. This circuit is to be characterized by its ability to process a three-bit binary number as its input. The uniqueness of this circuit lies in its output generation. The output is not a mere reflection of the input. Instead, it is a binary number that represents the square of the input number.

a) Draw the truth table of this circuit
b) Implement the circuit diagram
c) How does changing the square to calculating the cube of the input affect our circuit? Explain in 3-4 lines.

minterms	Inputs			Outputs					
	I_0	I_1	I_2	A_0	A_1	A_2	A_3	A_4	A_5
0	0	0	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0	0	1
2	0	1	0	0	0	0	1	0	0
3	0	1	1	0	0	1	0	0	1
4	1	0	0	0	1	0	0	0	0
5	1	0	1	0	1	1	0	0	1
6	1	1	0	1	0	0	1	0	0
7	1	1	1	1	1	0	0	0	1

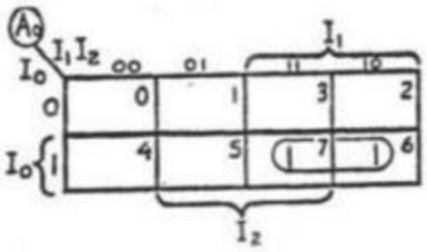
From the truth table it is seen that

$A_0 (I_0, I_1, I_2) = \sum 6, 7$
$A_1 (I_0, I_1, I_2) = \sum 4, 5, 7$
$A_2 (I_0, I_1, I_2) = \sum 3, 5$
$A_3 (I_0, I_1, I_2) = \sum 2, 6$
$A_4 (I_0, I_1, I_2) = \sum$ none – connect to Logic 0
$A_5 (I_0, I_1, I_2) = \sum 1, 3, 5, 7$

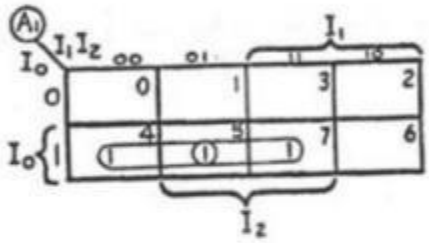
Use 3-variable K-maps to simplify the expressions

$A_0 = I_0 \, I_1$
$A_1 = I_0 \, \bar{I}_1 + I_0 \, I_2$
$A_2 = I_0 \, \bar{I}_1 \, \bar{I}_2 + \bar{I}_0 \, I_1 \, I_2$
$A_3 = I_1 \, \bar{I}_2$
$A_4 = 0$
$A_5 = I_2$

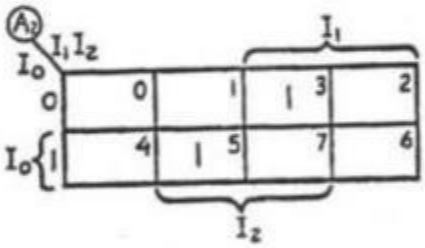
A logical diagram is drawn from the minimized equations. Figure 1 shows the combinational circuit.



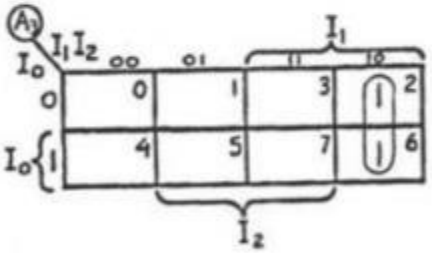
$A_0 = I_0 I_1$



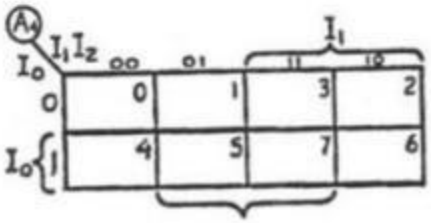
$A_1 = I_0 \bar{I}_1 + I_0 I_2$



$A_2 = I_0 \bar{I}_1 \; I_2 + \bar{I}_0 I_1 I_2$



$A_3 = I_1 \bar{I}_2$



$A_4 = 0$

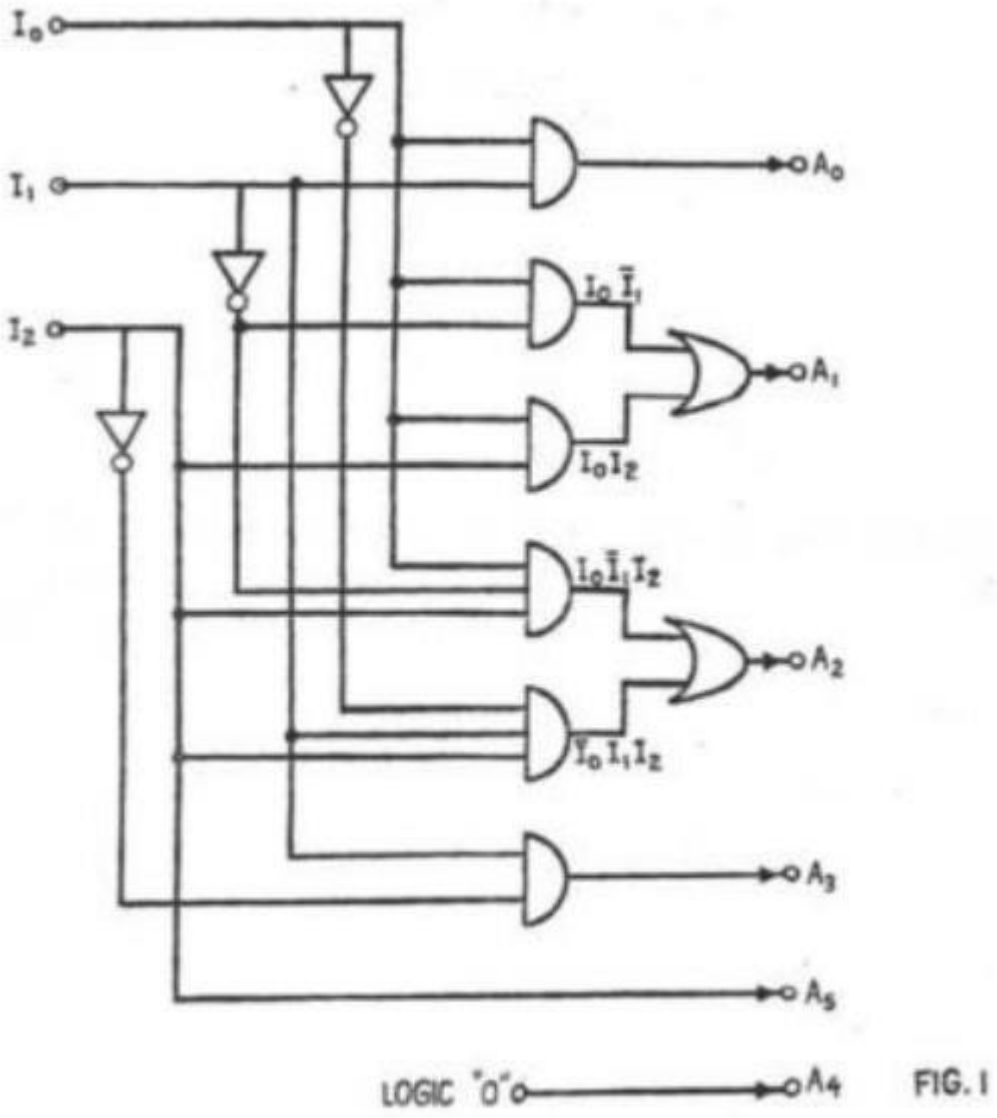


FIG. 1

c. Changing the operation from calculating the square to calculating the cube of the input would significantly affect our circuit. The complexity of the circuit would increase as the number of output bits would need to increase to accommodate the larger range of values. This is because the cube of a number can be much larger than the square of a number, especially for binary numbers. Therefore, more logic gates would be needed to implement the cubing operation, making the circuit more complex. Additionally, the truth table and the circuit diagram would also need to be updated to reflect these changes.

Question 8 **(5+3+2+5 = 15 marks)**

Mr James has invested a huge amount of money into buying and selling land. Before he buys a certain land, he must get input from three sources. His first source is Jimmy, a famous property dealer. His second source is Meg, a self-made millionaire in this business, and his third source is Carl, his best friend. After several months of receiving advice from all three, he has come to the following conclusions:

A). Buy if all three say yes.
B). Buy if the Carl says yes and Meg says no.
C). Buy if both the Carl and Jimmy says no.
D). Buy if Jimmy and Meg both say yes even if the Carl says no.
E). Don't buy otherwise.

Your task is to:

a) Explain the process of designing a combinational circuit in general step by step. Write it in your own words but keep it precise. (Limit 5-6 lines)
b) Implement the truth table of the above question
c) Write the equation in term of SOP
d) Optimize the equation using k-map properly showing grouping and labelling each pair's output in the diagram itself.
e) Draw circuit diagram.

a. Draw the truth table for above problem statement. **[2 Point]**

Jim	Meg	Carl	F1
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1

1	1	1	1

b. Write Output Equation in Sum of Minterms Form. **[1 Point]**

$$F = x'y'z' + x'y'z + x'yz' + xy'z + xyz' + xyz$$

c. Write Optimized version of above output equation using K-Maps. **[3 Points]**

$$F = x'y' + yz + yz'$$