National University

of Computer and Emerging Sciences Chiniot -Faisalabad Campus

EE1005 – Digital Logic Design
Quiz# 3

Instructor: Muhammad Adeel Tahir **Section:** SE – 2A **Time:** 20 Minutes

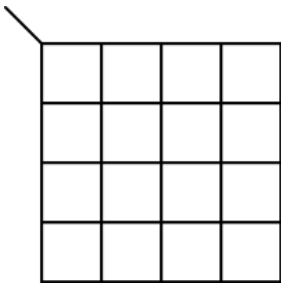
Name: _____

Roll No: _____ **Total: 20 marks**

Note: *Use the back side of the page if needed. Make sure the handwriting is neat while drawing the circuit, quiz will be marked as 0 if attempted in a writing that is not readable at all.* ***Cutting will result in negative marking.***

Q1: Draw a NAND logic diagram that implements the complement of the following function, use 2 input NAND gate for your implementation, label each output of gate carefully to avoid deduction of marks. Use the given k-map box, avoid cutting to show proper groupings. (5+5 = 10 marks)

$$F(A,B,C,D) = \Sigma(0,1,2,3,6,10,11,14)$$



G(A,B,C,D) = _____

Circuit Diagram:

Q2: Implement and draw circuit for the following Boolean function F, together with the don't-care conditions d, using no more than two NOR gates. Use the given k-map box, avoid cutting to show proper groupings. (5+5 = 10 marks)

$$\mathbf{F(A,B,C,D) = \Sigma(2,4,10,12,14)}$$
$$\mathbf{d(A,B,C,D) = \Sigma(0,1,5,8)}$$