EE1005 – Digital Logic Design

Assignment 5 (Solution)

Spring 2023

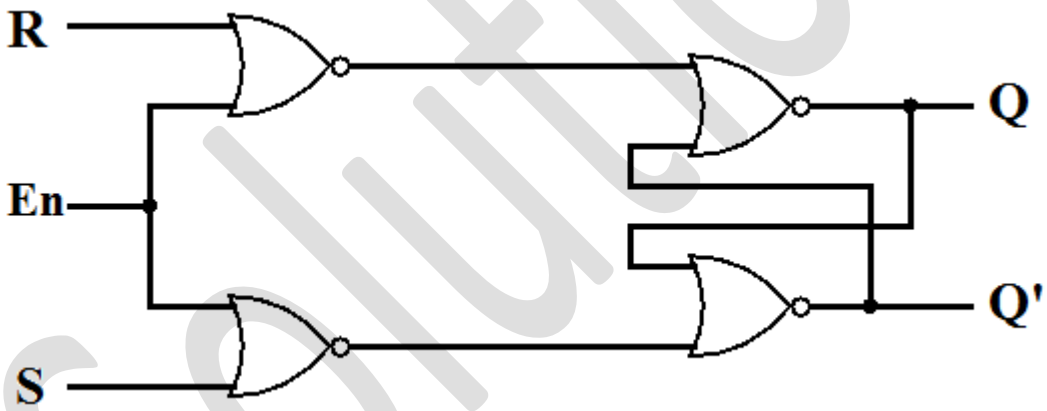
Maximum Marks: 70	**Due Date:** 02 May 2023

Instructions:

- Partially or fully **copied assignments** will be marked as **zero**.
- Only **handwritten** solution on **A4 page** will be accepted.
- Late submissions are not allowed.
- Clearly indicate all the calculations in your solution. No points will be awarded in case of missing calculations.

Question Number 1 **[10 Marks]**

Construct a SR latch by using NOR gates. The latch must have an enable input. Also compute the state table of the latch stating all possible combinations of enable input and S, R inputs.



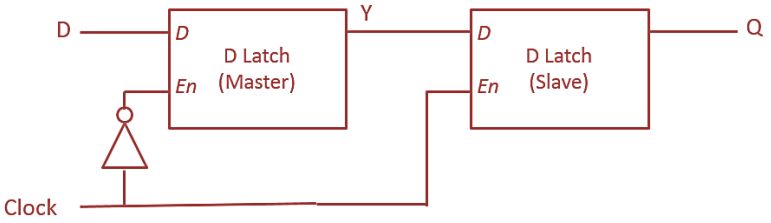
En	S	R	Q	State
1	X	X	Q	No Change
0	0	0	?	Forbidden
0	0	1	1	Set
0	1	0	0	Reset
0	1	1	?	Forbidden

Solution

Question Number 2 **[2.5 x 4 = 10 Marks]**

Write the output Y and Q for the following four cases with proper calculations/reasons. The latches are constructed with NAND gates.

- When clock = 0
- When clock is changing from 0 to 1
- When clock = 1
- When clock is changing from 1 to 0



1) When clock = 0
   - Master latch is enable
   - Slave latch is disable
   - Y = D
   - Q is unchanged
2) When clock is changing from 0 to 1
   - Master latch is disabled
   - Slave latch is enable
   - Q = Y (the value of D will appear at Q at positive edge of clock)
3) When clock = 1
   - Master latch is disabled
   - Slave latch is enable
   - Change in D will not affect Q
4) When clock is changing from 1 to 0
   - Master latch is enable
   - Slave latch is disable
   - Change in D will not affect Q

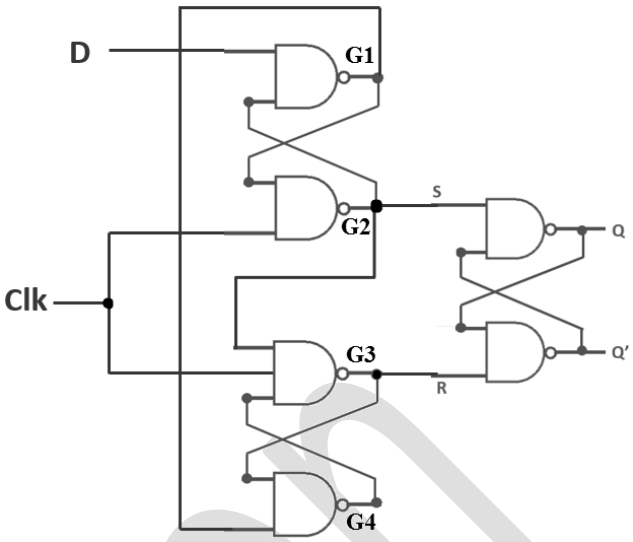
It is a positive edge trigger D flip flop

Solution

Question Number 3 **[2.5 x 4 = 10 Marks]**

Write the output of each gate for the following four cases with proper reasons/calculations.

- When clock = 0
- When clock is changing from 0 to 1
- When clock = 1
- When clock is changing from 1 to 0



1) **When clock = 0**
   - G2 = (0.G1)' = 1
   - G3 = (0.G2.G4)' = 1
   - S = R = 1
   - D = X
   - No change in state
2) **When clock is changing from 0 to 1**
   - **D = 0**
   - G1 = (1.0)' = 1
   - S = G2 = (1.1)' = 0
   - R = G3 = (1.0.G4)' = 1
   - G4 = (1.1)' = 0
   - Q = 1 (Set State)
3) **When clock is changing from 0 to 1**
   - **D = 1**
   - G1 = (1.1)' = 0
   - S = G2 = (1.0)' = 1
   - G4 = (0.1)' = 1
   - R = G3 = (1.1.1)' = 0
   - Q = 0 (Reset State)
4) **When clock = 1**
   - No further change in state as discussed in above two cases
5) **When clock is changing from 1 to 0**
   - G2 = (0.G1)' = 1
   - G3 = (0.G2.G4) = 1
   - S = R = 1
   - D = X
   - No change in state

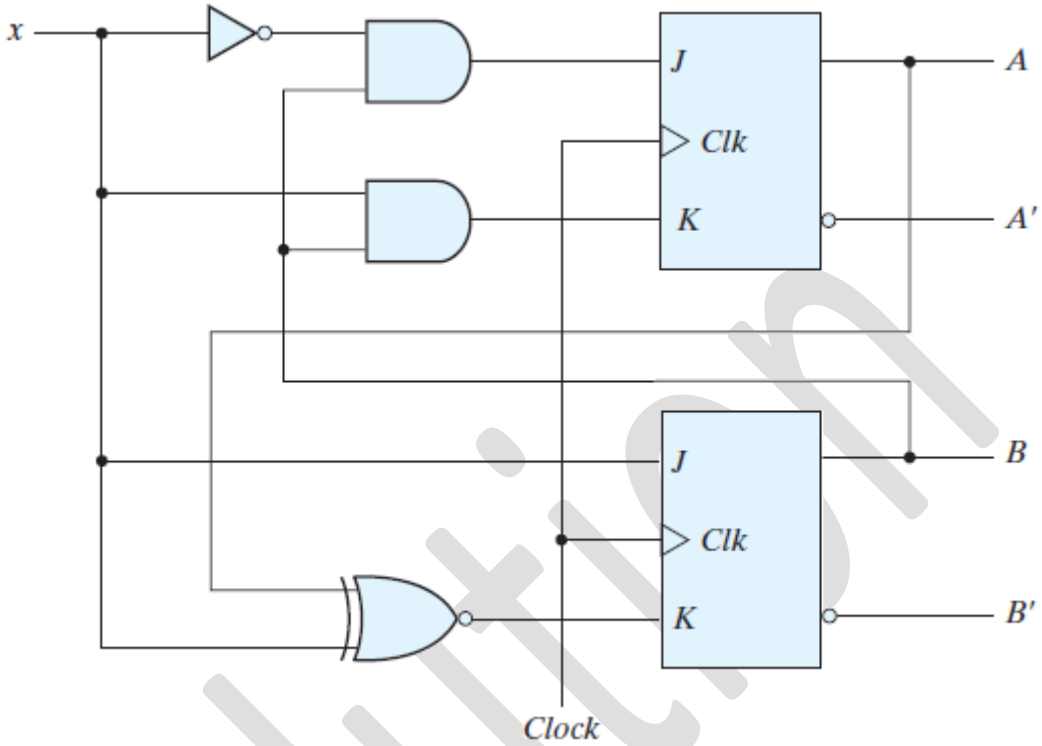
It is a positive edge trigger D flip flop

Solution

Question Number 4 **[4 + 4 + 2 = 10 Marks]**

Analyze the following combinational circuit to find its

i) State equation(s)
ii) State table
iii) State diagram



From circuit diagram

$J_A = x'B$ $K_A = xB$

$J_B = x$ $K_B = (x \oplus A)'$

For JK Flop flop we have

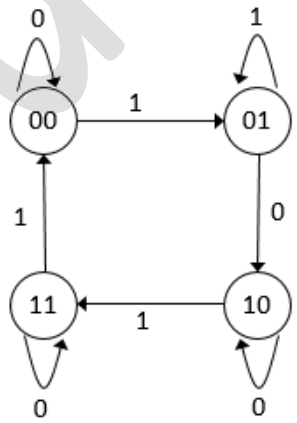
$Q(t + 1) = JQ' + K'Q$

For Flip Flop A

$A = x'BA' + (xB)'A$

For Flip Flop A

$B = xB' + (x \oplus A)B$



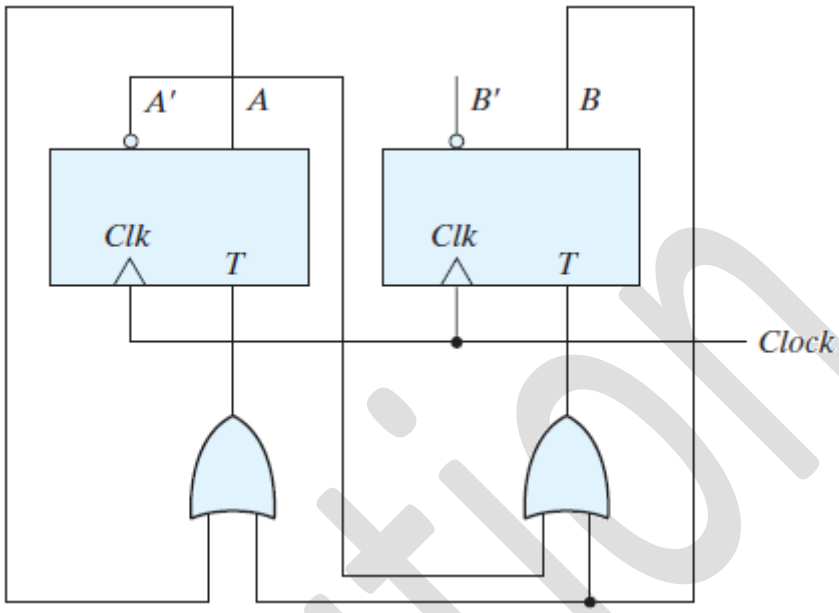
Present State		Input					Next State	
A	**B**	**x**	**x'BA'**	**(xB)'A**	**xB'**	**(x ⊕ A)B**	**A**	**B**
0	0	0	0	0	0	0	0	0
0	0	1	0	0	1	0	0	1
0	1	0	1	0	0	0	1	0
0	1	1	0	0	0	1	0	1
1	0	0	0	1	0	0	1	0
1	0	1	0	1	1	0	1	1
1	1	0	0	1	0	1	1	1
1	1	1	0	0	0	0	0	0

Solution

Question Number 5 **[4 + 4 + 2 = 10 Marks]**

Analyze the following combinational circuit to find its

i) State equation(s)
ii) State table
iii) State diagram

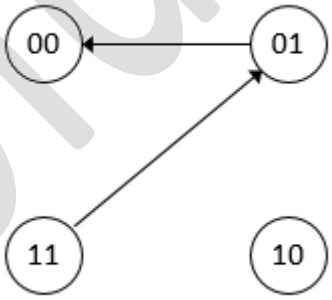


From circuit diagram
$T_A = AB$
$T_B = A'B$

For T Flop flop we have
$Q(t + 1) = T \oplus Q$

For Flip Flop A
$A = AB \oplus A$

For Flip Flop B
$B = A'B \oplus B$



Present State				Next State	
A	**B**	**A'B**	**AB**	**A**	**B**
0	0	0	0	0	0
0	1	1	0	0	0
1	0	0	0	1	0
1	1	0	1	0	1

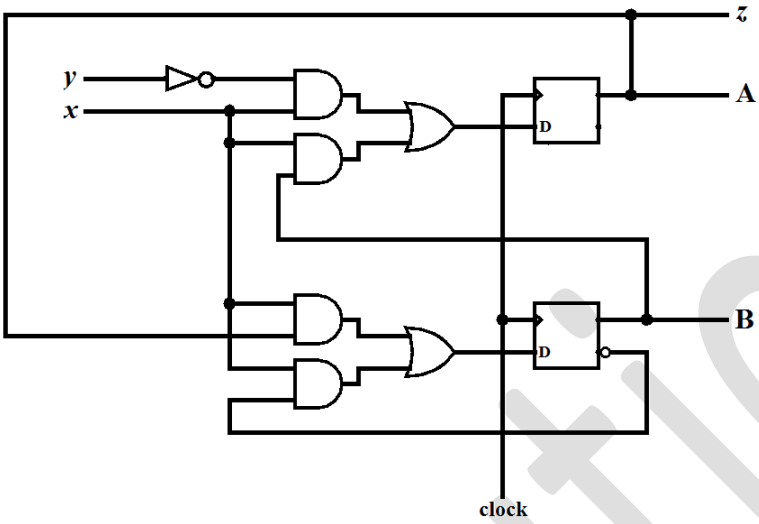
Solution

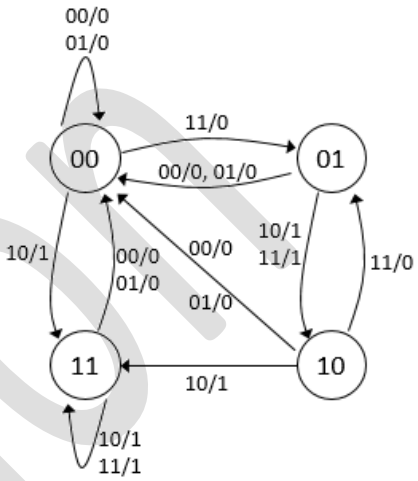
Question Number 6 **[4 + 4 + 2 = 10 Marks]**

A sequential circuit with two D flip-flops A and B, two inputs, x and y ; and one output z is specified by the following next-state and output equations.

$$A(t + 1) = xy' + xB$$
$$B(t + 1) = xA + xB'$$
$$z = A$$

- Draw the logic diagram of the circuit
- List the state table for the sequential circuit
- Draw the corresponding state diagram





Present State		Inputs						Next State		Output
A	B	x	y	xy'	xB	xA	xB'	A	B	z
0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	1	1	1	1
0	0	1	1	0	0	0	1	0	1	0
0	1	0	0	0	0	0	0	0	0	0
0	1	0	1	0	0	0	0	0	0	0
0	1	1	0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0	1	0	1
1	0	0	0	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0	0	0	0
1	0	1	0	1	0	1	1	1	1	1
1	0	1	1	0	0	1	1	0	1	0
1	1	0	0	0	0	0	0	0	0	0
1	1	0	1	0	0	0	0	0	0	0
1	1	1	0	1	1	1	0	1	1	1
1	1	1	1	0	1	1	0	1	1	1

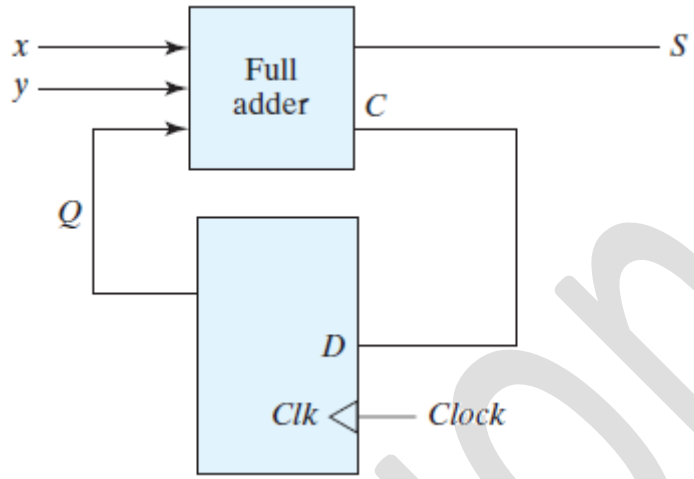
Question Number 7 **[5 + 5 = 10 Marks]**

A sequential circuit has one flip-flop Q, two inputs x and y, and one output S. It consists of a full-adder circuit connected to a D flip-flop, as shown in figure below.

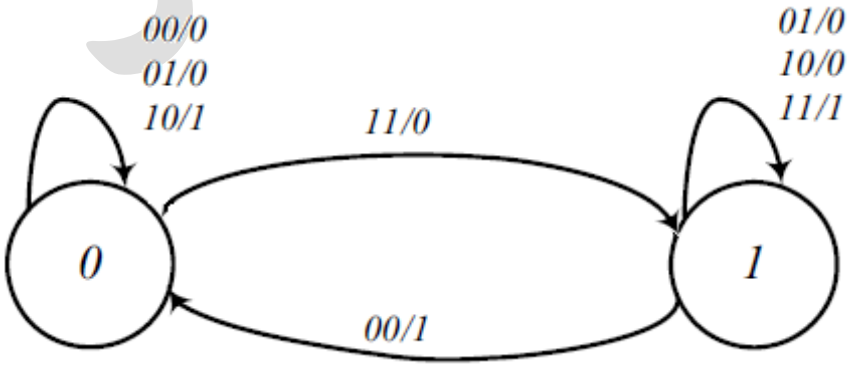
Derive the:

- State table and
- State diagram

of the sequential circuit.



Present State	Inputs		Output		Next State
Q	**x**	**y**	**S**	**C**	**Q**
0	0	0	0	0	0
0	0	1	1	0	0
0	1	0	1	0	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	0	1	1
1	1	0	0	1	1
1	1	1	1	1	1



Solution