EE1005 – Digital Logic Design

Assignment 4 (Solution)

Spring 2023

Maximum Marks: 100	**Due Date:** 31 March 2023

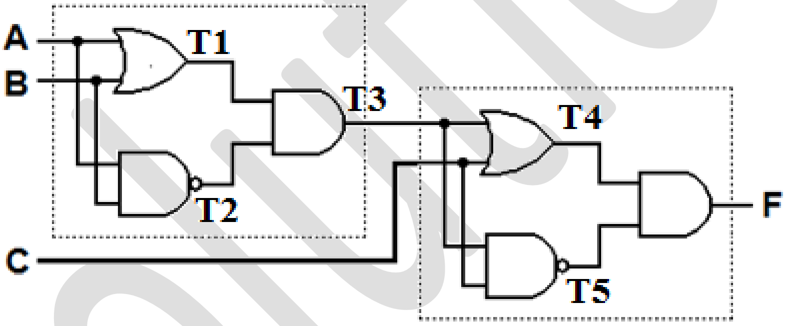
Instructions:

- Partially or fully **copied assignments** will be marked as **zero**.
- Only **handwritten** solution on **A4 page** will be accepted.
- Late submissions are not allowed.
- Clearly indicate all the calculations in your solution. No points will be awarded in case of missing calculations.
- You can submit your assignment **before 5:00 PM** on/before due date.

Question Number 1 **[5 + 4 + 1 = 10 Marks]**

Analyze the following combinational circuit to find its

i) Boolean function
ii) Truth Table



And then conclude that functionality of this circuit.

$T1 = A + B$ $T2 = (AB)'$ $T3 = T1T2$

$T4 = T3 + C$ $T5 = (T3C)'$ $F = T4T5$

$F = T4T5 = [(T3 + C)(T3C)'] = [(T3' + C')(T3 + C)] = T3'C + T3C'$

$F = (T1T2)'C + T1T2C' = (T1' + T2')C + (AB)'(A + B)C'$

$F = [(A + B)' + \{(AB)'\}']C + (A' + B')(A + B)C'$

$F = A'B'C + ABC + A'BC' + AB'C'$

$F = A \oplus B \oplus C$

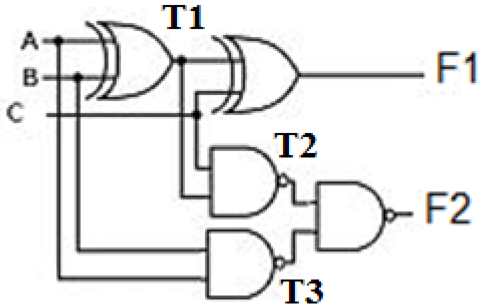
A	B	C	T1	T2	T3	T4	T5	F
0	0	0	0	1	0	0	1	0
0	0	1	0	1	0	1	1	1
0	1	0	1	1	1	1	1	1
0	1	1	1	1	1	1	0	0
1	0	0	1	1	1	1	1	1
1	0	1	1	1	1	1	0	0
1	1	0	1	0	0	0	1	0
1	1	1	1	0	0	1	1	1

This is a circuit of 3 input XOR function.

Question Number 2 **[5 + 4 + 1 = 10 Marks]**

Analyze the following combinational circuit to find its

i) Boolean functions of outputs
ii) Truth Table



And then conclude that functionality of this circuit.

T1 = A⊕B F1 = T1⊕C
T2 = (T1C)' T3 = (AB)'
F2 = (T2T3)'

F1 = T1⊕C = A⊕B⊕C

F2 = (T2T3)' = T2' + T3' = ((T1C)')' + ((AB)')' = T1C + AB = (A⊕B)C + AB
F2 = A'BC + AB'C + AB

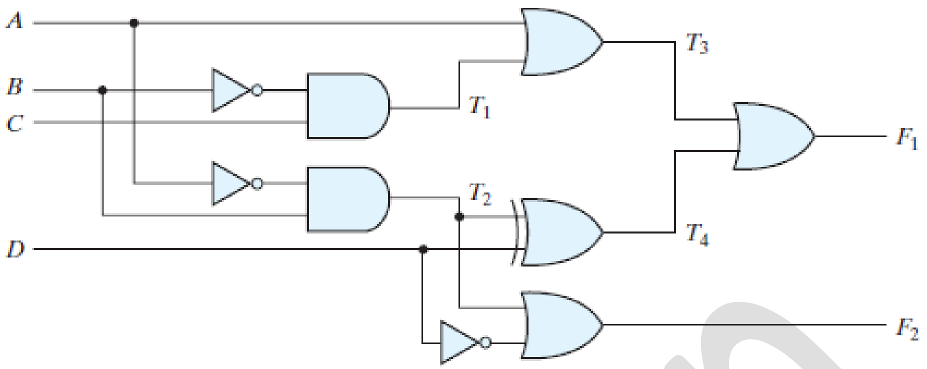
A	B	C	T1	T2	T3	F1	F2
0	0	0	0	1	1	0	0
0	0	1	0	1	1	1	0
0	1	0	1	1	1	1	0
0	1	1	1	0	1	0	1
1	0	0	1	1	1	1	0
1	0	1	1	0	1	0	1
1	1	0	0	1	0	0	1
1	1	1	0	1	0	1	1

This is a circuit of a full adder. Where F1 is sum and F2 is carry.

Question Number 3 **[7 + 3 = 10 Marks]**

Analyze the following combinational circuit to find its

i) Boolean functions of outputs
ii) Truth Table



T1 = B’C T2 = A’B T3 = A + T1 T4 = T2⊕D
F1 = T3 + T4 F2 = T2 + D’

F1 = T3 + T4 = A + T1 + T2⊕D = A + B’C + T2’D + T2D’ = A + B’C + (A’B)’D + A’BD’
F1 = A + B’C + AD + B’D + A’BD’

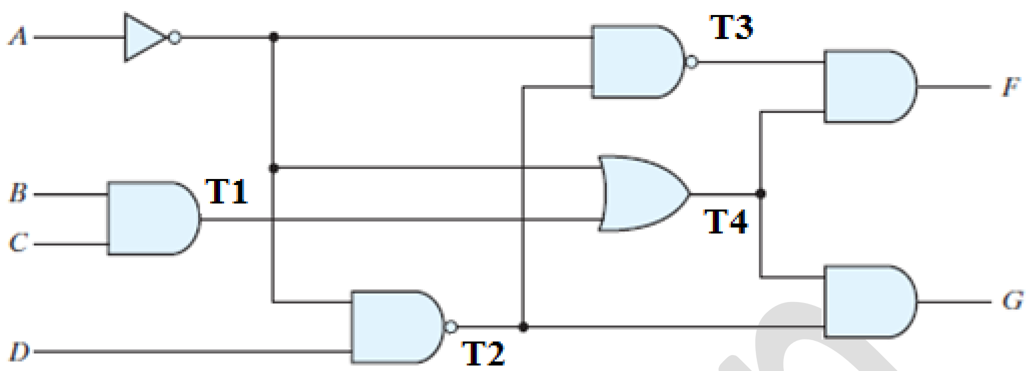
F2 = T2 + D’ = A’B + D’

A	B	C	D	A’	B’	D’	T1	T2	T3	T4	F1	F2
0	0	0	0	1	1	1	0	0	0	0	0	1
0	0	0	1	1	1	0	0	0	0	1	1	0
0	0	1	0	1	1	1	1	0	1	0	1	1
0	0	1	1	1	1	0	1	0	1	1	1	0
0	1	0	0	1	0	1	0	1	0	1	1	1
0	1	0	1	1	0	0	0	1	0	0	0	1
0	1	1	0	1	0	1	0	1	0	1	1	1
0	1	1	1	1	0	0	0	1	0	0	0	1
1	0	0	0	0	1	1	0	0	1	0	1	1
1	0	0	1	0	1	0	0	0	1	1	1	0
1	0	1	0	0	1	1	1	0	1	0	1	1
1	0	1	1	0	1	0	1	0	1	1	1	0
1	1	0	0	0	0	1	0	0	1	0	1	1
1	1	0	1	0	0	0	0	0	1	1	1	0
1	1	1	0	0	0	1	0	0	1	0	1	1
1	1	1	1	0	0	0	0	0	1	1	1	0

Question Number 4 **[7 + 3 = 10 Marks]**

Analyze the following combinational circuit to find its

i) Boolean functions of outputs
ii) Truth Table



T1 = BC T2 = (A'D)' T3 = (A'T2)' T4 = A' + T1
F = T3T4 G = T4T2

F = T3T4 = (A'T2)'(A' + T1) = (A + T2)(A' + T1) = (A + (A'D)')(A' + BC)
F = (A + A + D')(A' + BC) = (A + D')(A' + BC)
F = ABC + A'D' + BCD'

G = T4T2 = (A' + T1)(A'D)' = (A' + BC)(A + D')
G = A'D' + ABC + BCD'

A	B	C	D	A'	T1	T2	T3	T4	F	G
0	0	0	0	1	0	1	0	1	0	1
0	0	0	1	1	0	0	1	1	1	0
0	0	1	0	1	0	1	0	1	0	1
0	0	1	1	1	0	0	1	1	1	0
0	1	0	0	1	0	1	0	1	0	1
0	1	0	1	1	0	0	1	1	1	0
0	1	1	0	1	1	1	0	1	0	1
0	1	1	1	1	1	0	1	1	1	0
1	0	0	0	0	0	1	1	0	0	0
1	0	0	1	0	0	1	1	0	0	0
1	0	1	0	0	0	1	1	0	0	0
1	0	1	1	0	0	1	1	0	0	0
1	1	0	0	0	0	1	1	0	0	0
1	1	0	1	0	0	1	1	0	0	0
1	1	1	0	0	1	1	1	1	1	1
1	1	1	1	0	1	1	1	1	1	1

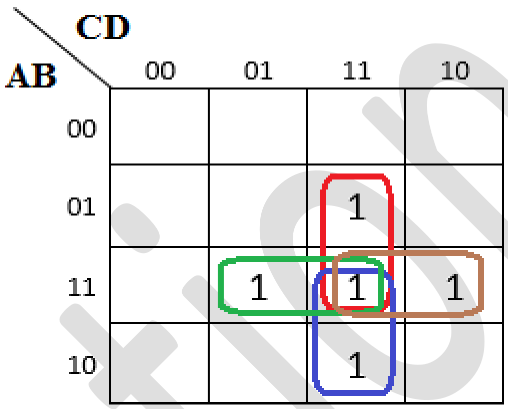
Question Number 5 **[2 + 5 + 2 + 1 = 10 Marks]**

A majority circuit is a combinational circuit whose output is equal to 1 if the input variables have more 1's than 0's. The output is 0 otherwise. Design a 4 input majority circuit by finding:

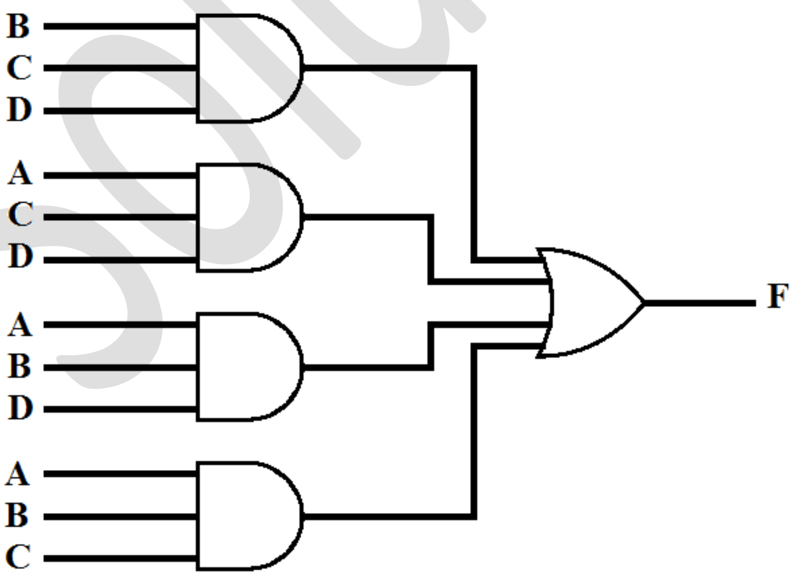
i) No. of inputs and outputs
ii) Truth Table
iii) Simplified expressions of outputs
iv) Logic Diagram

4 Inputs and 1 output

A	B	C	D	F
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1



$$F = BCD + ACD + ABD + ABC$$



Question Number 6 **[2 + 5 + 2 + 1 = 10 Marks]**

Design a combinational circuit to convert a 4 bit gray code to 4 bit binary number. Complete your design by finding the:

i) No. of input(s) and output(s)
ii) Truth Table
iii) Simplified expression(s) of output(s)
iv) Logic Diagram

4 Inputs and 4 output

G_3	G_2	G_1	G_0	B_3	B_2	B_1	B_0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	1
0	1	0	1	0	1	1	0
0	1	1	0	0	1	0	0
0	1	1	1	0	1	0	1
1	0	0	0	1	1	1	1
1	0	0	1	1	1	1	0
1	0	1	0	1	1	0	0
1	0	1	1	1	1	0	1
1	1	0	0	1	0	0	0
1	1	0	1	1	0	0	1
1	1	1	0	1	0	1	1
1	1	1	1	1	0	1	0

G_3G_2 \ G_1G_0	00	01	11	10
00				
01				
11	1	1	1	1
10	1	1	1	1

$B_3 = G_3$

G_3G_2 \ G_1G_0	00	01	11	10
00				
01	1	1	1	1
11				
10	1	1	1	1

$B2 = G_3'G_2 + G_3G_2'$

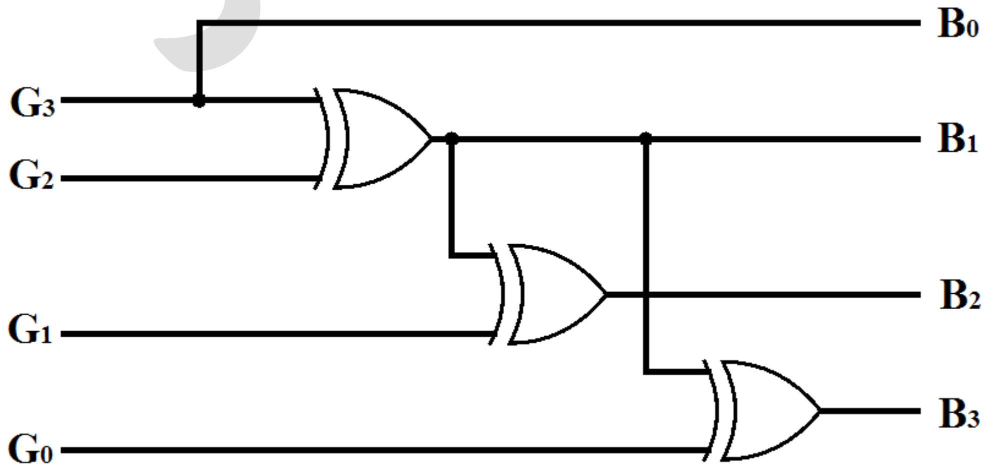
$B_2 = G_3 \oplus G_2$

G_3G_2 \ G_1G_0	00	01	11	10
00			1	1
01	1	1		
11			1	1
10	1	1		

$B_1 = G_3 \oplus G_2 \oplus G_1$

G_3G_2 \ G_1G_0	00	01	11	10
00		1		1
01	1		1	
11		1		1
10	1		1	

$B_0 = G_3 \oplus G_2 \oplus G_1 \oplus G_0$



Question Number 7 **[2 + 5 + 2 + 1 = 10 Marks]**

Design a 4 bit 2's complement calculator. The output of the circuit is the 2's complement of the input binary number. Complete your design by finding the:

i) No. of input(s) and output(s)
ii) Truth Table
iii) Simplified expression(s) of output(s)
iv) Logic Diagram

4 Inputs and 4 output

A	B	C	D	*w*	*x*	*y*	*z*
0	0	0	0	0	0	0	0
0	0	0	1	1	1	1	1
0	0	1	0	1	1	1	0
0	0	1	1	1	1	0	1
0	1	0	0	1	1	0	0
0	1	0	1	1	0	1	1
0	1	1	0	1	0	1	0
0	1	1	1	1	0	0	1
1	0	0	0	1	0	0	0
1	0	0	1	0	1	1	1
1	0	1	0	0	1	1	0
1	0	1	1	0	1	0	1
1	1	0	0	0	1	0	0
1	1	0	1	0	0	1	1
1	1	1	0	0	0	1	0
1	1	1	1	0	0	0	1

AB \ CD	00	01	11	10
00		1		1
01		1		1
11		1		1
10		1		1

$y = C'D + CD'$

AB \ CD	00	01	11	10
00		1	1	
01		1	1	
11		1	1	
10		1	1	

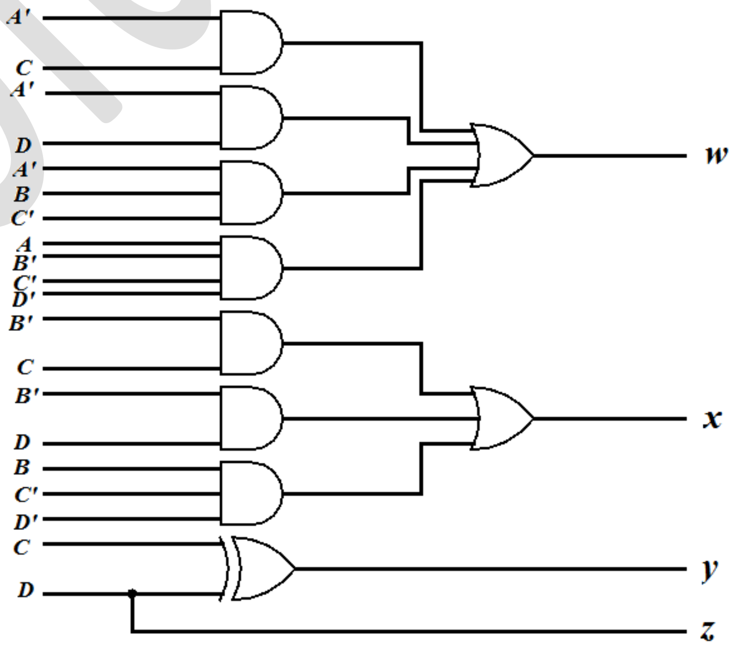
$z = D$

AB \ CD	00	01	11	10
00		1	1	1
01	1	1	1	1
11				
10	1			

$w = A'C + A'D + A'BC' + AB'C'D$

AB \ CD	00	01	11	10
00		1	1	1
01	1			
11	1			
10		1	1	1

$x = B'C + B'D + BC'D'$



Question Number 8 **[2 + 5 + 2 + 1 = 10 Marks]**

Design a combinational circuit whose output is equal to 1 when input is an odd number and multiple of 3, otherwise the output is 0. Your circuit should be capable of taking the input from 0 to 15. Complete your design by finding the:

i) No. of input(s) and output(s)
ii) Truth Table
iii) Simplified expression(s) of output(s)
iv) Logic Diagram

4 Inputs and 1 output

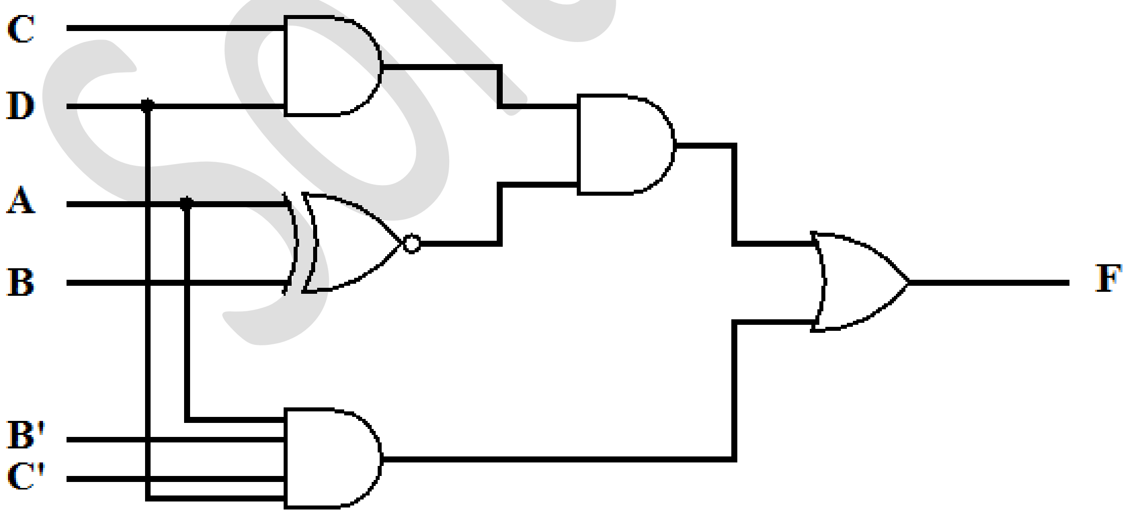
A	B	C	D	F
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

AB \ CD	00	01	11	10
00			1	
01				
11			1	
10		1		

F = A'B'CD + ABCD + AB'C'D

F = CD(A’B’ + AB) + AB’C’D

F = CD(A ⊕ B)’ + AB’C’D



Question Number 9 **[2 + 5 + 2 + 1 = 10 Marks]**

Design a combinational circuit to count the number of 1's in the input sequence of 4 bits. For example, if the input is $(1011)_2$ then the output should be 3 $(011)_2$.

i) No. of input(s) and output(s)
ii) Truth Table
iii) Simplified expression(s) of output(s)
iv) Logic Diagram

4 Inputs and 3 output

A	B	C	D	*x*	*y*	*z*
0	0	0	0	0	0	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	1	0
0	1	0	0	0	0	1
0	1	0	1	0	1	0
0	1	1	0	0	1	0
0	1	1	1	0	1	1
1	0	0	0	0	0	1
1	0	0	1	0	1	0
1	0	1	0	0	1	0
1	0	1	1	0	1	1
1	1	0	0	0	1	0
1	1	0	1	0	1	1
1	1	1	0	0	1	1
1	1	1	1	1	0	0

AB \ CD	00	01	11	10
00				
01				
11			1	
10				

x = ABCD

AB \ CD	00	01	11	10
00		1		1
01	1		1	
11		1		1
10	1		1	

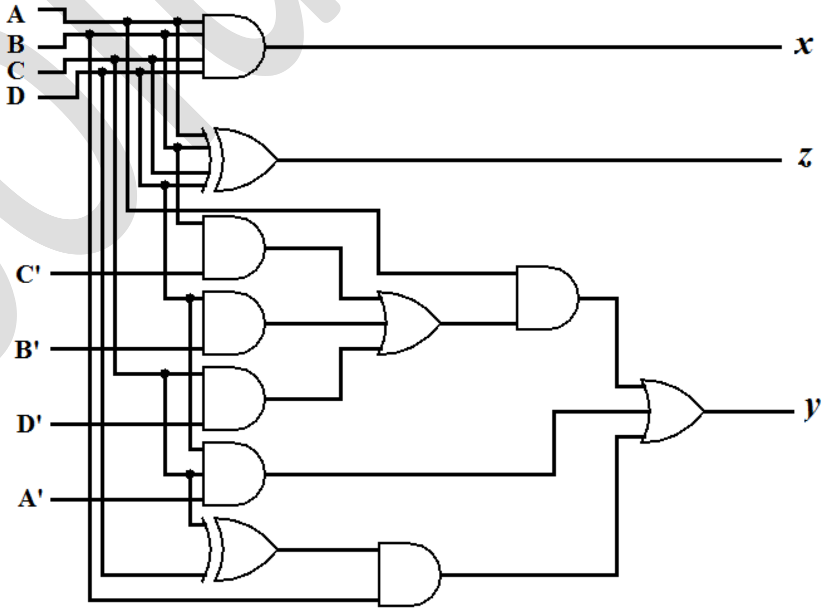
$z = A \oplus B \oplus C \oplus D$

AB \ CD	00	01	11	10
00			1	
01		1	1	1
11	1	1		1
10		1	1	1

$y = ABC' + AB'D + ACD' + BC'D + BCD' + A'CD$

$y = A(BC' + B'D + CD') + B(C'D + CD') + A'CD$

$y = A(BC' + B'D + CD') + B(C \oplus D) + A'CD$



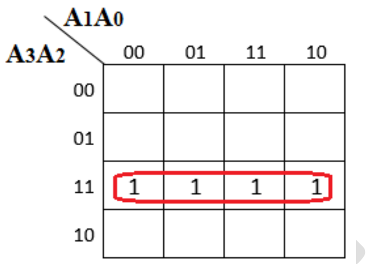
Question Number 10 **[2 + 5 + 2 + 1 = 10 Marks]**

Design a combinational circuit to divide a 4-bit binary number ($A_3A_2A_1A_0$) by a constant 3_{10} and after the division produce the quotient as output. Complete your design by finding the:

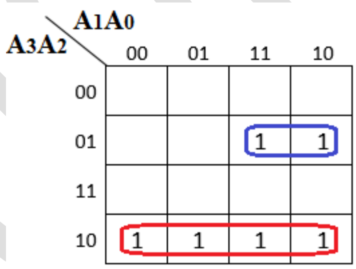
i) No. of input(s) and output(s)
ii) Truth Table
iii) Simplified expression(s) of output(s)
iv) Logic Diagram

4 Inputs and 3 output

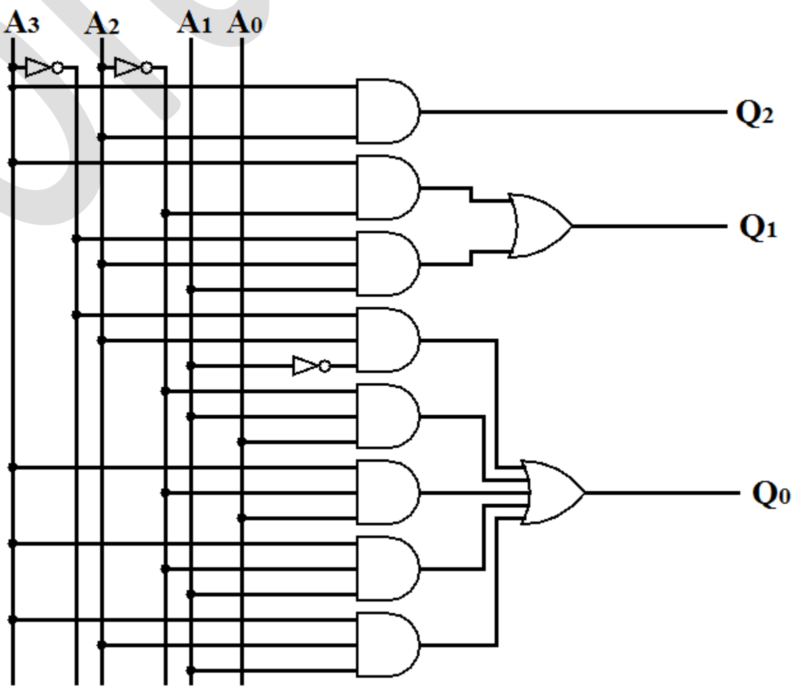
A_3	A_2	A_1	A_0	Q_2	Q_1	Q_0
0	0	0	0	0	0	0
0	0	0	1	0	0	0
0	0	1	0	0	0	0
0	0	1	1	0	0	1
0	1	0	0	0	0	1
0	1	0	1	0	0	1
0	1	1	0	0	1	0
0	1	1	1	0	1	0
1	0	0	0	0	1	0
1	0	0	1	0	1	1
1	0	1	0	0	1	1
1	0	1	1	0	1	1
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	1	0	1

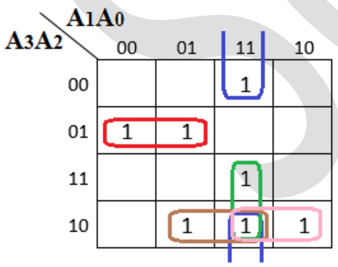


$Q_2 = A_3A_2$



$Q_2 = A_3A_2' + A_3'A_2A_1$





$F = A_3'A_2A_1' + A_2'A_1A_0 + A_3A_2'A_0 + A_3A_2'A_1 + A_3A_1A_0$