Instructor: Muhammad Adeel Tahir   **Sections:** BSE-9A, BSE-9B

Maximum Marks: 255 marks	**Due Date:** 27th July 2024

- Partially or fully **copied assignments** will be marked as **zero**.
- Only **handwritten** solution on **A4 page** will be accepted.
- Submission on the GCR by the deadline is **Compulsory.**
- <u>**Late submissions are not allowed. In case of late submission, assignment will not be accepted.**</u>
- Clearly indicate all the calculations in your solution. No points will be awarded in case of missing calculations.
- You can submit your assignment **during the class** on due date. But submitting on GCR as mentioned is compulsory.
- **Proper calculations including k-map and circuit diagram labelling at each output, simplifications if any are to be implemented, missing steps will receive zero marks in that question straight away.**
- **Only eligible handwriting will be checked, the question shall be liable to receiving a 0 if the not readable at all.**
- <u>**A viva of this assignment will take place and hence not being able to explain your questions will lead to 0 in that specific question.**</u>

Marks Distribution:

Questions	1	2	3	4	5	6	Total
Marks	65	15	40	70	10	55	**255**

Question 1: Decoders & MUX

Outcomes: You must have knowledge of the following after this section for your exam point of view:
Use full-adders to implement a parallel binary adder
Explain the addition process in a parallel binary adder
Discuss the difference between a ripple carry adder and a look-ahead carry adder
State the advantage of look-ahead carry addition
Define carry generation and carry propagation and explain the difference
Develop look-ahead carry logic

a) Design a combinational circuit that takes 3-bit input and at the output it multiplies it by 3 and adds 1 to have the final output. Design this circuit using only 2 × 4 decoders and basic logic gates if necessary.
   i. Properly label and fill the truth table in neat and clean manner for this design.
   ii. Design the circuit diagram for this problem.

b) Your task is to design an electronic circuit for a smart home security system called "Home Guardian." In this system, there are four surveillance cameras positioned around a house. Each camera can either detect motion (HIGH) or no motion (LOW) based on the activity in its field of view. The house is considered secure if at least three out of the four cameras do not detect motion.
   Requirements:
   Surveillance Cameras and Detection:
   There are four surveillance cameras positioned around the house. Each camera can either detect motion (HIGH) or no motion (LOW) based on the activity.
   Security Indicator: The system must include a "secure home indicator" that turns ON if the house is considered secure. For the purpose of this system, define "secure" as at least three out of the four cameras not detecting motion. If the house is not considered secure, the indicator should remain OFF, indicating that the house is at risk.
   Circuit Design:
   Use an 8 X 1 Multiplexer (MUX) to determine whether the house is secure based on the status of the cameras. You may use basic logic gates if necessary to assist in the design.
   Determine how the outputs from the cameras will control the selection lines of the MUX to achieve the desired outcome.
   Output Explanation:
   Clearly explain how the MUX and any additional logic gates you use contribute to the final decision of turning the secure home indicator ON or OFF.
   Implement the following:
   A truth table that outlines how different combinations of camera statuses affect the secure home indicator.
   A schematic diagram of the circuit, clearly labeling each input and output carefully.
   A detailed explanation of how the circuit processes the camera statuses to control the secure home indicator. Note: Ensure your design is clear and well-documented, as you will need to explain how it works later.
   Incase the writing is not readable a straight 0 shall be awarded.

c) Use the following 4×1 MUX to create a 8×1 MUX. Label the diagram neatly on the paper.
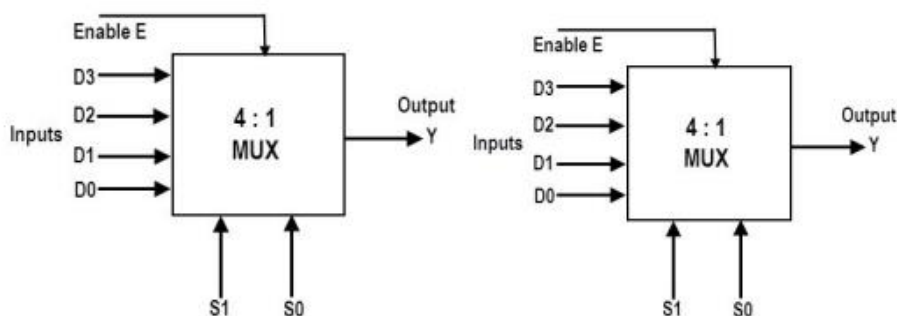
d) Construct a 16 X I multiplexer with two 8 X I and one 2 X I multiplexers. Use block diagrams.
e) Construct 3:8 decoder using 2:4 decoders.

f) Implement a <u>Full adder</u> using **three** 2:4 decoders. **Your design must use 3 number of 2:4 decoders with enable input E, make sure you come up with a very feasible solution to implement it**. To get yourself started first lay down the structure of first 2:4 decoder whose outputs are connected to the enable of 2:4 decoder of the other two decoders after implementing the truth table of the Full adder. (Hint: You will have to ground one of the inputs of decoder in order to make the selections work correctly). The outputs of the first decoder must be grounded which are not of use for us. During design procedure, use step 1, step 2 to indicate your working.

g) Implement the following using 4×1 MUX and external gates, connect A and B to the selection lines. The input requirements for the four data lines will be a function of variables C and D. These values are obtained by expressing F as a function of C and D for each of the four cases when AB= 00, 01,10,11. The functions may have to be implemented with external gates:

    i. $F(A,B,C,D) = \sum (1,3,4,11,12,13,14,15)$
    ii. $F(A,B,C,D) = \sum (1,2,4,7,8,9,10,11)$
    iii.   Implement the part i using 8×1 MUX and externals gates if required, a truth table with neat and clean diagram is necessary

h) Design a combinational circuit that takes 3-bit input and at the output it multiplies it by 3 and adds 1 to have the final output. Design this circuit using only 2×4 decoders and basic logic gates if necessary.

    a) Properly label and fill the truth table in neat and clean manner for this design.
    b) Design the circuit diagram for this problem.
    c) Explain the approach in your own words (5-8 lines max). Wrong explanation leads to 0.

i) Using a decoder and external gates, design the combinational circuit defined by the following three Boolean functions:

$F1 = x'yz' + xz$
$F2 = xy'z' + x'y$
$F3 = x'y'z' + xy$

j) Using two 2:4 decoders-with-enable. Add wires, one not gate, and two or gates to implement the functions F and G given in the truth table.

A	B	C	F	G
0	0	0	1	0
0	0	1	0	1
0	1	0	0	0
0	1	1	1	1
1	0	0	1	0
1	0	1	1	0
1	1	0	0	1
1	1	1	1	0

k) i) Implement $F = (0,2,6,7)$ using 3:8 Decoder and an OR gate.
    ii) F1 $(x,y,z) = \sum(2,5,7)$, F2 $(x,y,z) = \sum(2,3,4)$, F3 $= \sum(0,6,7)$. Implement using appropriate decoder and OR gate.

l) Show how two 2-to-1 multiplexers (with no added gates) could be connected to form a 3-to-1 MUX. Input selection should be as follows:

If AB = 00, select I_0
If AB = 01, select I_1
If AB = 1− (B is a don't-care), select I_2

m) Realize a BCD to excess-3 code converter using a 4-to-10 decoder with active low outputs and a minimum number of gates

**Question 2: Functions of Combinational Logic + Adders**

Outcomes: You must have knowledge of the following after this section for your exam point of view:
Use full-adders to implement a parallel binary adder
Explain the addition process in a parallel binary adder
Discuss the difference between a ripple carry adder and a look-ahead carry adder
State the advantage of look-ahead carry addition
Define carry generation and carry propagation and explain the difference
Develop look-ahead carry logic

a) The following system named "Baads" has been designed to help a vision impaired person to read the letters by feeling the dots that are slightly raised. Design a circuit that converts BCD to this new system. The table shows the correspondence between BCD and Baads. Use a multiple-output NAND-gate circuit to design this problem. Truth table, k-map simplifications, equations and circuit diagram must be implemented in steps.

A	B	C	D	W | X
				Z | Y
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	

b) Solve each part carefully related to **Adders** (consult reading material first and do it yourself or else in exam and quizzes you will not be able to attempt similar questions):

    a. A diagram of 1-bit Full adder is given below, you are supposed to make the following parallel adders by utilizing as many 1-bit Full Adders necessary to complete the design. Label each adder's input and output carefully, deciding the LSB and MSB bits.
        a) A 3-bit parallel adder
        b) A 4-bit parallel adder
        c) A 8-bit parallel adder

    b. After designing the above adders, you are required to perform the following operations to confirm whether your adder is working correctly. For this purpose, we will assume an example: $5 = (101)_2 + 3 = (011)_2 = 8$ (1000) is produced. When we apply the binary values as input to the **3-bit** parallel adder the output bits produced by it will indeed be 1000 where 1 will be C_{out} produced by the last adder at the MSB (FA_3). The following numbers are to be verified by the adders, you will choose a suitable adder that you have designed to perform the calculations at every step. **Note: You must draw the diagrams neatly labelling it carefully otherwise no marks shall be given. For every part, draw the adder again.**
        i. $A=(127)_{10}$, **B**$= (23)_8$
        ii. $A= (12)_{10}$, **B**$= (12)_{10}$
        iii. $A = (13)_8$, **B** $= (12)_8$

c) Show how two 74HC283 adders (IC chips are given in the diagram) can be connected to form an 8-bit parallel adder. Show output bits for the following 8-bit input numbers: A= 10111001 and B= 10011110. Draw the diagram
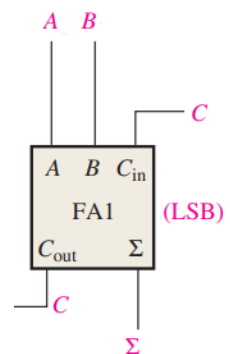
neatly on your paper and label everything in a neat and clean manner. **For this task, you must explain step by step how the bits are being added and calculated as you are labelling the diagram, this will help you understand how the outputs will be generated.** *If you are unable to understand it, you need to attempt part b carefully again. This is very much like the previous part.*


Low-order adder

High-order adder
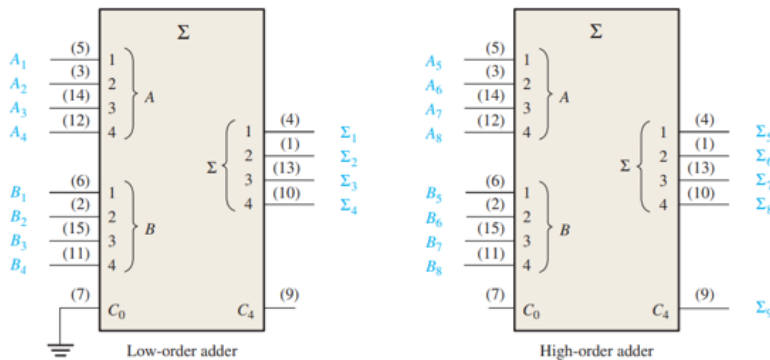
Question 3: Timing Diagrams | Latches & Flip Flops

Outcomes: You must have knowledge of the following after this section for your exam point of view:
How timing diagrams for any circuit is made when given inputs are applied

Note: Consult your reading material attached with this assignment, it is VERY important for exams point of view and quizzes as well.

a) **The Gated S-R Latch:** A gated latch requires an enable input, EN (G is also used to designate an enable input). The logic diagram and logic symbol for a gated S-R latch are shown in Figure.

a. Determine the Q output waveform if the inputs shown in Figure below are applied to a gated S-R latch that is initially RESET.

(a) Logic diagram   (b) Logic symbol
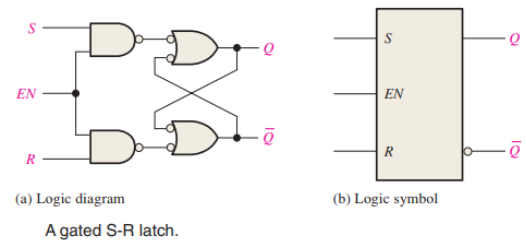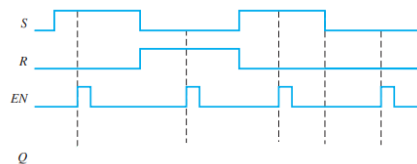
A gated S-R latch.

b. Determine the Q output of a gated S-R latch if the S and R inputs in the timing diagram above are inverted.

c. Draw the truth table of a gated S-R latch.

b) Determine the Q and Q' output waveforms of the flip-flop in **Figure 7–15** for the D and CLK inputs in **Figure 7–16(a).**

a. Assume that the positive edge-triggered flip-flop is initially RESET.

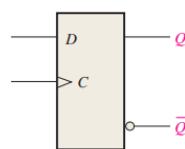b. Determine Q and Q' for the D input in Figure 7–16(a) if the flip-flop is a negative edge-triggered device.
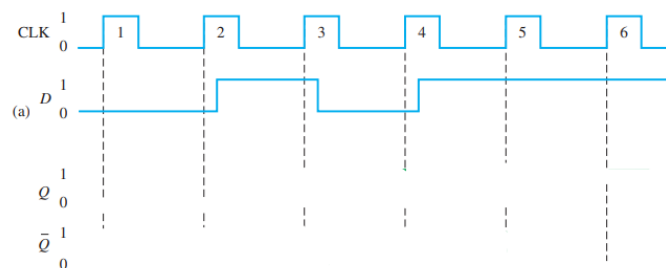

FIGURE 7–15   FIGURE 7–16

c) The waveforms in Figure 7–18(a) are applied to the J, K, and clock inputs as indicated.

a. Determine the Q output, assuming that the flip-flop is initially **RESET**

b. Determine the Q output of the J-K flip-flop if the J and K inputs in Figure 7–18(a) are inverted.
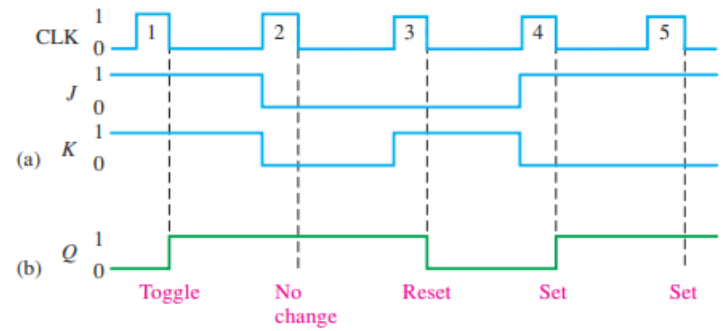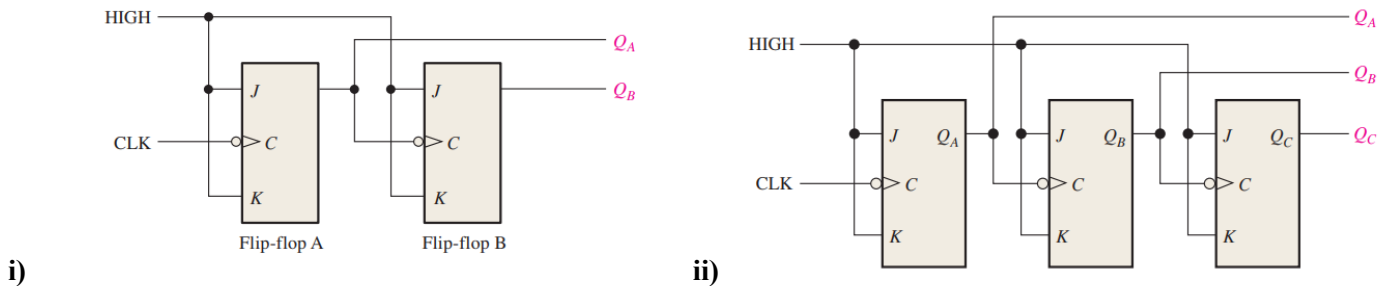

FIGURE 7-18

d) Determine the output waveforms in relation to the clock for QA, QB, and QC in the circuit of F in figure (i) and (ii) and show the binary sequence represented by these waveforms

i)   ii)

Question 4: Counters & Registers

Outcomes: You must have knowledge of the following after this section for your exam point of view:
Make basic counters using flip flops.
Working of all types of registers

For each of the following, draw state diagram, state table, and the corresponding steps required to complete your design where needed.

a) Design a 3-bit simple binary counter using D-Flip Flop.
b) Design a counter that goes from 000→100→111→010→011→000 using T flip flops.
c) Design a counter that goes from 7→0→1→5→1→3→7 using T flip flops.
d) Design a counter with T flip-flops that goes through the following binary repeated sequence: 000, 001, 011, 111, 110, 100. Show that when binary states 010 and 101 are considered as don't care conditions, the counter may not operate properly. Find a way to correct the design.
e) Design a synchronous BCD counter by using: • D Flip Flops • JK Flip. (hint: output y = 1 when BCD values are completely counted)
f) Solve the following:
   a. Suppose that we have two 4-bit shift registers A and B and one external shift control input. Design a circuit for serial transfer of data in such a way that contents of A are transferred to register B and the contents of B are transferred to register A when shift control is equal to 1. And if shift control is equal to 0, no transfer of data should occur.

b. If A = 1101 and B = 0110, show the contents of both registers after every clock pulse for the circuit designed in part (a) of this question.

g) There are basically four main types of flip-flops: SR, D, JK, and T. The major differences in these flip-flop types are in the number of inputs they have and how they change state. For each of these flip-flop types, implement in a clear writing the following:
- Characteristic Table
- State Diagram and Characteristic equations
- Excitation table.

a) Draw the state diagram for the table below that describes a finite-state machine which has one input x and one output z.

Present State	Next State		Output (z)	
	x = 0	x = 1	x = 0	x = 1
A	A	E	1	0
B	C	F	0	0
C	B	H	0	1
D	E	F	0	0
E	D	A	0	1
F	B	F	1	1
G	D	H	0	1
H	H	G	1	0

i. Determine whether it is a mealy machine or moor machine?
ii. Assign the binary codes to all the states by using:
    a. One hot assignment
    b. Binary assignment

b) Reduce the following state table to minimum states and draw the reduced state diagram.

Present State	Next State		Output	
	x = 0	x = 1	x = 0	x = 1
A	A	B	0	0
B	C	D	0	0
C	A	D	0	0
D	E	F	0	1
E	A	F	0	1
F	G	F	0	1
G	A	F	0	1

c) Solve each step carefully.
i. Reduce the given state table to minimum possible number of states.

Present State	Next State		Output	
	$x = 0$	$x = 1$	$x = 0$	$x = 1$
A	A	E	1	0
B	C	F	0	1
C	B	H	1	0
D	B	F	1	0
E	D	F	0	1
F	H	G	1	1
G	D	H	0	1
H	H	G	1	1

ii.   Determine the number of flip flops required to design a sequential circuit described by the above-mentioned state table?

iii. Determine the number of flip flops required to design a sequential circuit described by the reduced state table?

iv.   Draw the state diagram corresponding to the reduced state table.

v.   Design the circuit described by the reduced state table by using JK flip flop(s).

Question 6: Sequential Circuit – Design and analysis

Outcomes: You must have knowledge of the following after this section for your exam point of view:
Be able to design and analyze the sequential circuits.

Note: All types of these questions must be practiced on your own, incase you just copy paste from different sources (which you will hardly find to solve most of these) you will not be able to solve any of the coming quizzes since quizzes are based upon your assignment pattern. Any case of plagiarism will result in a straight 0 in complete assignment.

a) Design a sequential circuit having one input and one output that will produce an output of 1 for every second 0 it receives and for every second 1 it receives. (10 marks)

> **Example:**
>
> $X(\text{input}) = 0\ 1\ 1\ 0\ 1\ 1\ 1\ 0\ 0\ 0\ 0\ 1\ 0\ 1\ 1\ 0\ 0\ 1\ 0\ 1\ 1\ 0\ 1\ 0$
> $Z(\text{output}) = 0\ 0\ 1\ 1\ 0\ 1\ 0\ 0\ 1\ 0\ 1\ 1\ 0\ 0\ 1\ 1\ 0\ 0\ 1\ 1\ 0\ 0\ 1\ 1$

Design a Mealy sequential circuit using D flip-flops, showing a reduced state graph, and equations for the output and D inputs. It should be a reasonably economical design.

b) Consider the following state diagram for a synchronous circuit with one input X and one output Z. Design the below machine by using T Flip Flop(s).

(5 marks)
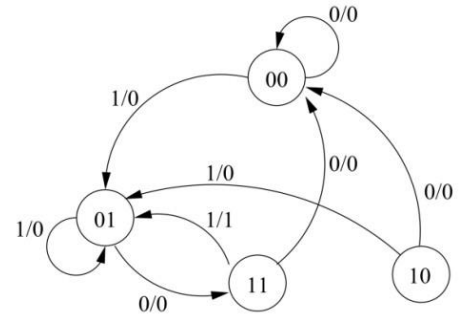
c) Create a sequential circuit utilizing two JK flip-flops labeled A and B, alongside two inputs, E and F. When E is set to 0, the circuit should preserve its current state, disregarding any changes in F. When E equals 1 and F also equals 1, the circuit should follow a sequence of state transitions: starting from 00, moving to 01, then to 10, subsequently to 11, and finally returning to 00, repeating this cycle indefinitely. Conversely, when E is 1 and F is 0, the circuit should adhere to a different sequence of state transitions: beginning at 00, progressing to 11, then to 10, moving to 01, and finally circling back to 00, continuously repeating this pattern. **(10 marks)**

d) Given below is the circuit diagram *(figure 1)* **of a synchronous (same clock is applied to both flip flops) sequential circuit with two flip flops (JK), one input x, and no output.** Analyze the given circuit to find the: (5)

- State Equation(s)
- State Table
- State Diagram

e) A sequential circuit with two D Flip-Flops, A and B; two inputs, x and y; and one output, z, is specified by the following next-state and output equations: (5)

$$A(t + 1) = x'y + xA$$
$$B(t + 1) = x'B + xA$$
$$z = B$$

i. Draw the logic diagram of the circuit.
ii. List the state table for the sequential circuit.
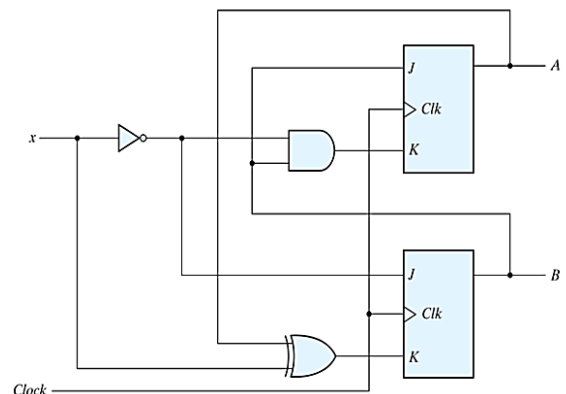iii. Draw the corresponding state diagram.

Figure 1

f) **Construct a sequential circuit incorporating two D flip-flops, denoted as A and B, along with a single input, x.**
When x is set to 0, the circuit maintains its current state. Conversely, when x is set to 1, the circuit undergoes a sequence of state transitions as follows: starting from 00, advancing to 01, then to 11, subsequently to 10, and finally returning to 00, continuously repeating this cycle. (5)

g) Draw the state diagram to detect **the sequence 101.** (2)

h) Draw the state diagram to detect **the sequence 00110.** (3)

i) Design a sequential circuit designed to identify sequences of **three or more consecutive 1's** within an input string. The circuit should transition through a series of states that monitor the input and detect the specified pattern. (10)