EE1005 Digital Logic Design

Thursday, May 25, 2023

Course Instructor

Dr. Arslan Ahmed Amin, Amir Zahoor, Muhammad Sajid Iqbal, Muhammad Irfan Ishaq & Waqar Baig

Serial No:

Final Term Exam

Total Time: 3 Hours

Total Marks: 100

_____

Signature of Invigilator

Roll No	Section	Signature

DO NOT OPEN THE QUESTION BOOK OR START UNTIL INSTRUCTED.

Instructions:

1. Verify at the start of the exam that you have a total of ten (10) questions printed on eleven (11) pages including this title page.
2. Attempt all questions on the question-book and in the given order.
3. The exam is closed books, closed notes. Please see that the area in your threshold is free of any material classified as 'useful in the paper' or else there may a charge of cheating.
4. Read the questions carefully for clarity of context and understanding of meaning and make assumptions wherever required, for neither the invigilator will address your queries, nor the teacher/examiner will come to the examination hall for any assistance.
5. Fit in all your answers in the provided space. You may use extra space on the last page if required. If you do so, clearly mark question/part number on that page to avoid confusion.
6. Use only your own stationery.
7. **Use of Calculator is not allowed, use manual calculations.**
8. Use only permanent ink-pens. Only the questions attempted with permanent ink-pens will be considered. Any part of paper done in lead pencil cannot be claimed for checking/rechecking.

	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8	Q9	Q10	**Total**
Total Marks	10	5	10	10	10	10	10	10	15	10	**100**
Marks Obtained											

Vetted By: _____ **Vetter Signature:** _____

University Answer Sheet Required: **No** ☐ **Yes** ☐

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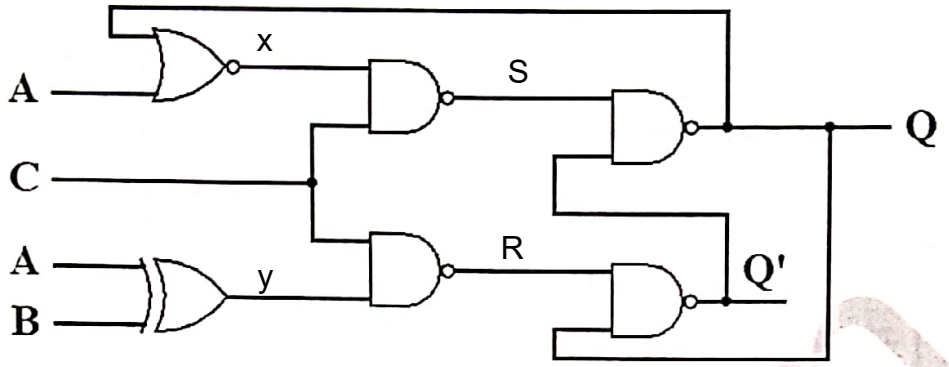
Question Number 1 **(05 + 05 = 10 marks)**

i. An AB latch with two inputs A and B and a control input C is shown below. Analyze the latch for all possible values of A, B, and C and determine the next state.



ii. Consider C = 1 and derive the equation of next state Q(t + 1) in terms of A, B and Q(t) by using k-map.

Part (i)

From the figure we can write that $x = (A + Q)'$ $y = A \oplus B$ $S = (xC)'$ $R = (yC)'$

C = 0, A = B = X

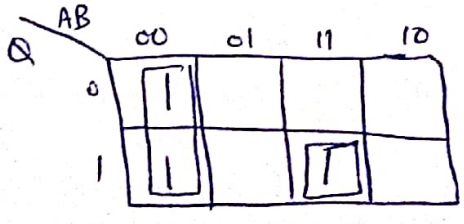
S = (x.0)' = 1
R = (y.0)' = 1
Q = (S.Q')' = (1.Q')' = (Q')' = Q
Q' = (R.Q)' = (1.Q)' = (Q)' = Q'

C = 1, A = 0, B = 1

x = (A + Q)' = (0 + Q)' = Q'
y = A⊕B = 0 ⊕ 1 = 1
S = (x.1)' = (Q')' = Q
R = (y.1)' = (1.1)' = 0
Q = (S.Q')' = (Q.Q')' = 1
Q' = (R.Q)' = (0.1)' = 1

C = 1, A = 1, B = 1

x = (A + Q)' = (1 + Q)' = 0
y = A⊕B = 1 ⊕ 1 = 0
S = (0.1)' = 1
R = (y.1)' = (0.1)' = 1
Q = (S.Q')' = (1.Q')' = (Q')' = Q
Q' = (R.Q)' = (1.Q)' = (Q)' = Q'



C = 1, A = 0, B = 0

x = (A + Q)' = (0 + Q)' = Q'
y = A⊕B = 0 ⊕ 0 = 0
S = (x.1)' = (Q')' = Q
R = (y.1)' = (0.1)' = 1
Q = (S.Q')' = (Q.Q')' = 1
Q' = (R.Q)' = (1.1)' = 0

C = 1, A = 1, B = 0

x = (A + Q)' = (1 + Q)' = 0
y = A⊕B = 1 ⊕ 0 = 1
S = (0.1)' = 1
R = (y.1)' = (1.1)' = 0
Q' = (R.Q)' = (0.Q)' = 1
Q = (S.Q')' = (1.1)' = 0

Part (ii)

Present State	Inputs		Next State
Q(t)	A	B	Q(t + 1)
0	0	0	1
0	0	1	?
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	?
1	1	0	0
1	1	1	1

$Q(t+1) = A'B' + AB\,Q(t)$

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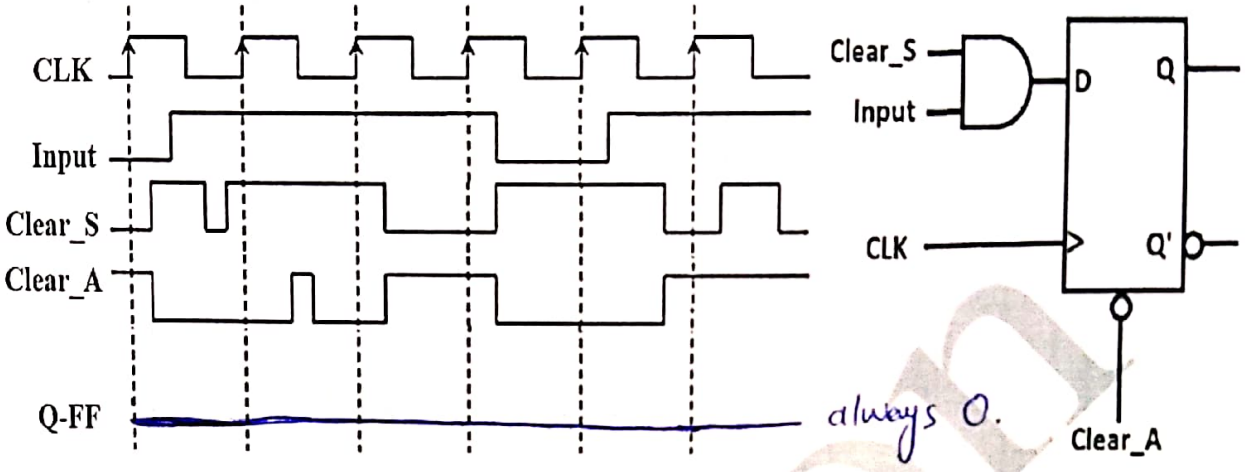
Question Number 2 **(05 Marks)**

Draw the output waveform for a D flip flop shown in figure below. Also describe the difference between Clear_S and Clear_A in the context of this circuit.

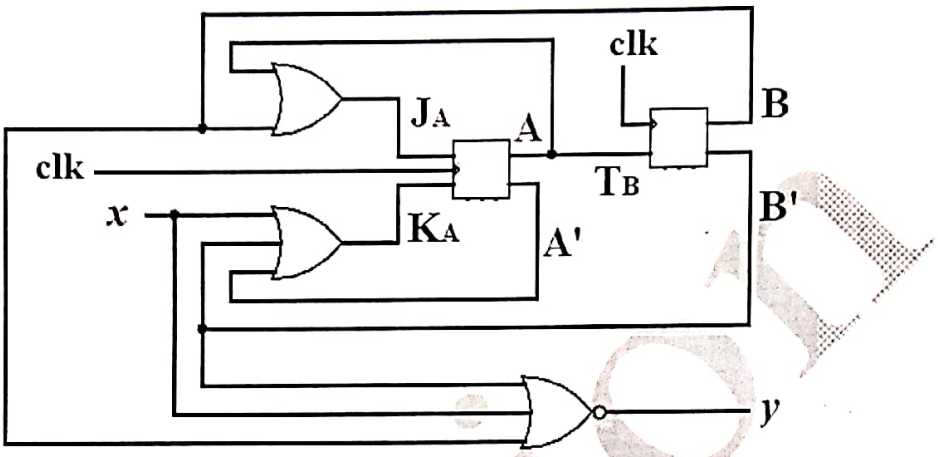


Here clear_A is asynchronous clear and clear_s is synchronous clear.

Question Number 3 **(2 + 5 + 3 = 10 Marks)**

Given below is the circuit diagram of a synchronous (same clock is applied to both flip flops) sequential circuit with two flip flops (JK and T), one input x, and one output y. Analyze the given circuit to find the:

- State Equation(s)
- State Table
- State Diagram



From the figure we can write that:

$J_A = A + B$ $K_A = x + A' + B'$

$T_B = A$ $y = (x + B + B')'$

State Equations

$A(t + 1) = J_A A' + K_A' A = (A + B)A' + (x + A' + B')'A = A'B + x'AB$

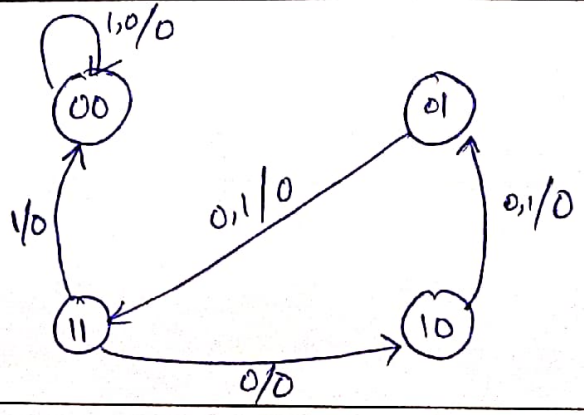
$B(t + 1) = T_B \oplus B = A \oplus B$

$y = (x + B + B')' = (x + 1)' = 0$

State Table

Present State		Input			Next State		Output
A	B	x	A'B	x'AB	A(t + 1)	B(t + 1)	y
0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0
0	1	0	1	0	1	1	0
0	1	1	1	0	1	1	0
1	0	0	0	0	0	1	0
1	0	1	0	0	0	1	0
1	1	0	0	1	1	0	0
1	1	1	0	0	0	0	0

State Diagram



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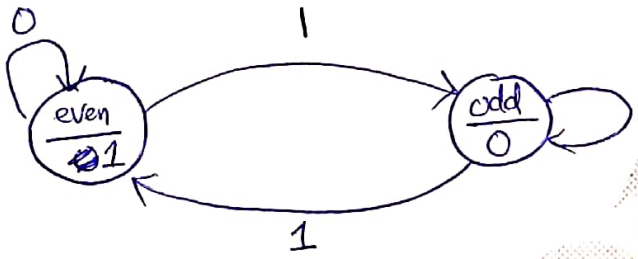
Question Number 4 **(3 + 3 + 2 + 2 = 10 Marks)**

A sequential machine takes a binary sequence (one bit per cycle) as input and gives Y as output. The output Y is 1 if the input is having even number of 1's and Y = 0 otherwise. Design the above-mentioned circuit by using D-Flip Flop(s). You can complete your design by:

- Constructing State Diagram
- State Table
- All the required Equation(s)
- Circuit Diagram



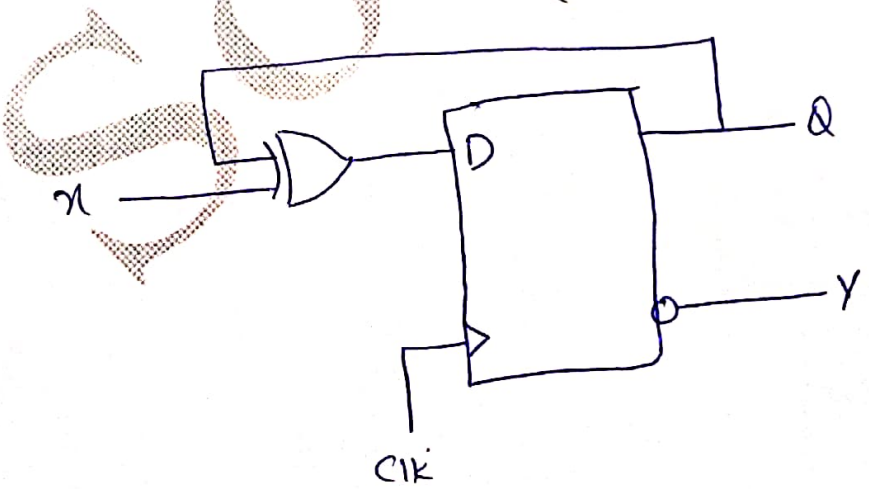
even = 0
odd = 1
State Assignment

Present State	Input	Next State	Output
Q(t)	x	Q(t + 1)	Y
0	0	0	1
0	1	1	1
1	0	1	0
1	1	0	0

For a D flip flop Q(t + 1) = D, hence we need to find the equations of D and Y. From the table it can be clearly seen that:

$$D = Q \oplus X$$

$$Y = Q'$$

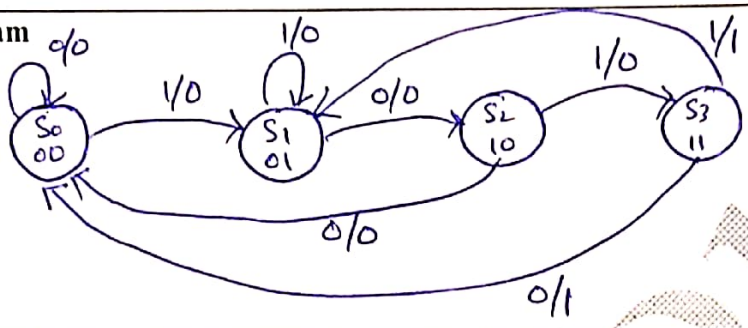


Question Number 5 **(3 + 3 + 2 + 2 = 10 Marks)**

Design a sequential circuit by using JK flip flop(s) to detect the input sequence 101. You can complete your design by:

- Constructing State Diagram
- State Table
- All the required Equation(s)
- Circuit Diagram

State Diagram

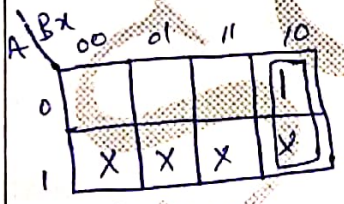


State table

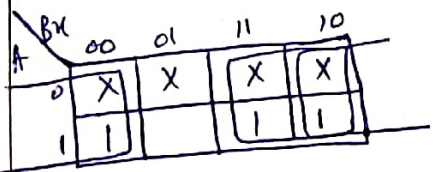
Present State		Input	Next State		Output	Flip Flop Inputs			
A(t)	B(t)	x	A(t+1)	B(t+1)	y	J_A	K_A	J_B	K_B
0	0	0	0	0	0	0	X	0	X
0	0	1	0	1	0	0	X	1	X
0	1	0	1	0	0	1	X	X	1
0	1	1	0	1	0	0	X	X	0
1	0	0	0	0	0	X	1	0	X
1	0	1	1	1	0	X	0	1	X
1	1	0	0	0	1	X	1	X	1
1	1	1	0	1	1	X	1	X	0

Equations and Circuit Diagram

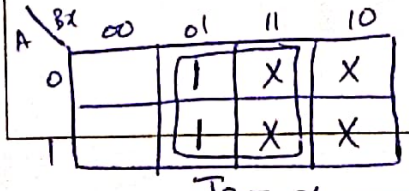
$y = AB$



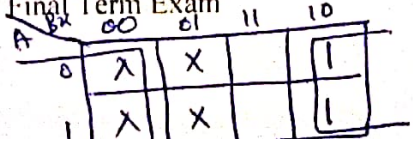
$J_A = Bx'$



$K_A = B + x'$



$J_B = x$



$K_B = x'$

Question Number 6 **(6 + 1 + 1 + 2 = 10 Marks)**

i. Reduce the given state table to minimum possible number of states.

Present State	Next State		Output	
	$x = 0$	$x = 1$	$x = 0$	$x = 1$
A	A	E	1	0
B	C	F	0	1
C	B	H	1	0
D	B	F	1	0
E	D	F	0	1
F	H	G	1	1
G	D	H	0	1
H	H	G	1	1

ii. Determine the number of flip flops required to design a sequential circuit described by the above-mentioned state table?

iii. Determine the number of flip flops required to design a sequential circuit described by the reduced state table?

iv. Draw the state diagram corresponding to the reduced state table.

Part (i)

- F and H are equivalent, remove H and replace H with F.

After replacing H with F

- E and G are equivalent, remove G and replace G with E.
- C and D are equivalent, remove D and replace D with C.

After making the above replacements

- B and E are equivalent, remove E and replace E with B.

The reduced state table is

Present State	Next State		Output	
	$x = 0$	$x = 1$	$x = 0$	$x = 1$
A	A	B	1	0
B	C	F	0	1
C	B	F	1	0
F	F	B	1	1

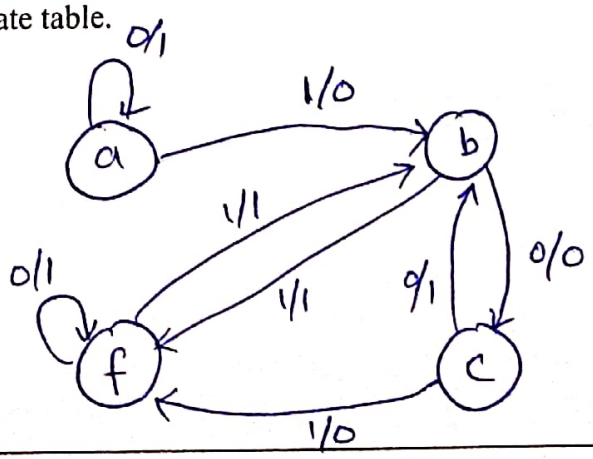
Part (ii)

As there are 8 states in the given table. So, we need 3 flip flops to design the circuit.

Part (iii)

In the reduced state table there are 4 states, hence we need 2 flip flops to design the circuit given by reduced state table.

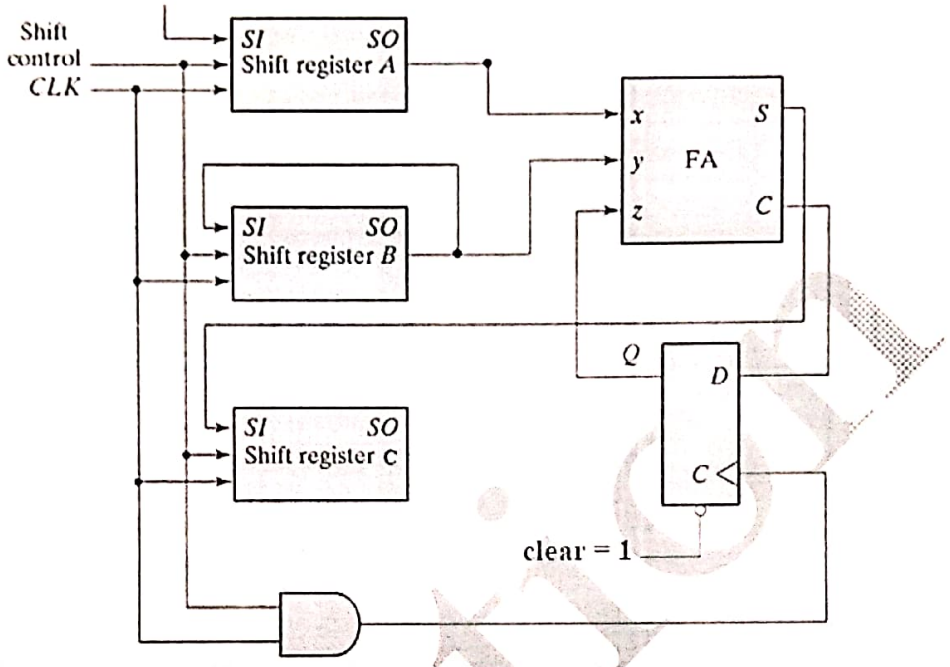
Part (iv)



Question Number 7 **(10 Marks)**

A sequential circuit containing three 4-bit shift registers, a full adder, and a D flip flop is shown below. Determine the contents of shift registers and flip flop after every clock pulse.

0110



Pulse	Shift Register A	Shift Register B	Shift Register C	D	Q
Initial Values	1001	1101	0000	0	0
After T1	0100	1110	0000	1	1
After T2	1010	0111	1000	0	0
After T3	1101	1011	1100	0	0
After T4	0110	1101	0110	1	1

Question Number 8 **(1 + 1 + 1 + 7 = 10 Marks)**

It is required to design a 4 bit universal shift register according to following table.

S_1	S_0	Register Operation
0	0	Shift Left
0	1	Clear register to 0 (asynchronous with the clock)
1	0	Clear register to 0 (synchronous with the clock)
1	1	Shift Right

Determine the

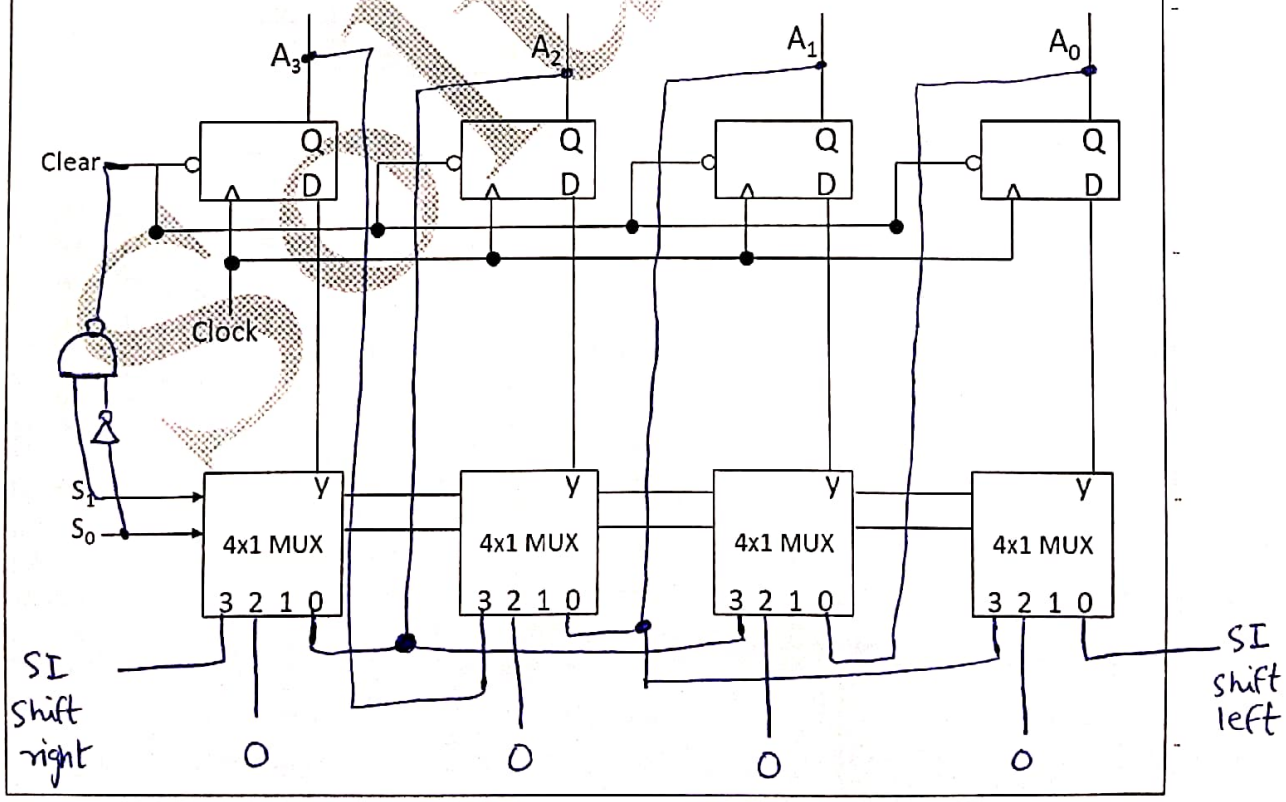
i. No. of D flip flops required
ii. No. of MUX required
iii. Size of each MUX
iv. Draw the circuit diagram

i. Four D flip flops are required

ii. Four MUX will be used

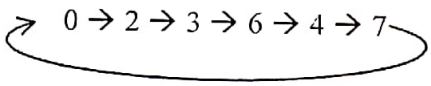
iii. As there are four operations, so 4x1 MUX will be used

iv. Circuit diagram is given below.



Question Number 9 **(10 + 5 = 15 Marks)**

Design a synchronous counter by using T-Flip Flop(s) that counts in the following sequence:

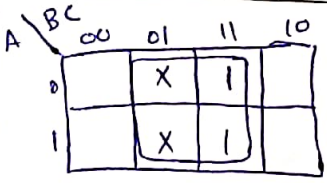


i. Take the unused states as don't care.

ii. Modify the above counter to make it self-correcting (in case of an invalid input, the counter should move to the possible next state, for example if input is 1, then the next state should be 2).

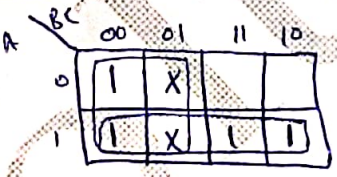
Part (i)

Present State			Next State			Flip Flop Inputs		
A	B	C	A	B	C	T_A	T_B	T_C
0	0	0	0	1	0	0	1	0
0	0	1	X	X	X	X	X	X
0	1	0	0	1	1	0	0	1
0	1	1	1	1	0	1	0	1
1	0	0	1	1	1	0	1	1
1	0	1	X	X	X	X	X	X
1	1	0	1	0	0	0	1	0
1	1	1	0	0	0	1	1	1

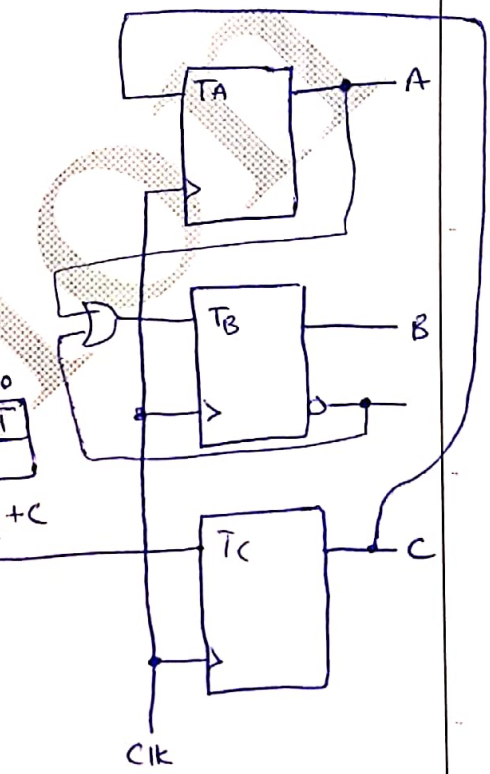


$T_A = C$

$T_C = AB' + A'B + C$

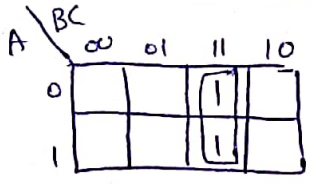


$T_B = A + B'$

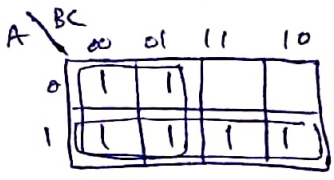


Part (ii)

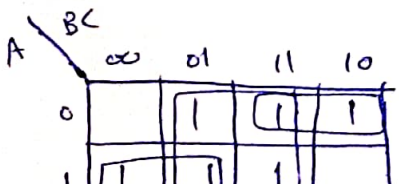
Present State			Next State			Flip Flop Inputs		
A	B	C	A	B	C	T_A	T_B	T_C
0	0	0	0	1	0	0	1	0
0	0	1	0	1	0	0	1	1
0	1	0	0	1	1	0	0	1
0	1	1	1	1	0	1	0	1
1	0	0	1	1	1	0	1	1
1	0	1	1	1	0	0	1	1
1	1	0	1	0	0	0	1	0
1	1	1	0	0	0	1	1	1



$T_A = BC$



$T_B = A + B'$



$T_C = AB' + A'B + C$

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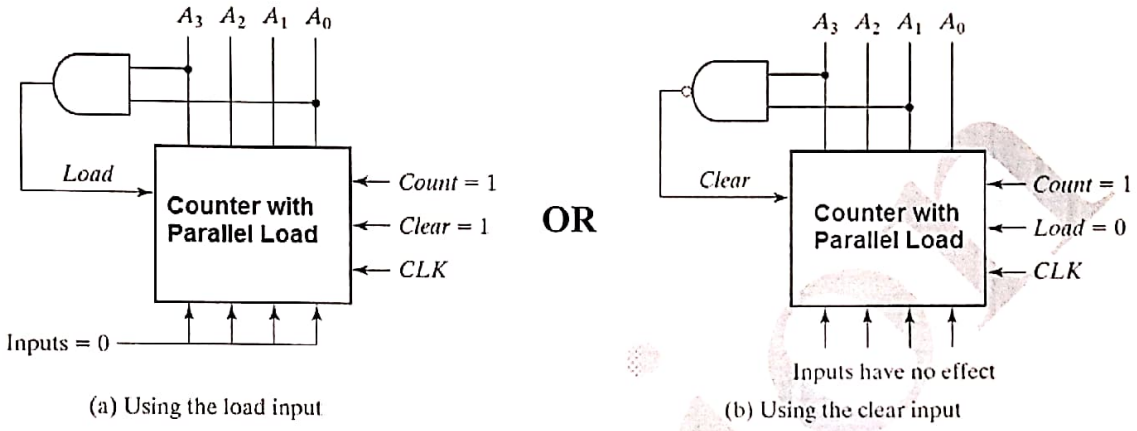
Question Number 10 **(04 + 06 = 10 Marks)**

Use the 4-bit counter with parallel load to design:

i. A BCD counter

ii. A counter that counts from 4 to 12.

Part (i)



(a) Using the load input

(b) Using the clear input

Part (ii)