EE1005 Digital Logic Design

Tuesday, April 11, 2023

Course Instructor

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Serial No:

2nd Sessional Exam

Total Time: 1 Hour

Total Marks: 40

_____

Signature of Invigilator

Roll No	Section	Signature

DO NOT OPEN THE QUESTION BOOK OR START UNTIL INSTRUCTED.

Instructions:

1. Verify at the start of the exam that you have a total of five (5) questions printed on eight (8) pages including this title page.
2. Attempt all questions on the question-book and in the given order.
3. The exam is closed books, closed notes. Please see that the area in your threshold is free of any material classified as 'useful in the paper' or else there may a charge of cheating.
4. Read the questions carefully for clarity of context and understanding of meaning and make assumptions wherever required, for neither the invigilator will address your queries, nor the teacher/examiner will come to the examination hall for any assistance.
5. Fit in all your answers in the provided space. You may use extra space on the last page if required. If you do so, clearly mark question/part number on that page to avoid confusion.
6. Use only your own stationery.
7. **Use of Calculator is not allowed, use manual calculations.**
8. Use only permanent ink-pens. Only the questions attempted with permanent ink-pens will be considered. Any part of paper done in lead pencil cannot be claimed for checking/rechecking.

	Q-1	Q-2	Q-3	Q-4	Q-5	Total
Total Marks	10	10	10	10	10	**40**
Marks Obtained						

Vetted By: _____ **Vetter Signature:** _____

University Answer Sheet Required: **No** ☐ **Yes** ☐

Main Instruction:

BCS students will do the first 04 questions only (They cannot attempt 5th question). The ROBO, AI and SE students can attempt any 4 questions out of 5.

Question Number 1 (05 + 05 = 10 marks)

a) The waveforms in Figure 2 below are observed on the inputs of a 74HC151 8-input multiplexer. Sketch the Y output waveform. (5 marks)

Figure 1: 74HC151 8-Input Multiplexer

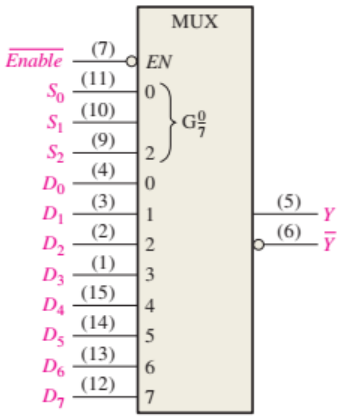
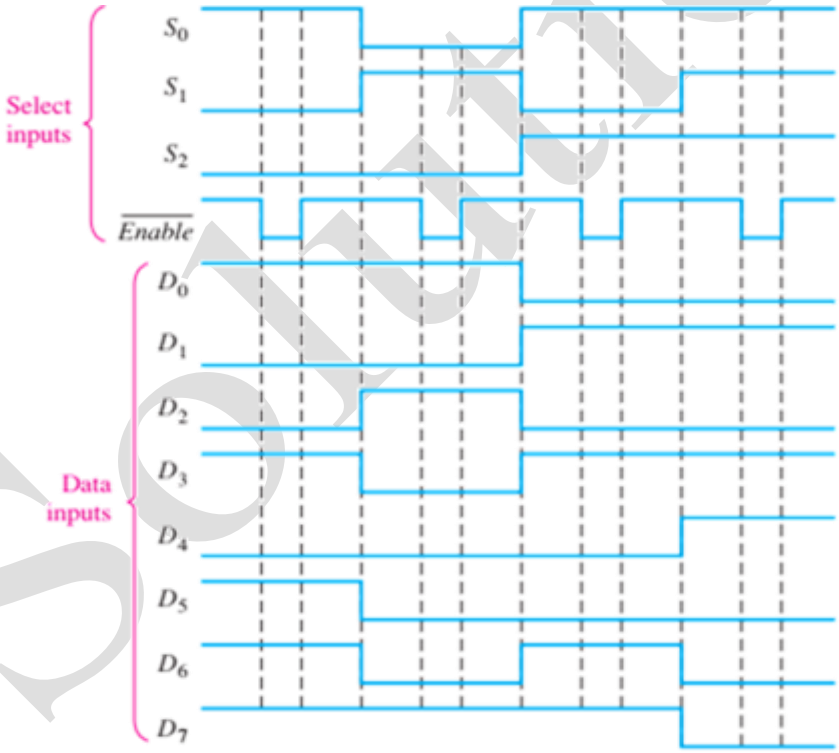
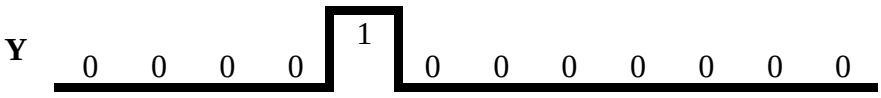


Figure 2: Waveforms of 8X 1 MUX



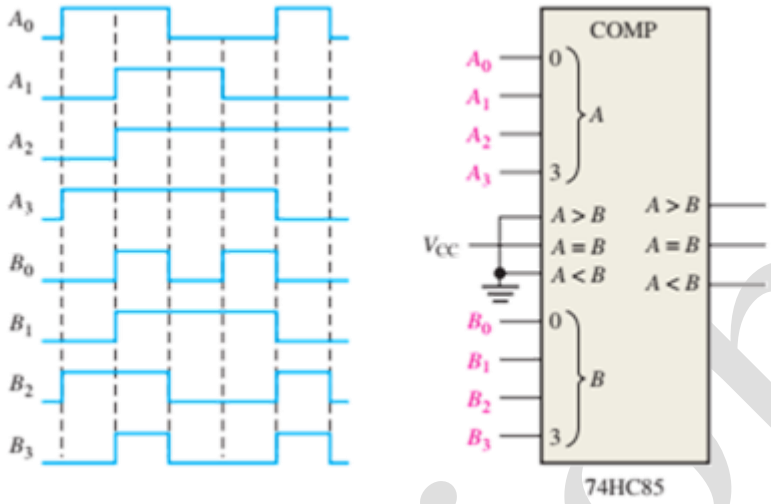
If enable = 1, Y = 0

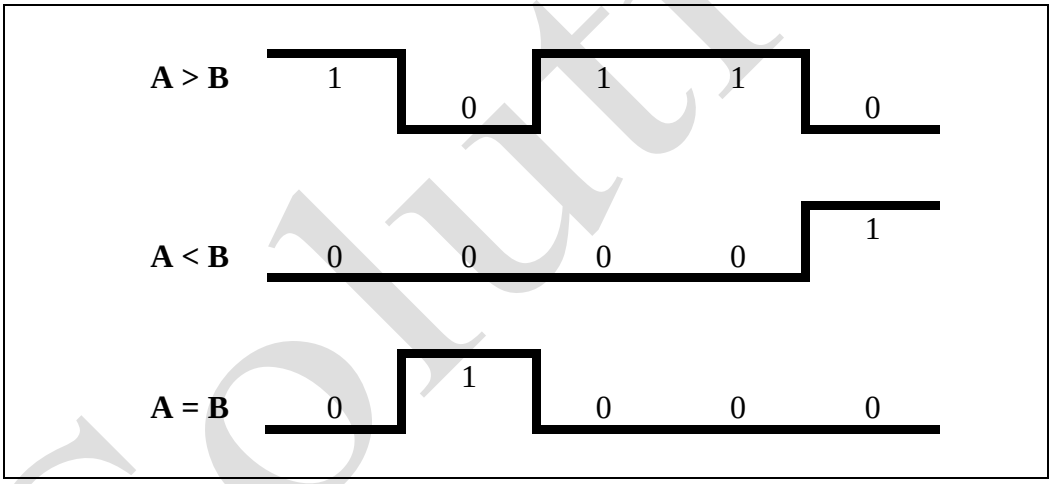
If enable = 0, select the data line depending upon the selection logic



b) For the 4-bit comparator in figure below, plot the output waveforms for A > B, A < B, and A = B for each time interval. The outputs are active-HIGH. (5 marks)

Figure 3: 4- bit comparator waveforms





Question Number 2 **(10 Marks)**

An M-bit thermometer code for the number k consists of k 1's in the least significant bit positions and (M – k) 0's in all the more significant bit positions. A binary-to-thermometer code converter has N inputs and 2^N-1 outputs. It produces a 2^N-1 bit thermometer code for the number specified by the input. For example, if the input is (6) = $(110)_2$, the output should be 0111111. Design a 3:7 binary-to-thermometer code converter by finding:

- The number of input(s), output(s)
- Truth Table
- Simplified Boolean equation for each output
- Sketch a schematic

Number of Inputs = 3
Number of Outputs = 7

Truth Table

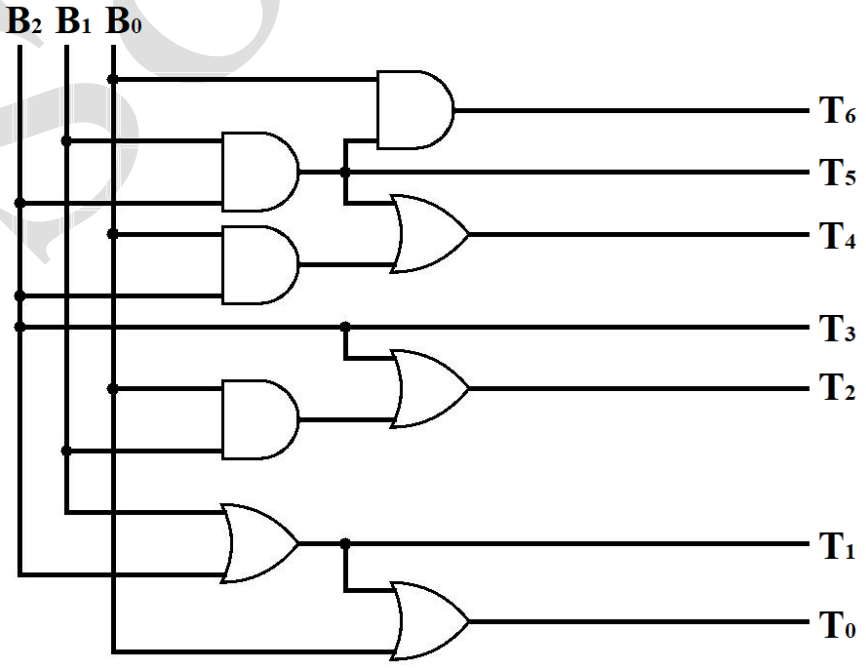
Decimal Digit	Inputs			Outputs						
	B_2	B_1	B_0	T_6	T_5	T_4	T_3	T_2	T_1	T_0
0	0	0	0	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0	0	0	1
2	0	1	0	0	0	0	0	0	1	1
3	0	1	1	0	0	0	0	1	1	1
4	1	0	0	0	0	0	1	1	1	1
5	1	0	1	0	0	1	1	1	1	1
6	1	1	0	0	1	1	1	1	1	1
7	1	1	1	1	1	1	1	1	1	1

Equations

$T_6 = B_2B_1B_0$ $T_5 = B_2B_1$ $T_4 = B_2B_0 + B_2B_1$

$T_3 = B_2$ $T_2 = B_2 + B_1B_0$ $T_1 = B_2 + B_1$ $T_0 = B_2 + B_1 + B_0$

Circuit Diagram



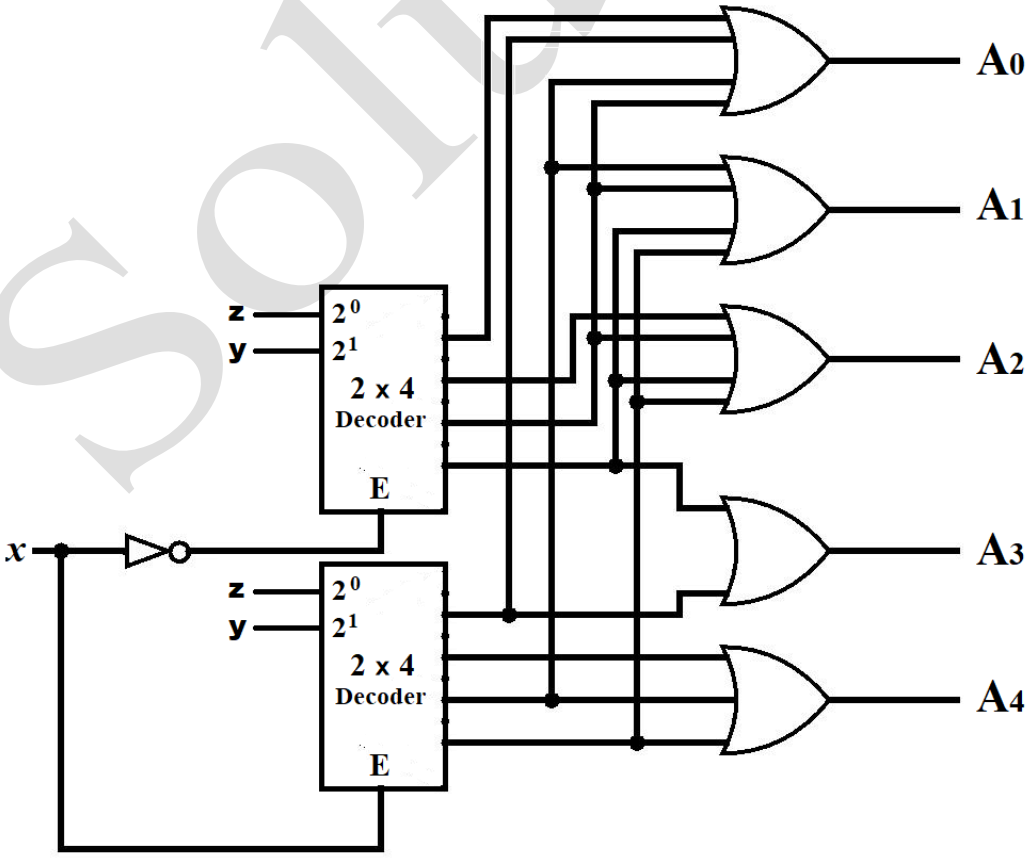
Question Number 3 **(10 Marks)**

Design a combinational circuit that takes 3-bit input and at the output it multiplies it by 3 and adds 1 to have the final output. Design this circuit using only 2 × 4 decoders and basic logic gates if necessary.

The input is a 3-bit number (0 – 7).
The maximum output can be (7 × 3) + 1 = 22, so we need 5 bits at the output.

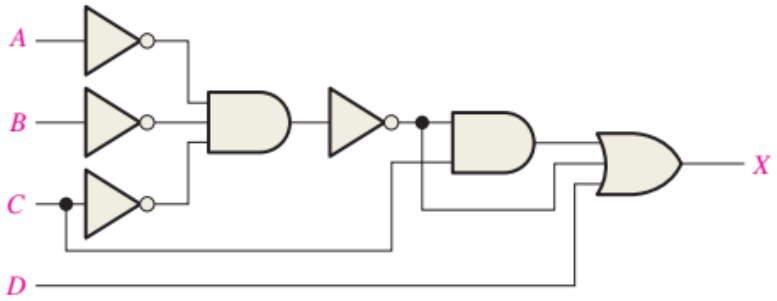
Input Number	Input Bits			Output Number	Output Bits				
	x	*y*	*z*		A_4	A_3	A_2	A_1	A_0
0	0	0	0	(0 × 3) + 1 = 1	0	0	0	0	1
1	0	0	1	(1 × 3) + 1 = 4	0	0	1	0	0
2	0	1	0	(2 × 3) + 1 = 7	0	0	1	1	1
3	0	1	1	(3 × 3) + 1 = 10	0	1	0	1	0
4	1	0	0	(4 × 3) + 1 = 13	0	1	1	0	1
5	1	0	1	(5 × 3) + 1 = 16	1	0	0	0	0
6	1	1	0	(6 × 3) + 1 = 19	1	0	0	1	1
7	1	1	1	(7 × 3) + 1 = 22	1	0	1	1	0

$A_4 = \Sigma(5, 6, 7)$ $A_3 = \Sigma(3, 4)$ $A_2 = \Sigma(1, 2, 4, 7)$
$A_1 = \Sigma(2, 3, 6, 7)$ $A_0 = \Sigma(0, 2, 4, 6)$



Question Number 4 **(10 Marks)**

Reduce the given below logic circuit to minimum number of terms in SOP form. Write the Boolean equation for the reduced form and draw the schematic of reduced circuit.

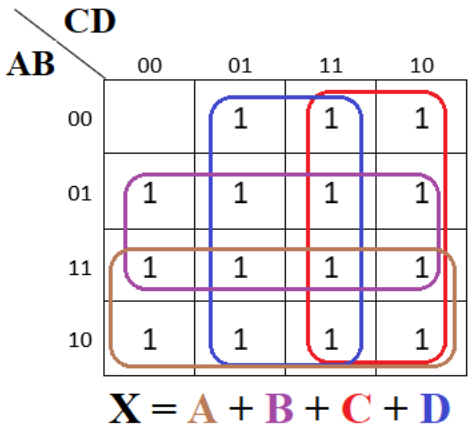


From the given diagram

$$X = (A'B'C')'C + (A'B'C')' + D$$
$$X = (A + B + C)C + A + B + C + D$$
$$X = AC + BC + A + B + C + D$$
$$X = A(C + 1) + B(C + 1) + C + D$$
$$\boldsymbol{X = A + B + C + D}$$

With K-map

A	B	C	D	A'	B'	C'	A'B'C'	(A'B'C')'	(A'B'C')'C	X
0	0	0	0	1	1	1	1	0	0	**0**
0	0	0	1	1	1	1	1	0	0	**1**
0	0	1	0	1	1	0	0	1	1	**1**
0	0	1	1	1	1	0	0	1	1	**1**
0	1	0	0	1	0	1	0	1	0	**1**
0	1	0	1	1	0	1	0	1	0	**1**
0	1	1	0	1	0	0	0	1	1	**1**
0	1	1	1	1	0	0	0	1	1	**1**
1	0	0	0	0	1	1	0	1	0	**1**
1	0	0	1	0	1	1	0	1	0	**1**
1	0	1	0	0	1	0	0	1	1	**1**
1	0	1	1	0	1	0	0	1	1	**1**
1	1	0	0	0	0	1	0	1	0	**1**
1	1	0	1	0	0	1	0	1	0	**1**
1	1	1	0	0	0	0	0	1	1	**1**
1	1	1	1	0	0	0	0	1	1	**1**



X = A + B + C + D

Question Number 5 **(10 Marks)**

Design a Pakistan Voice Idol Game. The game has 04 judges, when the contestant gets the maximum votes from the judges, the winning light of selection must get ON, otherwise, it should remain OFF to show not selected. Design it by using 8×1 Multiplexer and basic logic gates, if necessary, to show the winners and non-winners.

Vote = HIGH No Vote = LOW

Here we have 4 inputs and 1 output.
As we are using 8×1 Multiplexer, so there will be 3 selections lines and 8 data lines.
J1, J2, and J3 will act as selection lines.
We will divide the truth table in 8 equal parts and for each part we will represent S in terms of J4

Truth Table

J1	J2	J3	J4	S	
0	0	0	0	0	S = 0
0	0	0	1	0	
0	0	1	0	0	S = 0
0	0	1	1	0	
0	1	0	0	0	S = 0
0	1	0	1	0	
0	1	1	0	0	S = J4
0	1	1	1	1	
1	0	0	0	0	S = 0
1	0	0	1	0	
1	0	1	0	0	S = J4
1	0	1	1	1	
1	1	0	0	0	S = J4
1	1	0	1	1	
1	1	1	0	1	S = 1
1	1	1	1	1	

MUX Implementation