





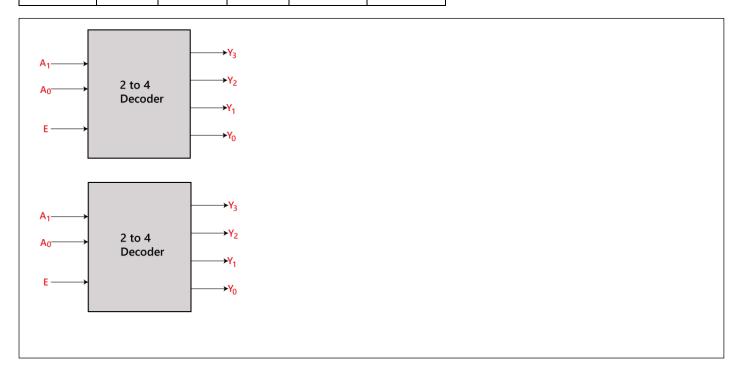
# EE1005 – Digital Logic Design Quiz# 5

Instructor: Muhammad Adeel Tahir	Section: CS-2F	Time: 40 Minutes
Name:		
Roll No:		Total: 25+20+20= 65 marks

**Instructions:** Make sure the handwriting is neat and clean while drawing the circuit, quiz will be marked as 0 if attempted in a writing that is not readable at all.

**Question 1:** Design a combinational circuit that takes 3-bit input and at the output it multiplies it by 3 and adds 1 to have the final output. Design this circuit using only 2:4 decoders and basic logic gates if necessary.

[10 marks]



- a) Implementing the truth table
- b) All the required steps to implement the circuit diagram (if any).
- c) A neat and clean circuit implementation using MUX.

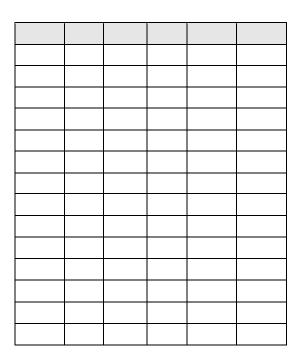
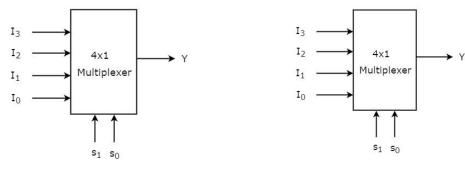


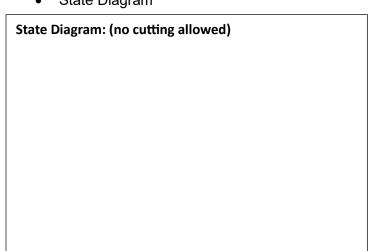
Diagram: (cutting is not allowed- will lead to 0) Show proper connections.

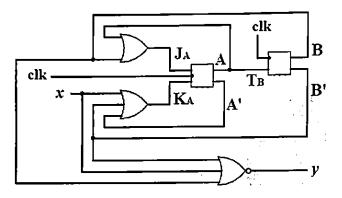


**Question 3:** Given below is the circuit diagram of a synchronous (same clock is applied to both flip flops) sequential circuit with two flip flops (JK and T), one input r, and one output y. Analyze the given circuit to find the:

[2+5+3=10 Marks]

- State Equation(s)
- State Table
- State Diagram





## State Equation(s):

Question 4:

a) Reduce the given state table to minimum possible number of states.

- b) Determine the number of flip flops required to designed a sequential circuit described by the above mentioned state table?
- c) Determine the number of flip flops required to design a sequential circuit described by the reduced state table?
- d) Draw the state diagram corresponding to the reduced state table.

[6+1+1+2= 10 marks]

State Table (binary checking- no cutting allowed)					
Present State	Next	State	Output		
	X=0	X=1	X=0	X=1	
A	Α	Е	1	0	
В	С	F	0	1	
С	В	Н	1	0	
D	В	F	1	0	
E	D	F	0	1	
F	Н	G	1	1	
G	D	Н	0	1	
Н	Н	G	1	1	

State Reductions (step by step)		
	c)	

d) State Diagram:

Question 5: Design a sequential circuit that processes a sequence of binary digits (bits). The circuit should
output a signal Y. This signal Y will be 1 if the total number of 1's in the input sequence so far is even, and it
will be 0 if the total number of 1's is odd. Use D-Flip Flops to build this circuit. You can complete your
design by: [2+5+5+3 = 15 marks]

**Equations:** 

- Constructing state diagram
- State Table
- Required Equations
- Circuit Diagrams

**State Diagram: (Cutting not allowed)** 

State Table:				

**Circuit Diagram:** 

## Question 6: Select the correct option(s) and fill the box with LETTERS:

#### [5 marks]

#### 1) What is the function of a 4-to-1 multiplexer?

- A) Combines four inputs into one output.
- B) Selects one of four inputs to output.
- C) Divides one input into four outputs.
- D) Encodes four inputs into fewer lines.

#### 2) What is true about a 2-to-4 line decoder?

- A) Activates multiple outputs at a time.
- B) Has 4 inputs and 2 outputs.
- C) Has 2 inputs and 4 outputs, one active at a time.
- D) All outputs are always active.

#### 3) What does a D latch do?

- A) Divides the clock frequency.
- B) Stores a bit when enabled.
- C) Converts serial to parallel data.
- D) Toggles between states.

## 4) What feature do sequential circuits have?

- A) Only arithmetic operations.
- B) Memory elements.
- C) No clock signals.
- D) Faster than combinational circuits.

## How can decoders and multiplexers be used together?

- A) Decoder enables multiplexer signals.
- B) Multiplexer selects decoders.
- C) Decoder outputs connect to multiplexer inputs.
- D) Multiplexer generates decoder selection lines.

1	
2	
3	
4	
5	

Bonus Question: [2 marks]

A basket contains five apples. You, your friend, and their friend each take one apple. How is it possible that one apple remains in the basket? Think of a logical answer.