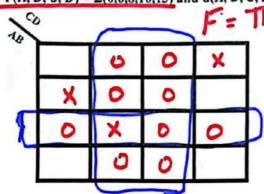
CLO # 01: Apply Binary Logic, Boolean Algebra, and Karnaugh map Methods to calculate and simplify Boolean functions.

Q1: Apply the Karnaugh map on the Boolean function "F", together with the don't care conditions "d" and find the simplified POS equation: $F(A, B, C, D) = \Sigma(0,6,8,10,13)$ and $d(A, B, C, D) = \Sigma(2,4,13)$ [10 marks]



Simplified equation with all possible step (if any):

$$F' = D + AB$$

 $(F) = (D + AB)$
 $F = D' \cdot (A' + B')$

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CLO # 02: Use digital circuit-solving techniques to obtain truth tables, Boolean functions, and timing diagrams for combinational circuits, and State equations, state tables, and state diagrams for sequential circuits.

Q2: Design a combinational circuit with four inputs (A, B, C, D) and two outputs (X, Y). The output x will be high if the input is divisible by 4, while output y will indicate high if any two neighboring input variables are set to 1. [15 marks]

a. Draw the truth table

(5 Marks)

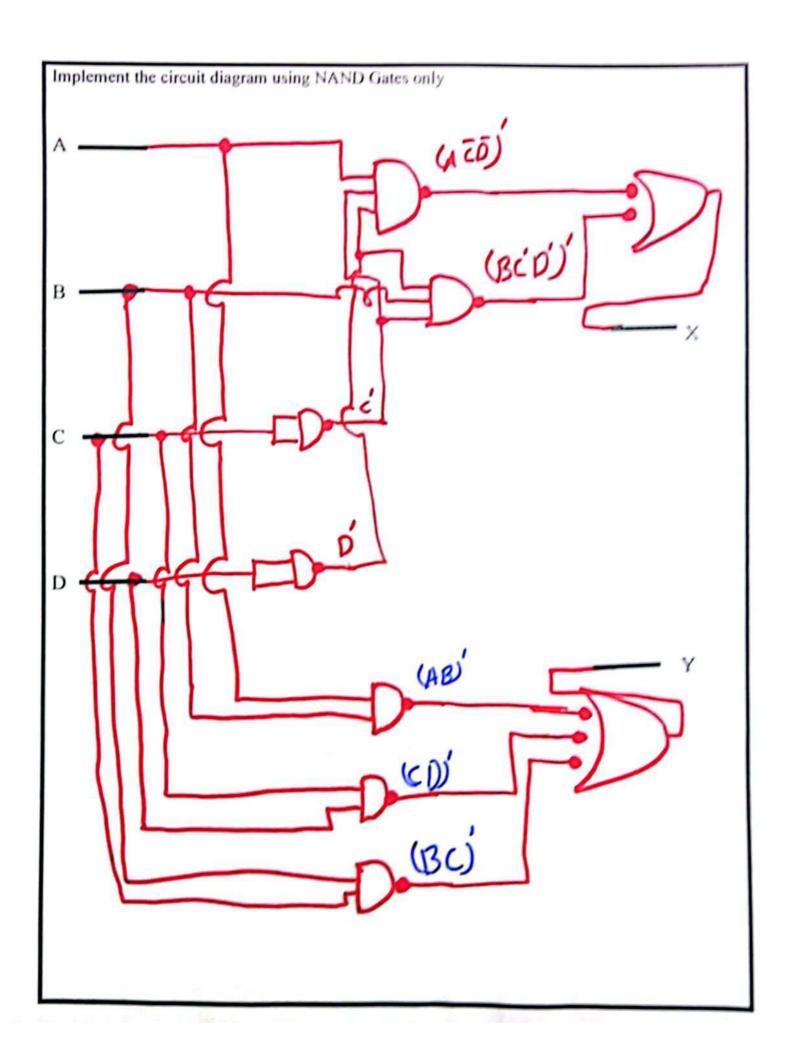
b. Derive a simplified Boolean expression using K-Map

(5 Marks)

c. Implement the circuit diagram using NAND gates only

(5 Marks)

		р.т		oun un	gram a.	- (3 // mars)
Α	В	С	D	х	Υ	for X
0	0	٥	0	0	0	
0	0	0	1	0	0	
0	٥	-	0	0	D	
0	0	-	1	0	1	
0	1	0	0	1	0	Equation with all possible step:
0	ı	0	1	0	0	X= ACD+BCD
0	_	ı	0	0	1	X= CO (A+B)
0	-	ı	. 1	0	1	for Y
1	0	0	0	1	0	
1	0	0	ı	0	0	
1	0	1	0	0	0	
1	0	ı	1	O	1	
1	1	0	0	1	1	
1	1	0	1	0	1	Equation with all possible step: Y= AB+CD+BC
1	1	ı	0	0	1	15. CD7 BC
)	1	1	1	0	1	

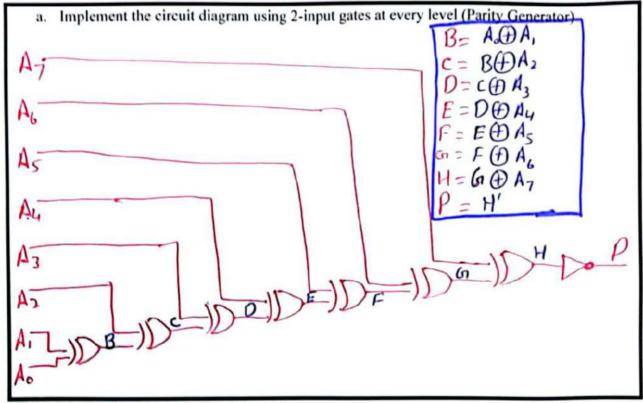


Q3: Design the 8-bit odd-parity generator and checker. Also give five examples (given in following table with the help of ASCII Codes) of the input patterns to show that the generator and checker are working as expected For a 8-bit system using odd parity scheme:

[20 marks]

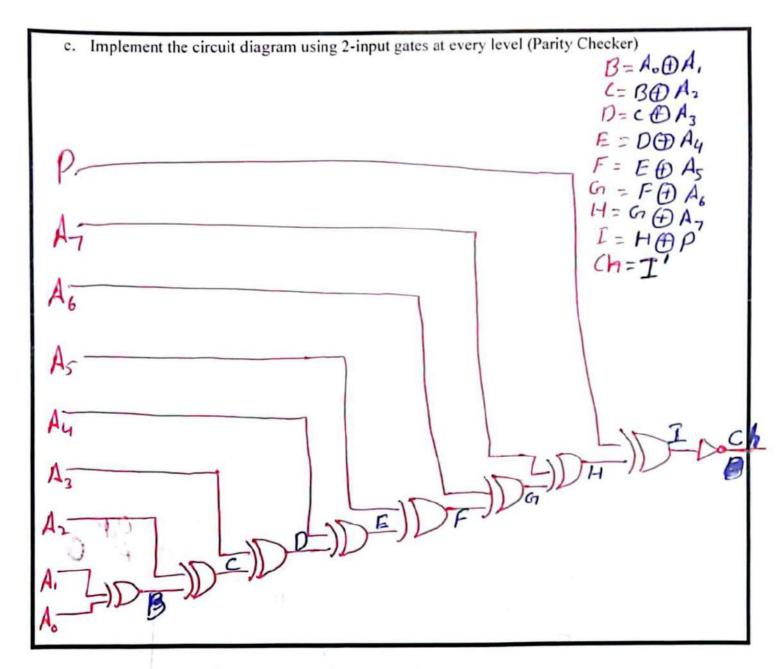
a.	Design circuit of 8-bit parity generator	[5 marks]
b.	Complete the table	[5 marks]
c.	Design circuit of 8-bit parity checker	[5 marks]
d.	Complete the table	[5 marks]

Note: A neat and clean Circuit diagram is important. Cutting and overwriting can directly affect your marks (more than 2 cutting directly mark as zero). Label every point and attempt all the best practices. We know that ASCII of "A=65" and "a=97")



b. Complete the table:

	A7	A ₆	A ₅	A4	Аз	A ₂	A_1	A_0	Parity
A	0	1	0	0	0	0	0	1	1
d	0	1	1	0	0	1	0	0	0
e	0	1	1	0	0	1	0	1	1
e	0	1	1	0	0	1	0	1	1
l	0	1	1	0	1	1	0	0	1

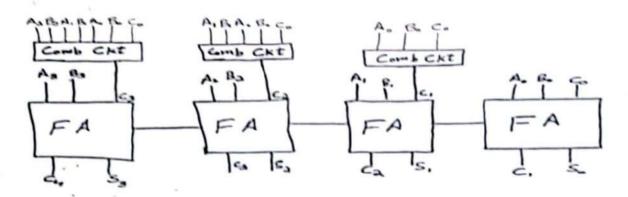


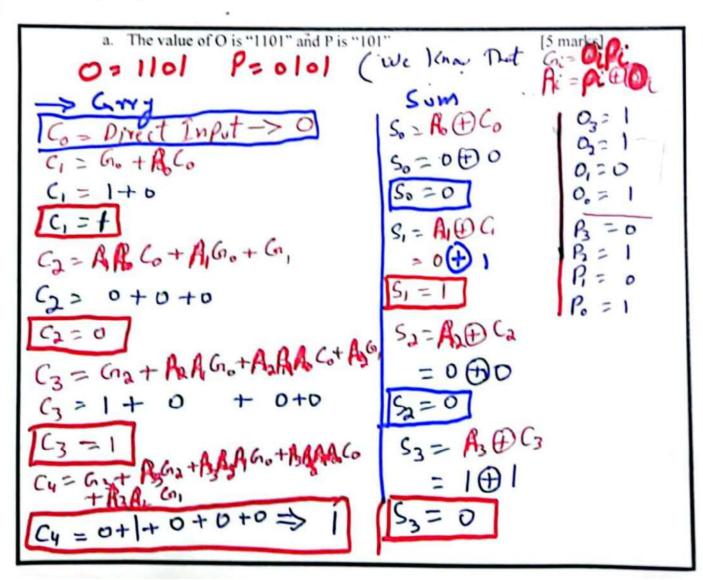
d. Complete the rest of the table according to part 3(b):

	A7	A ₆	A5	A4	A3	A ₂	\mathbf{A}_{1}	A_0	Parity	Checker
A	0	1	0	0	1	0	0	1	1 -183	-1
d	b	1	1	1	1	1	0	0	0	0
e	0	1	1	0	0	0	, 0	1	1	1
e	0	1	١	0	0	1	0	1	1	0
l	0	1	1	0)	1	Q	0	1	0

Q4: Following figure shows a Carry Look Ahead Adder which can be designed from four (4) full adder. Addition of 4-bit number using parallel adder is difficult due to delay in the circuit. This can be overcome with the help of carry look ahead adder circuit. In this question you are required to add the below 4-bit number by using the Carry Look ahead adder shown below.

[10] marks]





Cy= 1+0+0+0+0

Som
$$S_{0} = A \oplus C_{0}$$

$$S_{0} = A \oplus C_{1}$$

$$S_{1} = A \oplus C_{1}$$

$$S_{2} = A \oplus C_{2}$$

$$S_{3} = A \oplus C_{3}$$

$$S_{4} = A \oplus C_{4}$$

$$S_{5} = A \oplus C_{5}$$

$$S_{5} = A \oplus C_{5}$$

$$S_{7} = A \oplus C_{7}$$

[5 marks]