



EE1005 – Digital Logic Design Quiz# 5

Instructor: Muhammad Adeel Tahir **Section:** CS-2F

Time: 60 Minutes

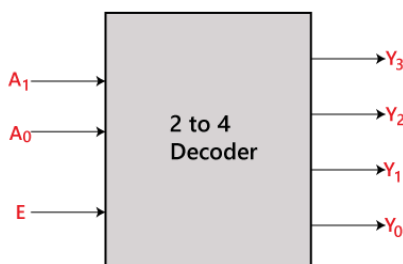
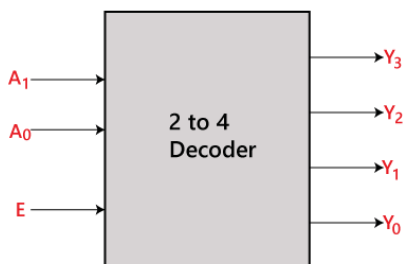
Name: _____

Roll No: _____

Total: 25+20+20= 65 marks

Instructions: Make sure the handwriting is neat and clean while drawing the circuit, quiz will be marked as 0 if attempted in a writing that is not readable at all.

Question 1: Design a combinational circuit that takes 3-bit input and at the output it multiplies it by 3 and adds 1 to have the final output. Design this circuit using only 2:4 decoders and basic logic gates if necessary. **[10 marks]**

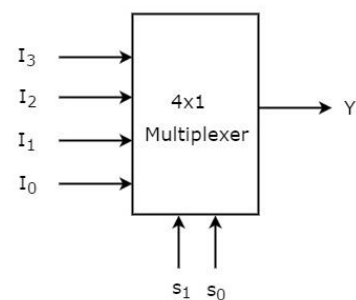
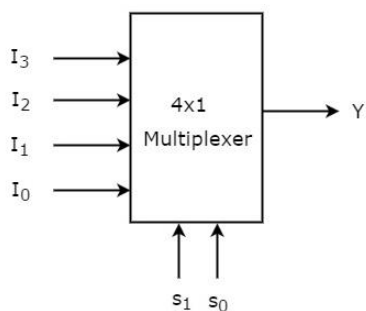


Question 2: Implement a Full Adder using two 4:1 MUX. Complete it by:

[3+5+7 = 15 marks]

- Implementing the truth table
- All the required steps to implement the circuit diagram (if any) .
- A neat and clean circuit implementation using MUX.

Diagram: (cutting is not allowed- will lead to 0) Show proper connections.

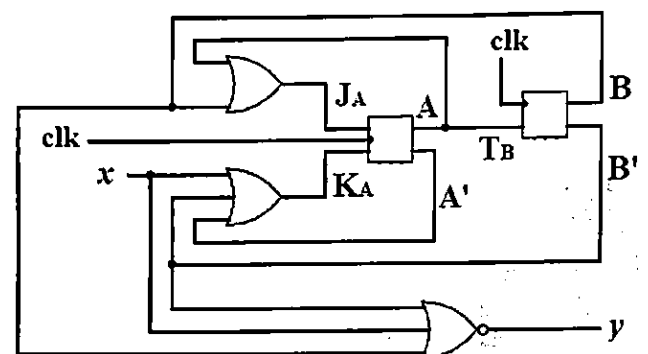


Question 3: Given below is the circuit diagram of a synchronous (same clock is applied to both flip flops) sequential circuit with two flip flops (JK and T), one input x , and one output y . Analyze the given circuit to find the:

[2+5+3=10 Marks]

- State Equation(s)
- State Table
- State Diagram

State Diagram: (no cutting allowed)



State Equation(s):

Question 4:

[6+1+1+2= 10 marks]

- Reduce the given state table to minimum possible number of states.
- Determine the number of flip flops required to designed a sequential circuit described by the above mentioned state table?
- Determine the number of flip flops required to design a sequential circuit described by the reduced state table?
- Draw the state diagram corresponding to the reduced state table.

State Table (binary checking- no cutting allowed)				
Present State	Next State		Output	
	X=0	X=1	X=0	X=1
A	A	E	1	0
B	C	F	0	1
C	B	H	1	0
D	B	F	1	0
E	D	F	0	1
F	H	G	1	1
G	D	H	0	1
H	H	G	1	1

a)

State Reductions (step by step)

b) _____ c) _____

d) State Diagram:

Question 5: Design a sequential circuit that processes a continuous input of binary digits (1s or 0s). Each bit is processed in a cycle, and the circuit produces an output signal, Y.

- **Output Y should be set to 1** whenever the total number of '1's in the sequence received so far is even.
- **Output Y should be 0** if the total number of '1's received so far is odd.

Start the system assuming Y = 1 (even count of 1s exist already before the input string was given to the circuit)

Complete your design by constructing:

[2+5+5+3 = 15 marks]

State Diagram:

State Table

Required Equations

Circuit Diagrams:

State Diagram: (Cutting not allowed)

State Table:

Equations:

Circuit Diagram:

Question 6: Select the correct option(s) and fill the box with LETTERS:

[5 marks]

1) What is the function of a 4-to-1 multiplexer?

- A) Combines four inputs into one output.
- B) Selects one of four inputs to output.
- C) Divides one input into four outputs.
- D) Encodes four inputs into fewer lines.

2) What is true about a 2-to-4 line decoder?

- A) Activates multiple outputs at a time.
- B) Has 4 inputs and 2 outputs.
- C) Has 2 inputs and 4 outputs, one active at a time.
- D) All outputs are always active.

3) What does a D latch do?

- A) Divides the clock frequency.
- B) Stores a bit when enabled.
- C) Converts serial to parallel data.
- D) Toggles between states.

4) What feature do sequential circuits have?

- A) Only arithmetic operations.
- B) Memory elements.
- C) No clock signals.
- D) Faster than combinational circuits.

How can decoders and multiplexers be used together?

- A) Decoder enables multiplexer signals.
- B) Multiplexer selects decoders.
- C) Decoder outputs connect to multiplexer inputs.
- D) Multiplexer generates decoder selection lines.

1	
2	
3	
4	
5	

ROUGH WORK:

Bonus Question:

[2 marks]

A basket contains five apples. You, your friend, and their friend each take one apple. How is it possible that one apple remains in the basket? Think of a logical answer.
