Reduced Instruction Set Computers

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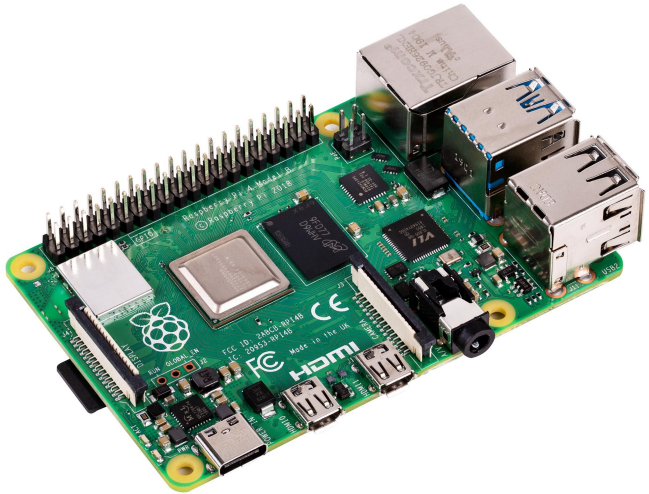
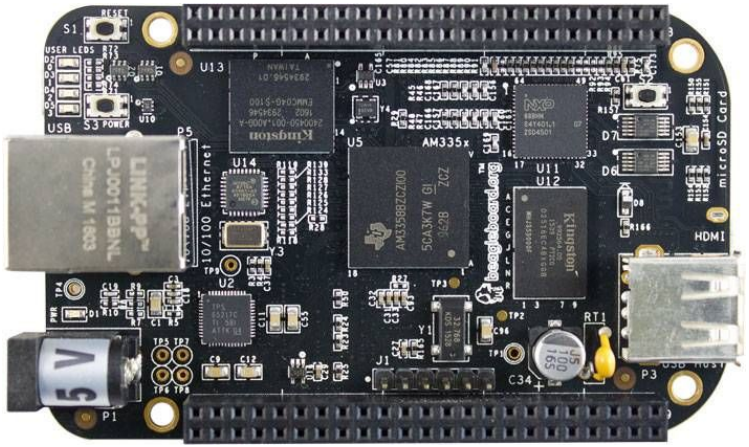
What are Reduced Instruction Set Computers

- Microcontroller architecture
- Small and highly-optimized
- One Cycle Execution Time
- Pipelining
- Large Number of Registers

Examples of RISCs



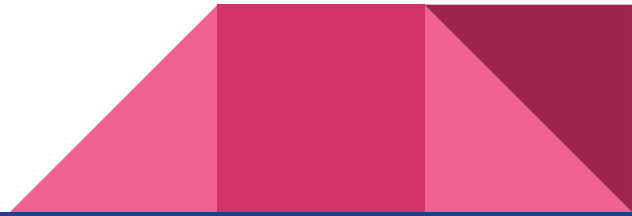


Brief history of RISC

- IBM, Stanford, and UC-Berkeley
- 1960s - Designs
- Early 1970s - IBM 801
- Mid 1980s - IBM ROMP

RISC vs a standard computer

RISC	CISC
Code is large	Code is small
Takes a single clock cycle to execute	Takes more than one clock cycle to execute
Fixed sized instructions	Variable sized instructions
More general-purpose registers	Less number of general-purpose registers



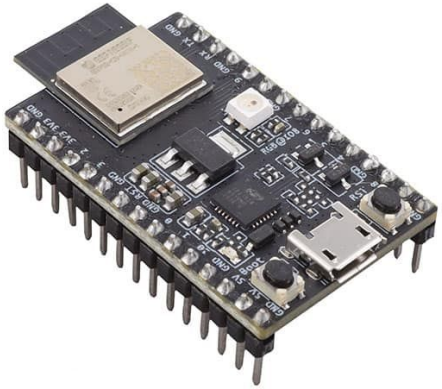
Sample Code of RISC (Hello World)

Assembler MASM DOS.asm

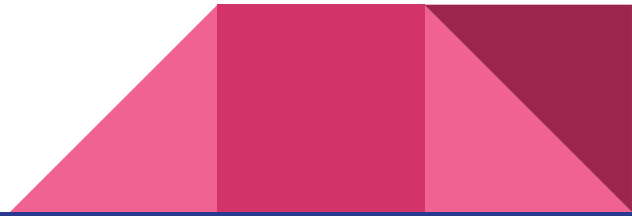
```
1  .model small
2  .stack
3  .data
4      message  db "Hello World" "$"
5  .code
6      main   proc
7          mov  ax,seg message
8          mov  ds,ax
9          mov  ah,09
10         lea  dx,message
11         int  21h
12
13         mov  ax,4c00h
14         int  21h
15     main   endp
16 end main
17
```

Future of RISC

- Apple moving from ARM
- RISC vs RISC-V



Any Questions?



Sources

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