Tyler Anderson   BSD_event_protocol
rev1   3/11/2013

Event Packets

Contents	Byte in Packet	Bit in Byte	Associated CS	Description
0x8F	0	*	N/A	SYNC
0xC7	1	*	N/A	SYNC
0xCD	2	*	N/A	SYNC
0xDC	3	*	N/A	SYNC
EVTNO[31:24]	4	*	N/A	Instrument event number
EVTNO[23:16]	5	*	N/A	Instrument event number
EVTNO[15:8]	6	*	N/A	Instrument event number
EVTNO[7:0]	7	*	N/A	Instrument event number
EVTCNT[7:0]	8	*	N/A	Event counter, number of events collected since system reset
EVENT STATUS	9	*	N/A	Flags indicating trigger and event conditions
TRIG_MODE	9	7-5	N/A	Trigger Mode for this event
CONF_MODE	9	4-3	N/A	Confirmation Mode for this event
TRIG2	9	2	N/A	Flag is set if T2 was involved in T0 formation
TRIG1	9	1	N/A	Flag is set if T1 was involved in T0 formation
EXTIN	9	0	N/A	Flag is set if EXTIN (IMT for flight) was involved in T0 formation
A2D11L[15:8]	10	*	A2D11LCS\	PMT 1 Quartet 1 Low Gain ADC High Byte
A2D11L[7:0]	11	*	A2D11LCS\	PMT 1 Quartet 1 Low Gain ADC Low Byte
A2D11H[15:8]	12	*	A2D11HCS\	PMT 1 Quartet 1 High Gain ADC High Byte
A2D11H[7:0]	13	*	A2D11HCS\	PMT 1 Quartet 1 High Gain ADC Low Byte
A2D21L[15:8]	14	*	A2D21LCS\	PMT 2 Quartet 1 Low Gain ADC High Byte
A2D21L[7:0]	15	*	A2D21LCS\	PMT 2 Quartet 1 Low Gain ADC Low Byte
A2D21H[15:8]	16	*	A2D21HCS\	PMT 2 Quartet 1 High Gain ADC High Byte
A2D21H[7:0]	17	*	A2D21HCS\	PMT 2 Quartet 1 High Gain ADC Low Byte
A2D31L[15:8]	18	*	A2D31LCS\	PMT 3 Quartet 1 Low Gain ADC High Byte
A2D31L[7:0]	19	*	A2D31LCS\	PMT 3 Quartet 1 Low Gain ADC Low Byte
A2D31H[15:8]	20	*	A2D31HCS\	PMT 3 Quartet 1 High Gain ADC High Byte
A2D31H[7:0]	21	*	A2D31HCS\	PMT 3 Quartet 1 High Gain ADC Low Byte
A2D41L[15:8]	22	*	A2D41LCS\	PMT 4 Quartet 1 Low Gain ADC High Byte
A2D41L[7:0]	23	*	A2D41LCS\	PMT 4 Quartet 1 Low Gain ADC Low Byte
A2D41H[15:8]	24	*	A2D41HCS\	PMT 4 Quartet 1 High Gain ADC High Byte
A2D41H[7:0]	25	*	A2D41HCS\	PMT 4 Quartet 1 High Gain ADC Low Byte
A2D12L[15:8]	26	*	A2D12LCS\	PMT 1 Quartet 2 Low Gain ADC High Byte
A2D12L[7:0]	27	*	A2D12LCS\	PMT 1 Quartet 2 Low Gain ADC Low Byte
A2D12H[15:8]	28	*	A2D12HCS\	PMT 1 Quartet 2 High Gain ADC High Byte
A2D12H[7:0]	29	*	A2D12HCS\	PMT 1 Quartet 2 High Gain ADC Low Byte
A2D22L[15:8]	30	*	A2D22LCS\	PMT 2 Quartet 2 Low Gain ADC High Byte
A2D22L[7:0]	31	*	A2D22LCS\	PMT 2 Quartet 2 Low Gain ADC Low Byte
A2D22H[15:8]	32	*	A2D22HCS\	PMT 2 Quartet 2 High Gain ADC High Byte
A2D22H[7:0]	33	*	A2D22HCS\	PMT 2 Quartet 2 High Gain ADC Low Byte
A2D32L[15:8]	34	*	A2D32LCS\	PMT 3 Quartet 2 Low Gain ADC High Byte
A2D32L[7:0]	35	*	A2D32LCS\	PMT 3 Quartet 2 Low Gain ADC Low Byte
A2D32H[15:8]	36	*	A2D32HCS\	PMT 3 Quartet 2 High Gain ADC High Byte
A2D32H[7:0]	37	*	A2D32HCS\	PMT 3 Quartet 2 High Gain ADC Low Byte
A2D42L[15:8]	38	*	A2D42LCS\	PMT 4 Quartet 2 Low Gain ADC High Byte
A2D42L[7:0]	39	*	A2D42LCS\	PMT 4 Quartet 2 Low Gain ADC Low Byte
A2D42H[15:8]	40	*	A2D42HCS\	PMT 4 Quartet 2 High Gain ADC High Byte
A2D42H[7:0]	41	*	A2D42HCS\	PMT 4 Quartet 2 High Gain ADC Low Byte
A2D13L[15:8]	42	*	A2D13LCS\	PMT 1 Quartet 3 Low Gain ADC High Byte
A2D13L[7:0]	43	*	A2D13LCS\	PMT 1 Quartet 3 Low Gain ADC Low Byte
A2D13H[15:8]	44	*	A2D13HCS\	PMT 1 Quartet 3 High Gain ADC High Byte
A2D13H[7:0]	45	*	A2D13HCS\	PMT 1 Quartet 3 High Gain ADC Low Byte
A2D23L[15:8]	46	*	A2D23LCS\	PMT 2 Quartet 3 Low Gain ADC High Byte
A2D23L[7:0]	47	*	A2D23LCS\	PMT 2 Quartet 3 Low Gain ADC Low Byte
A2D23H[15:8]	48	*	A2D23HCS\	PMT 2 Quartet 3 High Gain ADC High Byte
A2D23H[7:0]	49	*	A2D23HCS\	PMT 2 Quartet 3 High Gain ADC Low Byte
A2D33L[15:8]	50	*	A2D33LCS\	PMT 3 Quartet 3 Low Gain ADC High Byte
A2D33L[7:0]	51	*	A2D33LCS\	PMT 3 Quartet 3 Low Gain ADC Low Byte
A2D33H[15:8]	52	*	A2D33HCS\	PMT 3 Quartet 3 High Gain ADC High Byte
A2D33H[7:0]	53	*	A2D33HCS\	PMT 3 Quartet 3 High Gain ADC Low Byte
A2D43L[15:8]	54	*	A2D43LCS\	PMT 4 Quartet 3 Low Gain ADC High Byte
A2D43L[7:0]	55	*	A2D43LCS\	PMT 4 Quartet 3 Low Gain ADC Low Byte
A2D43H[15:8]	56	*	A2D43HCS\	PMT 4 Quartet 3 High Gain ADC High Byte
A2D43H[7:0]	57	*	A2D43HCS\	PMT 4 Quartet 3 High Gain ADC Low Byte
A2D14L[15:8]	58	*	A2D14LCS\	PMT 1 Quartet 4 Low Gain ADC High Byte
A2D14L[7:0]	59	*	A2D14LCS\	PMT 1 Quartet 4 Low Gain ADC Low Byte
A2D14H[15:8]	60	*	A2D14HCS\	PMT 1 Quartet 4 High Gain ADC High Byte
A2D14H[7:0]	61	*	A2D14HCS\	PMT 1 Quartet 4 High Gain ADC Low Byte
A2D24L[15:8]	62	*	A2D24LCS\	PMT 2 Quartet 4 Low Gain ADC High Byte
A2D24L[7:0]	63	*	A2D24LCS\	PMT 2 Quartet 4 Low Gain ADC Low Byte
A2D24H[15:8]	64	*	A2D24HCS\	PMT 2 Quartet 4 High Gain ADC High Byte
A2D24H[7:0]	65	*	A2D24HCS\	PMT 2 Quartet 4 High Gain ADC Low Byte
A2D34L[15:8]	66	*	A2D34LCS\	PMT 3 Quartet 4 Low Gain ADC High Byte
A2D34L[7:0]	67	*	A2D34LCS\	PMT 3 Quartet 4 Low Gain ADC Low Byte
A2D34H[15:8]	68	*	A2D34HCS\	PMT 3 Quartet 4 High Gain ADC High Byte
A2D34H[7:0]	69	*	A2D34HCS\	PMT 3 Quartet 4 High Gain ADC Low Byte
A2D44L[15:8]	70	*	A2D44LCS\	PMT 4 Quartet 4 Low Gain ADC High Byte
A2D44L[7:0]	71	*	A2D44LCS\	PMT 4 Quartet 4 Low Gain ADC Low Byte
A2D44H[15:8]	72	*	A2D44HCS\	PMT 4 Quartet 4 High Gain ADC High Byte
A2D44H[7:0]	73	*	A2D44HCS\	PMT 4 Quartet 4 High Gain ADC Low Byte
A2DT1L[15:8]	74	*	A2DT1LCS\	Trigger PMT 1 Low Gain ADC High Byte
A2DT1L[7:0]	75	*	A2DT1LCS\	Trigger PMT 1 Low Gain ADC Low Byte
A2DT1H[15:8]	76	*	A2DT1HCS\	Trigger PMT 1 High Gain ADC High Byte
A2DT1H[7:0]	77	*	A2DT1HCS\	Trigger PMT 1 High Gain ADC Low Byte
A2DT2L[15:8]	78	*	A2DT2LCS\	Trigger PMT 2 Low Gain ADC High Byte
A2DT2L[7:0]	79	*	A2DT2LCS\	Trigger PMT 2 Low Gain ADC Low Byte
A2DT2H[15:8]	80	*	A2DT2HCS\	Trigger PMT 2 High Gain ADC High Byte
A2DT2H[7:0]	81	*	A2DT2HCS\	Trigger PMT 2 High Gain ADC Low Byte

Command Packets

Contents	Byte in Packet	Bit in Byte	Associated CS	Description
0x8F	0	*	N/A	SYNC
0xC7	1	*	N/A	SYNC
0xAB	2	*	N/A	SYNC
0xBA	3	*	N/A	SYNC
Command	4-7	*	N/A	See command list document

Housekeeping Packets

Contents	Byte in Packet	Bit in Byte	Associated CS	Description
0x8F	0	*	N/A	SYNC
0xC7	1	*	N/A	SYNC
0xBC	2	*	N/A	SYNC
0xCB	3	*	N/A	SYNC
HK response	4-7	*	N/A	See command list document