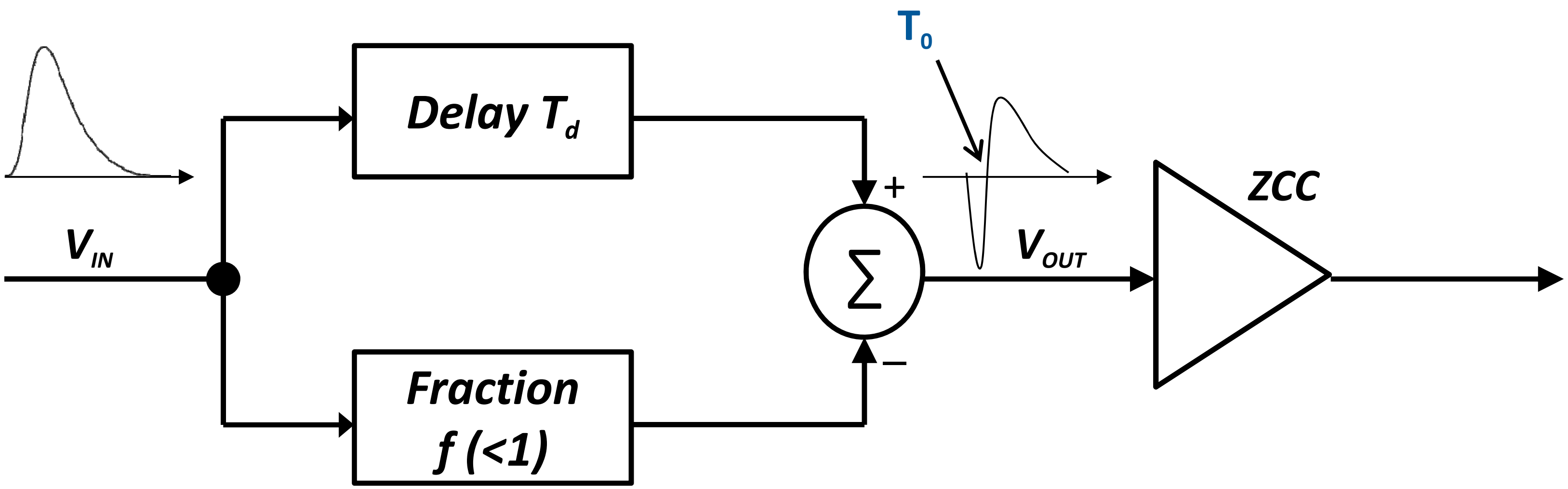
CONSTANT FRACTION DISCRIMINATOR

F. Loddo & C. Tamma – INFN Bari

Principle of Operation



Creation of a variable threshold tracking the signal always at a certain fraction of its amplitude

$$V_{OUT}(t) = V_{IN}(t - T_d) - f * V_{IN}(t)$$

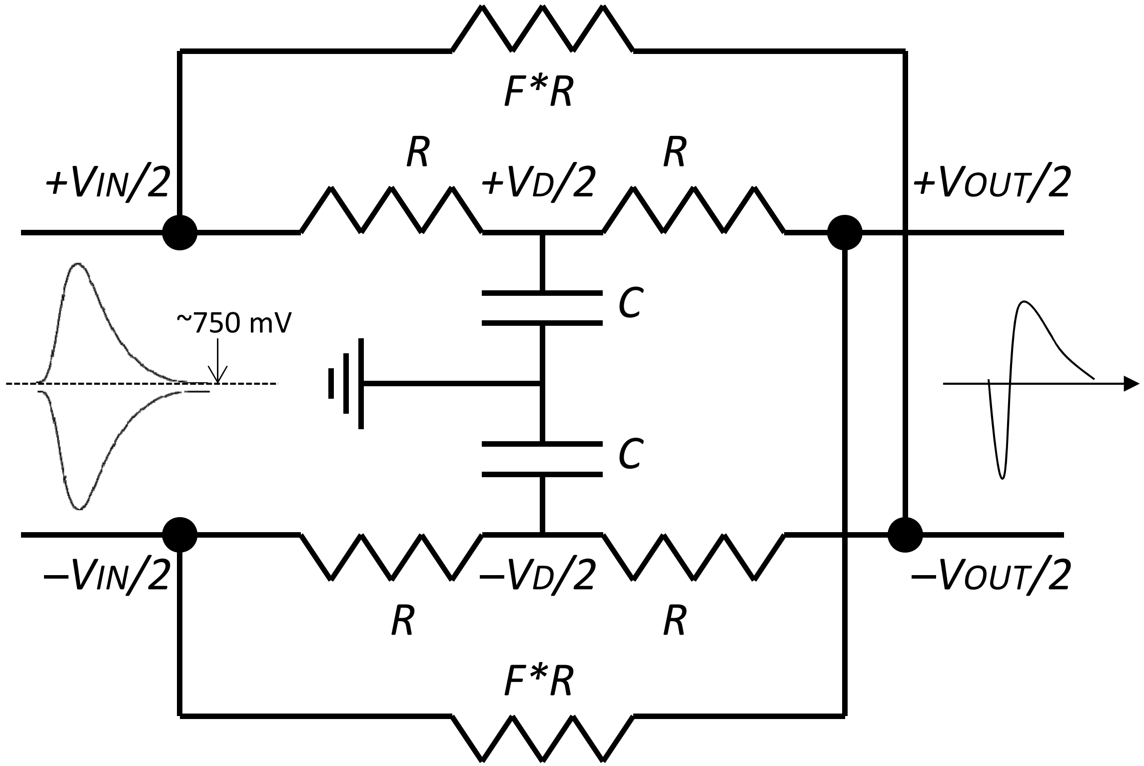
The output bipolar signal has a zero crossing time T_0 depending only on network parameters (T_d, f)

$T_d > (1\text{-}f) * T_p$ ***TRUE CONSTANT FRACTION TIMING TCF***

$T_d < (1\text{-}f) * T_p$ ***AMPLITUDE AND RISE TIME COMPENSATED TIMING ARC***

Proposed Shaping Network

Cross coupling topology

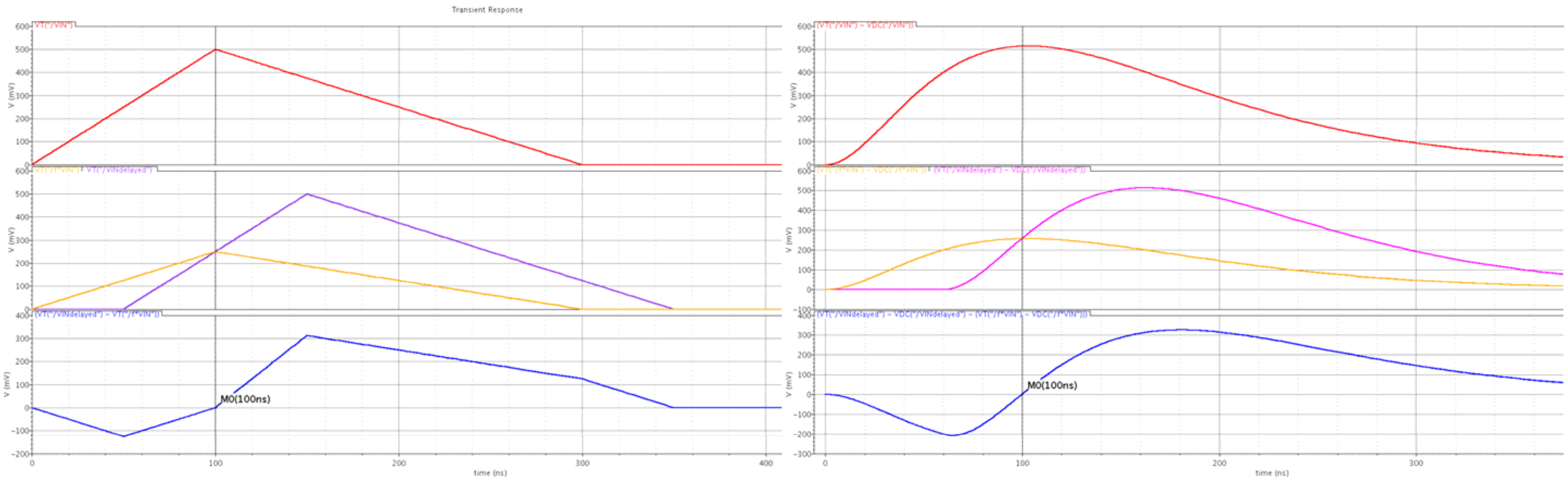


<u>Main Advantage :</u>
The fully differential structure provides very good rejection of common mode noise injected in the substrate by the switching digital logic

<u>S. Garbolino, S. Martoiu and A. Rivetti</u>
Implementantion of Constant-Fraction-Discriminators (CFD) in Sub-micron CMOS Technologies
2011 IEEE Nuclear Science Symposium Conference Record

Shaping Network

To minimize timing jitter, the rms noise must be minimized while the signal slope through the threshold crossing must be maximized



f = 0.5

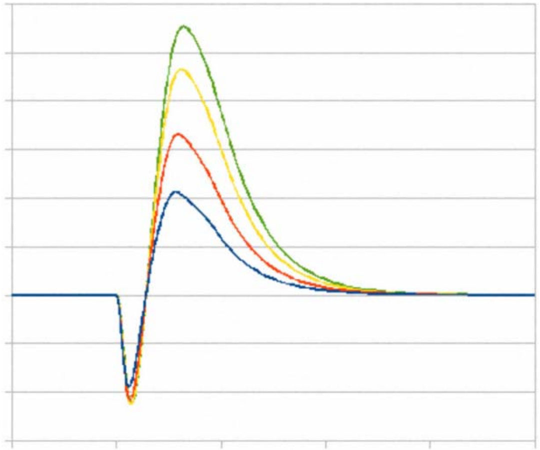
T_d = 50% T_p

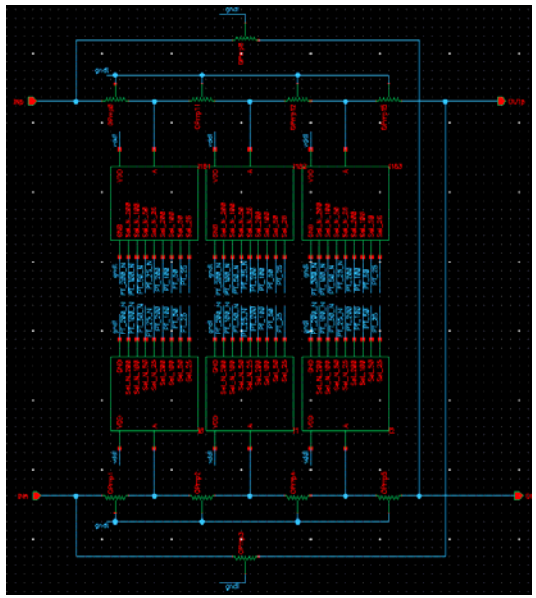
T_0 matches the peak of the input signal T_p and the amplitude tracking threshold is set to the 50% of the amplitude of the input signal

Shaping Network

Cross coupling topology

Moreover, once the fraction is fixed a higher order filter has a higher slope (less jitter)





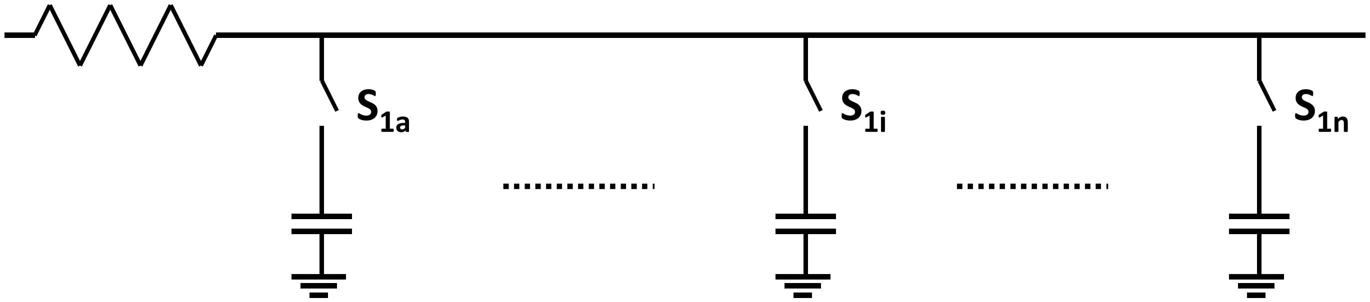
Design Specifications:

- filter order **n = 3** as compromise between timing precision and area occupied
- fraction factor **f = 0.4**
- Time delay **T_d = 0.6* T_p** programmable with T_p through switches
- TCF configuration with Crossing Time **$T_0 = T_p$**
- Use of polysilicon resistors and vertical natural capacitors

- New: Possibility to compensate parameter process variations using additional capacitors (enabled by switches)

Shaping Network

One or more “S_1“ analog switches can be closed to reach the desired T_d.



Optimization of T_d with process variations

- **+3σ case:**

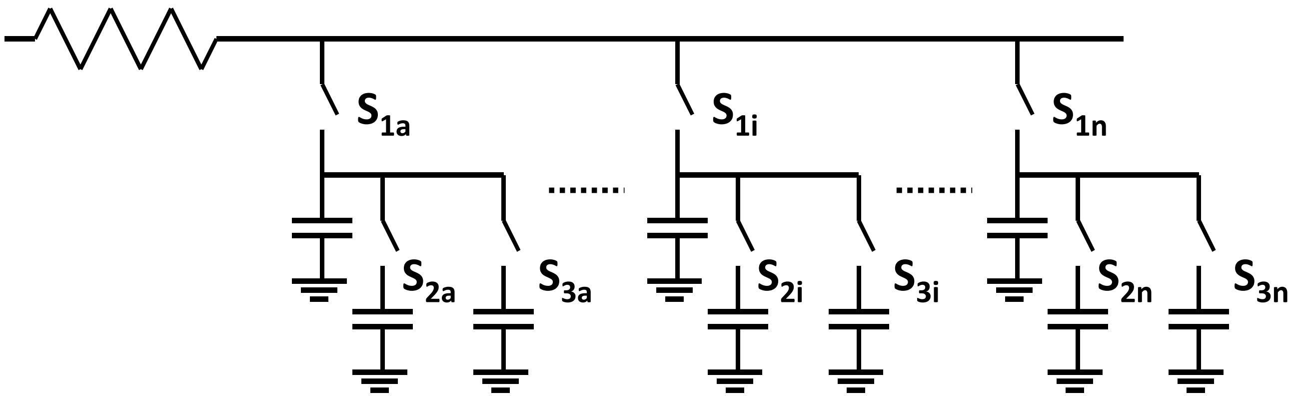
S_{1i} closed.
S_{2i} and S_{3i} opened.

- **typical case:**

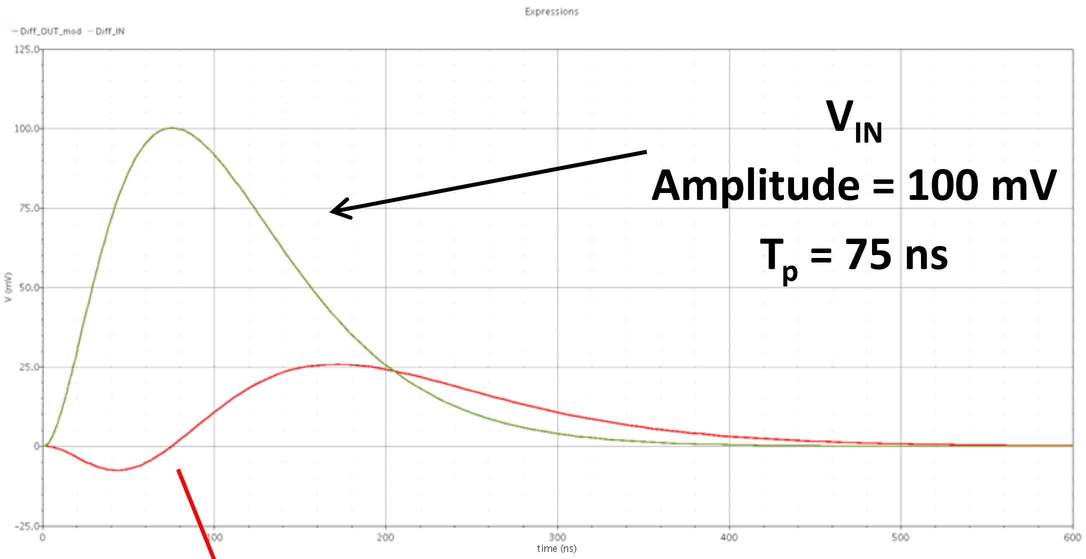
S_{1i} and S_{2i} closed.
S_{3i} opened.

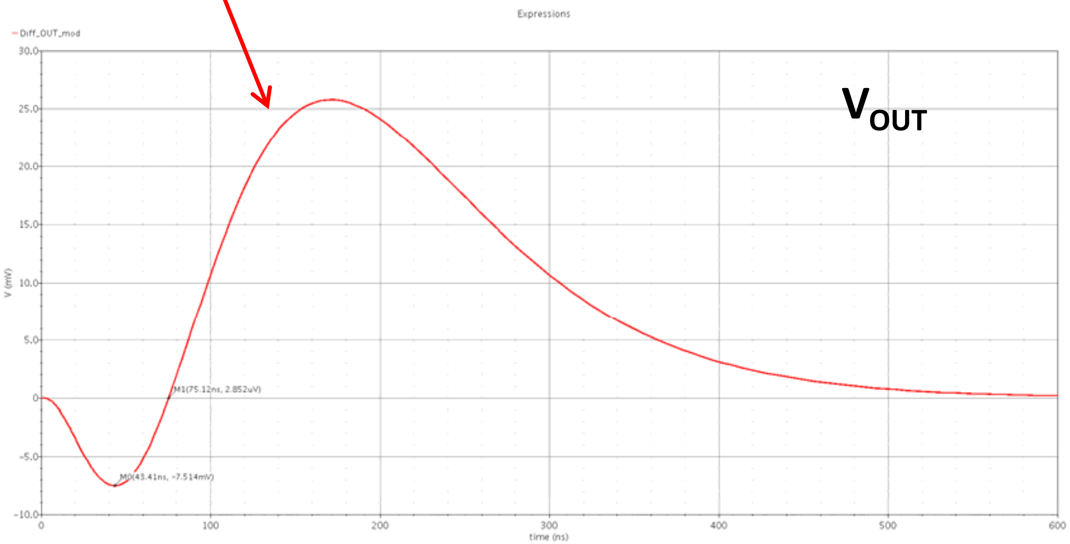
- **-3σ case:**

S_{1i}, S_{2i} and S_{3i} closed.



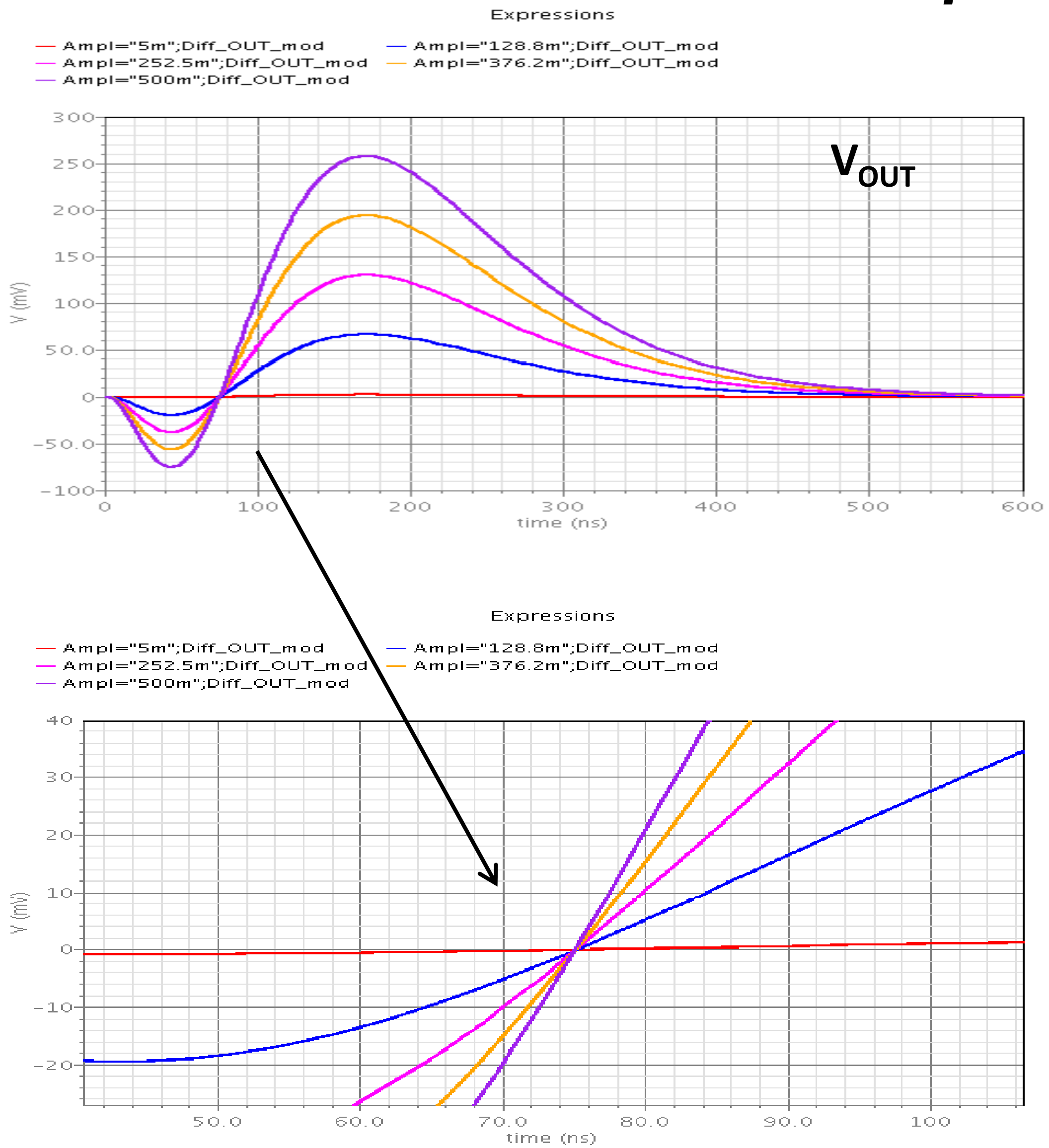
Example: T_p = 75 ns





Crossing time T_0	75.12 ns
Delay time T_d	43.41 ns
Fraction factor f	0.422

Example: T_p = 75 ns



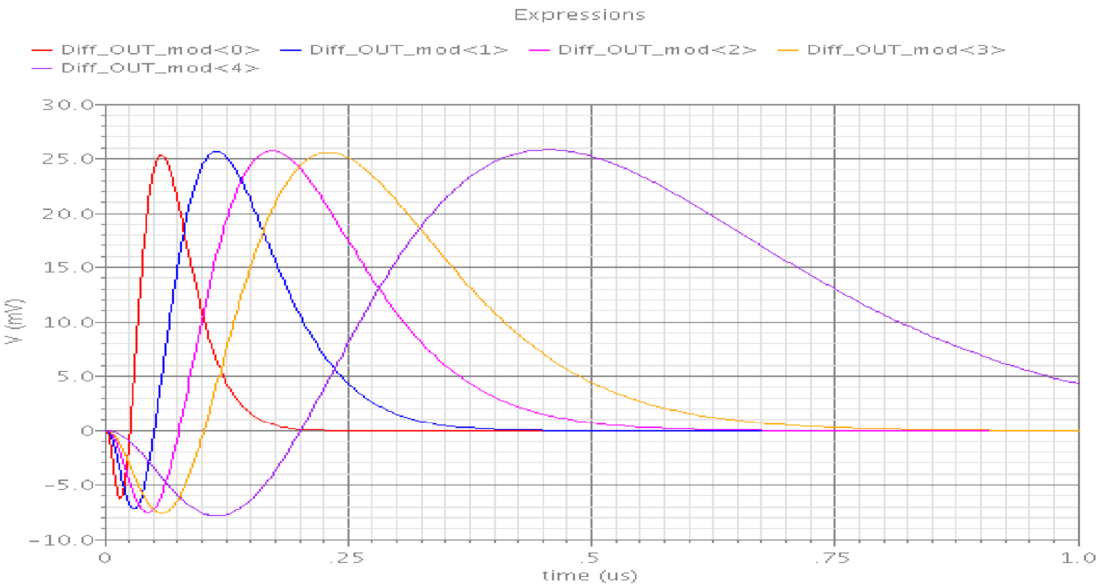
Amplitude Compensation

V_{IN}

Amplitude = 10 ÷ 1000 mV

T_p = 75 ns

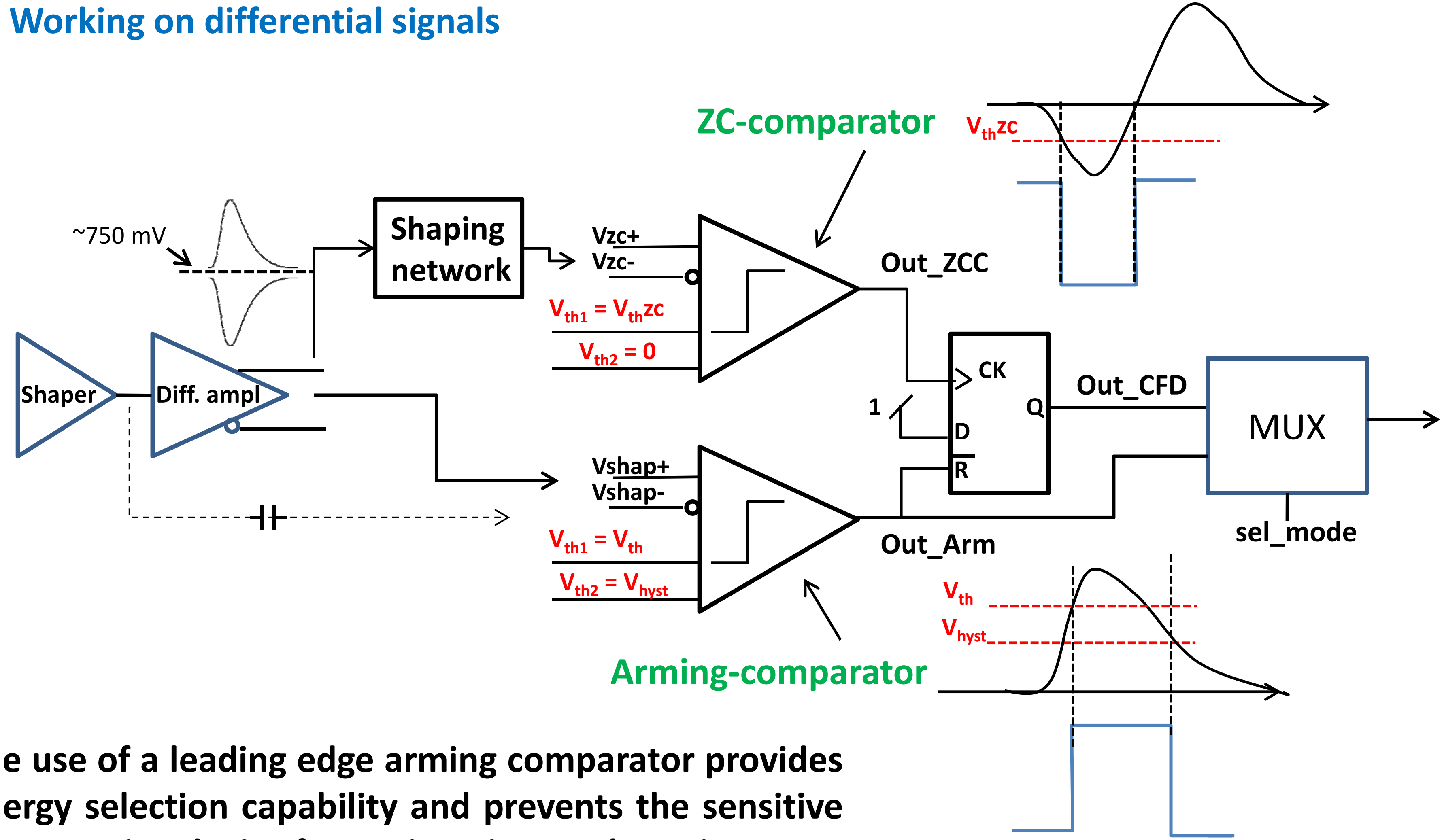
T_0	74.98 ÷ 75.12 ns
ΔT_0	0.14 ns



T_p [ns]	Crossing Time T_0 [ns]	Delay Time T_d [ns]	Fraction Factor	ΔT_0 [ns] (10 ÷ 1000 mV)
25	24.75	15	0.393	0.07
50	49.77	29.07	0.416	0.07
75	75.12	43.41	0.422	0.14
100	100.45	57.82	0.424	0.1
200	199.96	114	0.429	0.1

CFD block diagram

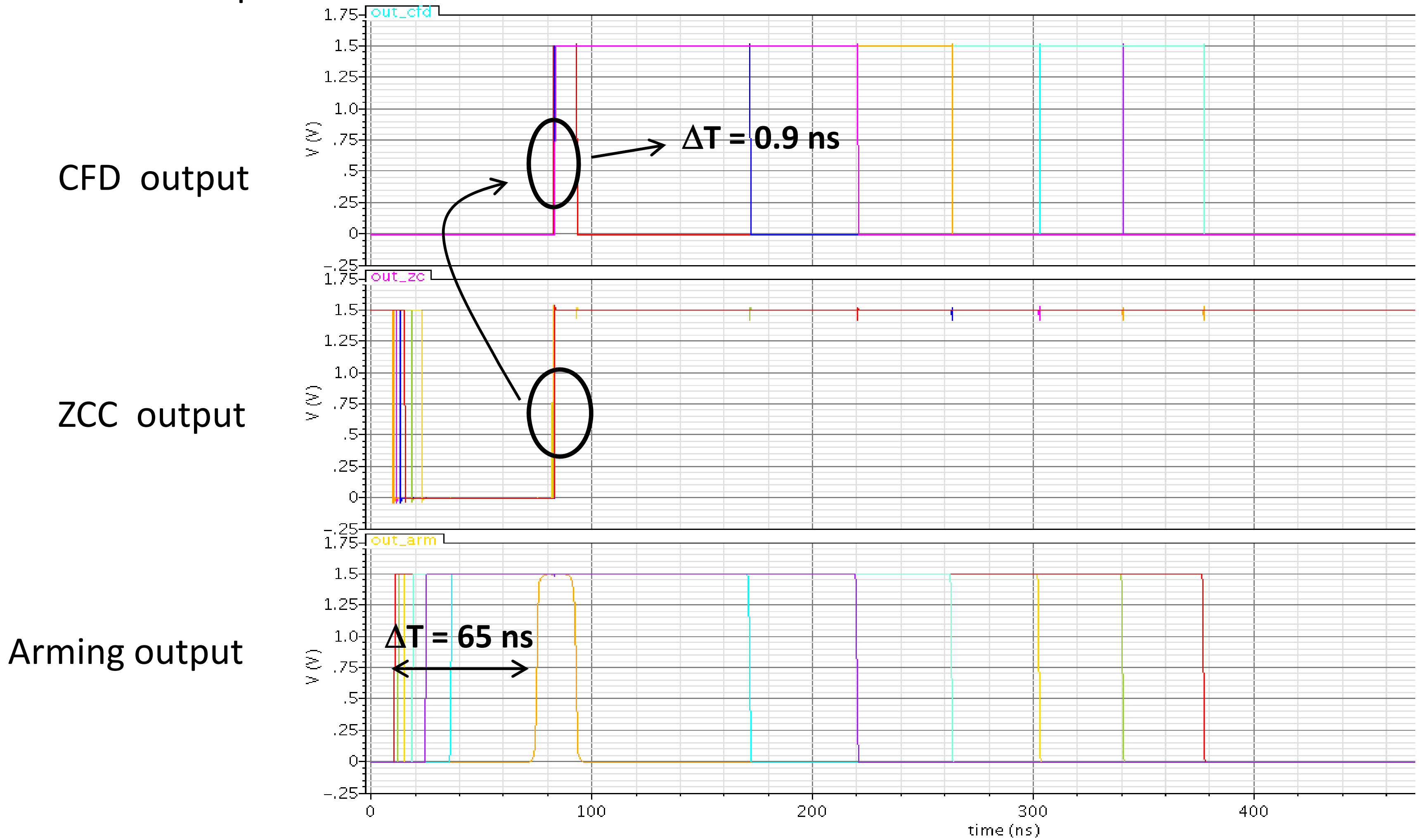
- Based on two identical comparators with hysteresis (60 µA + digital inverters)
- Working on differential signals



The use of a leading edge arming comparator provides energy selection capability and prevents the sensitive zero-crossing device from triggering on the noise

CFD simulations (T_p = 75 ns)

T_{peak} = 75 ns 10 mV (close to Vth) ≤ V_{in} ≤ 1000 mV



- Time walk < 1 ns in all configurations: (T_p = 25 ns, 50 ns, 75 ns, 100 ns and 200 ns)
- In case of T_p = 400 ns, using the CFD settings for 200 ns we get ΔT_0 ~ 3 ns

CFD Status

• CFD preliminary results look promising

• The Zero-crossing section quite mature (corner simulations looks fine)

• Arming section: 2 options
1. Single-ended shaper output (and AC coupling)
2. Differential outputs (same as CFD shaping network)

• We are working on Threshold network for option 2

• Probably not ready for August submission