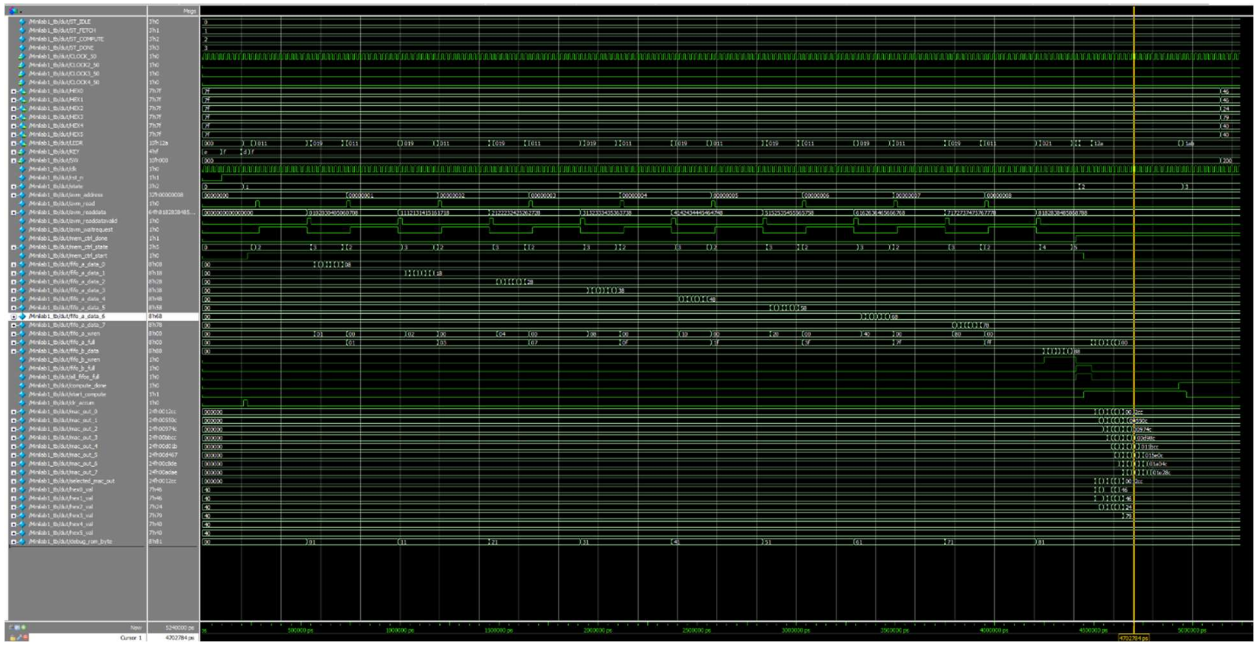
This is design we tested by doing the following:

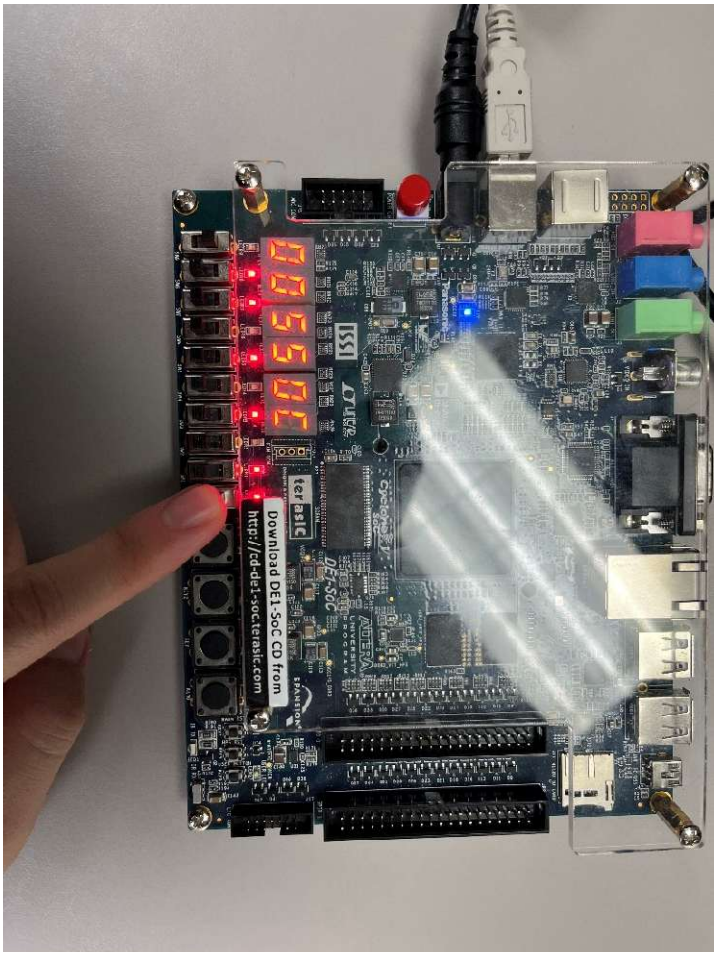
- We simulated our design by running scenarios that mirrors scenarios that may arise from operating the actual hardware. At the end we had mac output verification we checked each MAC value against the expected and displayed our output (then cross checked to see if we passed or failed)

```
VSIM 27> run
# Minilabl Testbench
# [0] Applying reset...
# [0] State: IDLE
# [200000] Reset complete. State = 0
# [200000] Pressing KEY[1] to start...
# [210000] State: FETCH
# [240000] Waiting for DONE state (state=3)...
# [4430000] State: COMPUTE
# [4950000] State: DONE
# [5040000] DONE state reached!
#
# MAC OUTPUT VERIFICATION
#   [PASS] MAC[0]: 0x0012cc
#   [PASS] MAC[1]: 0x00550c
#   [PASS] MAC[2]: 0x00974c
#   [PASS] MAC[3]: 0x00d98c
#   [PASS] MAC[4]: 0x011bcc
#   [PASS] MAC[5]: 0x015e0c
#   [PASS] MAC[6]: 0x01a04c
#   [PASS] MAC[7]: 0x01e28c
# Simulation complete.
# ** Note: $finish    : I:/ECE554/Minilablb/Minilabl_tb.sv(143)
#    Time: 5240 ns  Iteration: 0  Instance: /Minilabl_tb
```



2. We pipelined the MAC.

3. We flip the switch and then it shows us what the value is at that index in the vector.



5. We had a few different difficulties across different aspects of the minilab. Our main one was a bug with our FIFO where the signals were all coming in at the same time. We didn't initially think this was a problem but it caused errors in displaying our values on the FPGA. We found about this error through debugging and analyzing the waveform, which took up most of our labtime.

SignalTap:

4. Used AVM_READ as our trigger, with a sample size of 1K.