4 Slow Control

4.1 Overview

The slow control allows the user to configure & reset the chips manually. The six modules can be configured in parallel as shown in *Figure 15*.

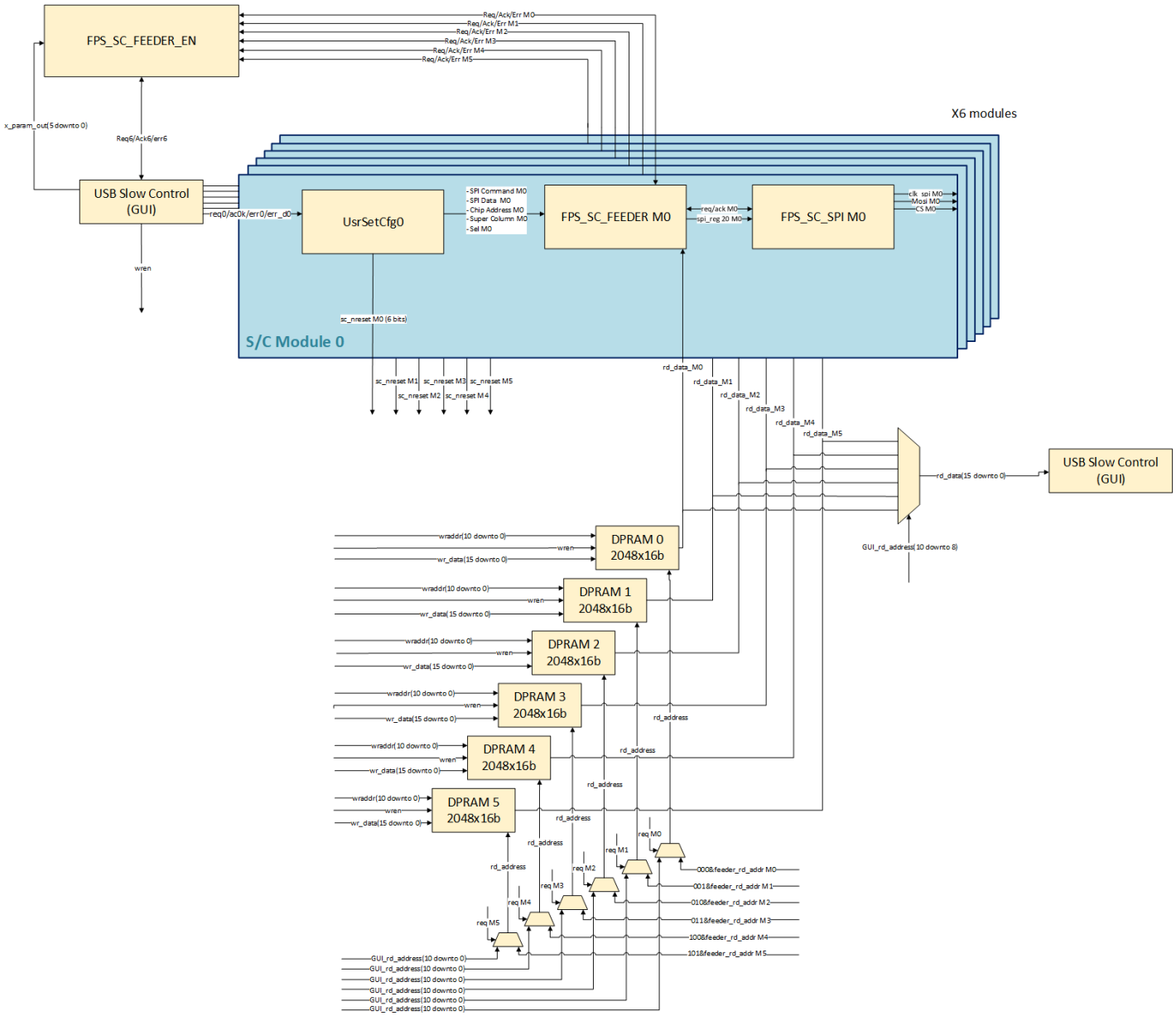

Figure 15 : Slow Control Architecture

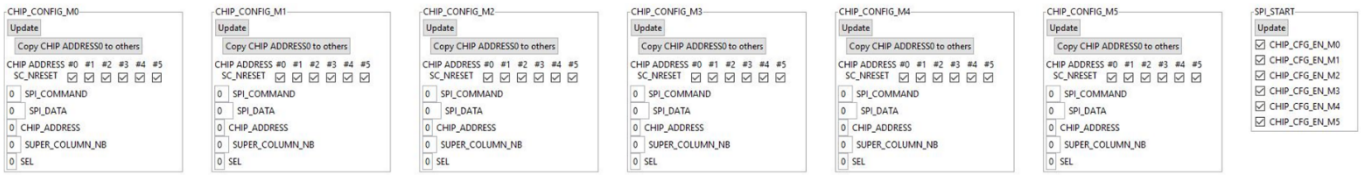

Figure 16 : Slow Control Configuration Registers/Bits

4.2 Entities details

4.2.1 FPS_SC_SPI

FPS_SC_SPI controls *spi_clk*, *spi_cs* and *spi_mosi* signals. It takes a 20-bits register at its input and serialises it upon request, then sends back an acknowledge when done.

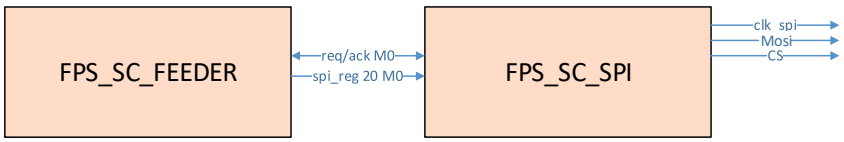

Figure 17 : FPS_SC_SPI interface

4.2.2 FPS_SC_FEEDER

FPS_SC_FEEDER provides the registers to serialise, to FPS_SC_SPI and makes a request. At its input are provided by the user the following information:

- SPI Command
- SPI Data
- Chip address
- Super column
- Sel

With sel, the user can choose to (upon SPI_START):

- Configure an entire super column with ***sel* = 0**
- Configure two entire super columns (of the same number) of two different asics with ***sel* = 1**
    - The two asics are given by chip_address(2 downto 1) & '0' and chip_address(2 downto 1) & '1'
- Send a single spi command with ***sel* = 2**
- Send a spi-reset when ***sel* = 3**

The SPI commands are constructed accordingly with what was defined in the chip specification document: FASER ASIC.

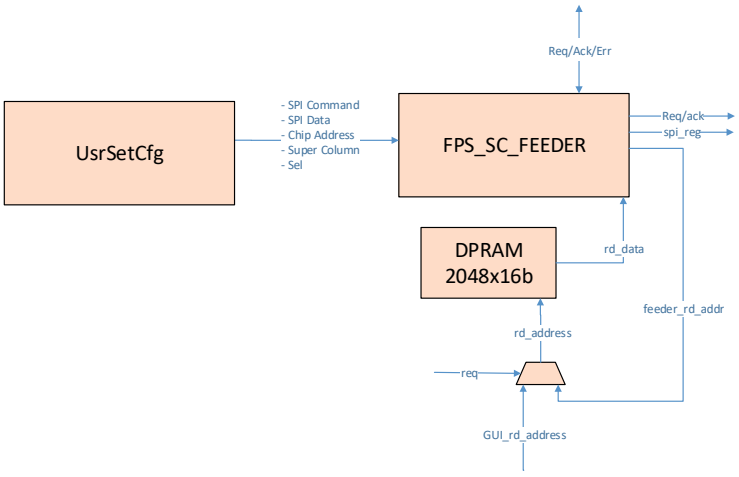

Figure 18 : FPS_SC_FEEDER interface

4.2.3 FPS_SC_FEEDER_EN

FPS_SC_FEEDER_EN manages which modules are to configure according with what the user has selected the SPI_START in the GUI box. It concentrates the feeders' acknowledges/errors into one. If at least one error is detected, it will propagate back to the Ethernet wrapper (via code). FPS_SC_CODE_MGR waits for every activated feeder to finish/acknowledge then generates a congregated acknowledge back to the Ethernet wrapper.

Explanation of FPS_SC_FEEDER_MGR & FPS_SC_CODE_MGR:

Upon an enable signal provided from the GUI via x_param_out, FPS_SC_FEEDER_MGR will manage req, ack and err signals that are interfaced with FPS_SC_FEEDER and will output a code with the following meaning:

- 01 if an error has been detected along with an acknowledge from FPS_SC_FEEDER
- 10 if an acknowledge alone has been detected from FPS_SC_FEEDER

The FPS_SC_CODE_MGR will transfer an error along with an acknowledge to the Ethernet wrapper if at least one enabled FPS_SC_FEEDER_MGR has output an error and all enabled FPS_SC_FEEDER_MGR has received an acknowledge. If all enabled FPS_SC_FEEDER_MGR have received an acknowledge, all without error, then FPS_SC_CODE_MGR will propagate an acknowledge without error back to the Ethernet wrapper.

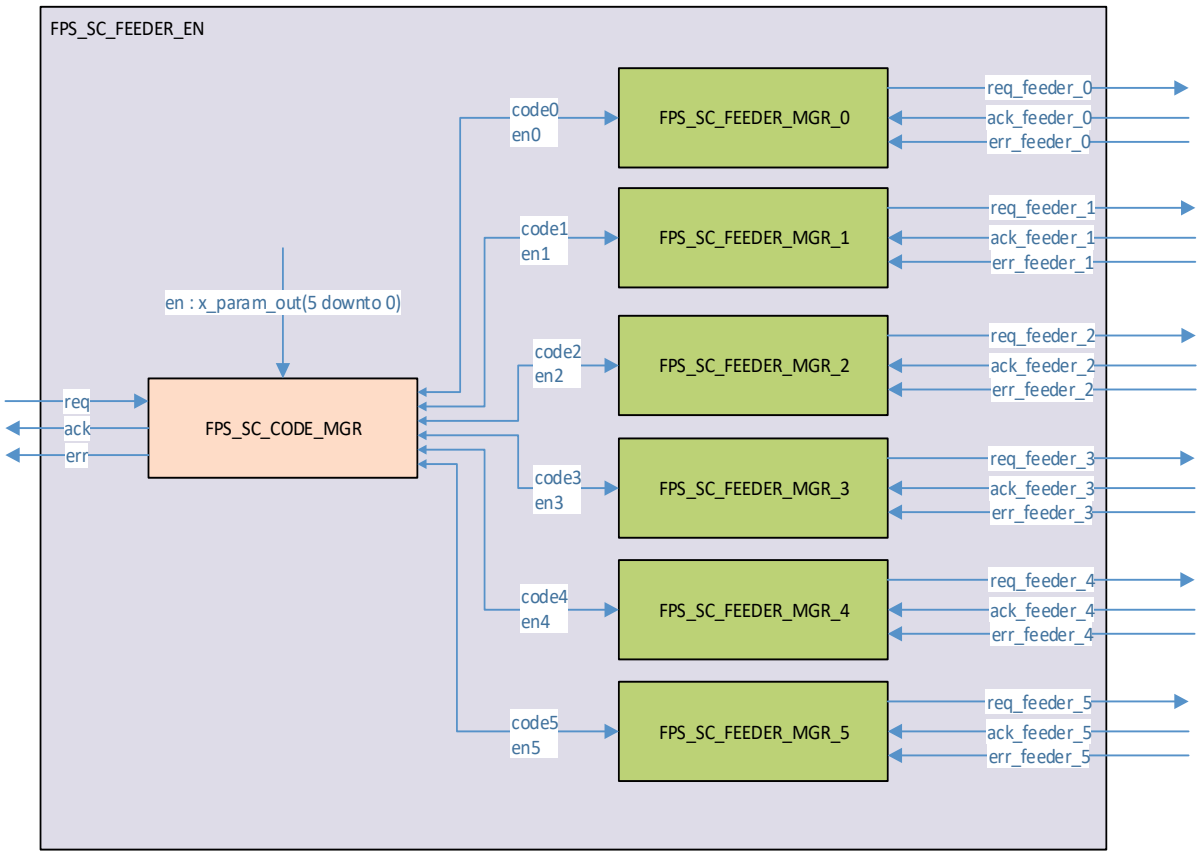

Figure 19 : FPS_SC_FEEDER_EN Block Diagram