

QVGPIO GPIO\_N[0..23] ♦
GPIO\_P[0..23] ♦

## POWER

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SYS\_5P0V I2C\_SDA♦ I2C\_SCL DSP\_YID[0..3] DSP\_XID[0..3] PROG\_IO**◇** USER\_LED**D** >REG\_EN[1..4] DSP\_FLAGD >1P0V >VDD\_DSP >1P35V UART\_RX< UART\_TXD D1P8V >VDD\_ADJ >VDD\_GPIO >2P5V RESET\_N**♦ →**3P3V VADC\_N < JTAG\_BOOT\_EN SPDIFD JTAG\_TDO TURBO\_MODED SPARE JTAG\_TCK paracard-power.sch

## <u>MountingHoles</u>

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dsys\_5pov

## NORTH

QVDDIO

PRXI\_LCLK\_P TXO\_LCLK\_PD
PRXI\_LCLK\_N TXO\_LCLK\_ND
PRXI\_FRAME\_P TXO\_FRAME\_PD
PRXI\_FRAME\_N TXO\_FRAME\_ND
QRXO\_RD\_WAIT\_P TXI\_RD\_WAIT\_PC
QRXO\_WR\_WAIT\_P TXI\_WR\_WAIT\_PC
QRXO\_WR\_WAIT\_N TXI\_WR\_WAIT\_PC
QRXO\_WR\_WAIT\_N TXI\_WR\_WAIT\_NC
PRXI\_DATA\_P[0..7] TXO\_DATA\_P[0..7]D
PRXI\_DATA\_N[0..7] TXO\_DATA\_N[0..7]D

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## SOUTH

QVDDIO

PRXI\_LCLK\_P

PRXI\_LCLK\_N

PRXI\_FRAME\_P

PRXI\_FRAME\_P

PRXI\_FRAME\_N

QRXO\_RD\_WAIT\_P

QRXO\_RD\_WAIT\_N

QRXO\_WR\_WAIT\_P

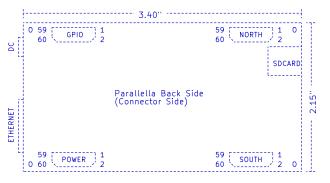
QRXO\_WR\_WAIT\_N

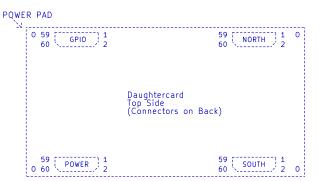
TXI\_WR\_WAIT\_N

PRXI\_DATA\_P[0..7]

PRXI\_DATA\_N[0..7]

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"Paracard" Daughtercard template for Adapteva Parallella—I. This schematic and associated PCB design may be used as a starting point for Parallella—I daughtercard design.

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