

Tcl's Syntax Parsing Overview

Command and Word **Separation**

Variable Return Value Substitution sequences of *white space* (space or horizontal tab) separate words

line endings and semicolons (;) separate commands

variable content (aka. its "value") gets inserted for a dollar (\$) followed by a valid variable name

return value of a command gets inserted for parts of a command line enclosed in square brackets

Command Execution

Applies *recursively* for nested command substitution, i.e. for *square brackets inside square brackets*.

use it as channel argument: puts \$chan [...]

From the syntax viewpoint only the *first word* is relevant – all the following words are evaluated by the command itself!

array name must be followed by index

unusual ("funny") names may need to be enclosed in curly braces

their return value

0

Ν

0

Q U

0

Ν

G

A backslash (\)at the very end of a line is special, as it concatenates a line with the next one, removing all leading white space

> **Backslash-***Substitutions* – to insert non-graphic characters (e.g. \n, \t, \a ... - like in C/C++)

Backslash-*Quoting* – to remove a special meaning from the directly following character (e.g. \; denotes a literal semicolon, not a Command Separator)

Quoting with Double Quotes (" ... ") – to remove the special meaning from Separators and Curly Brace Quoting, while still allowing Variable and Command Substitution.

Quoting with Curly Braces ({ ... }) – to remove the special meaning from Everything enclosed.

> For a full description in manual style see XILINX documentation ug835.

R ead	
T he	
F ine	
M anual	

Similar for commands string, clock, file ...

list-related but creates proper list from its arguments

commonality: first letter ell

in parentheses to access an element

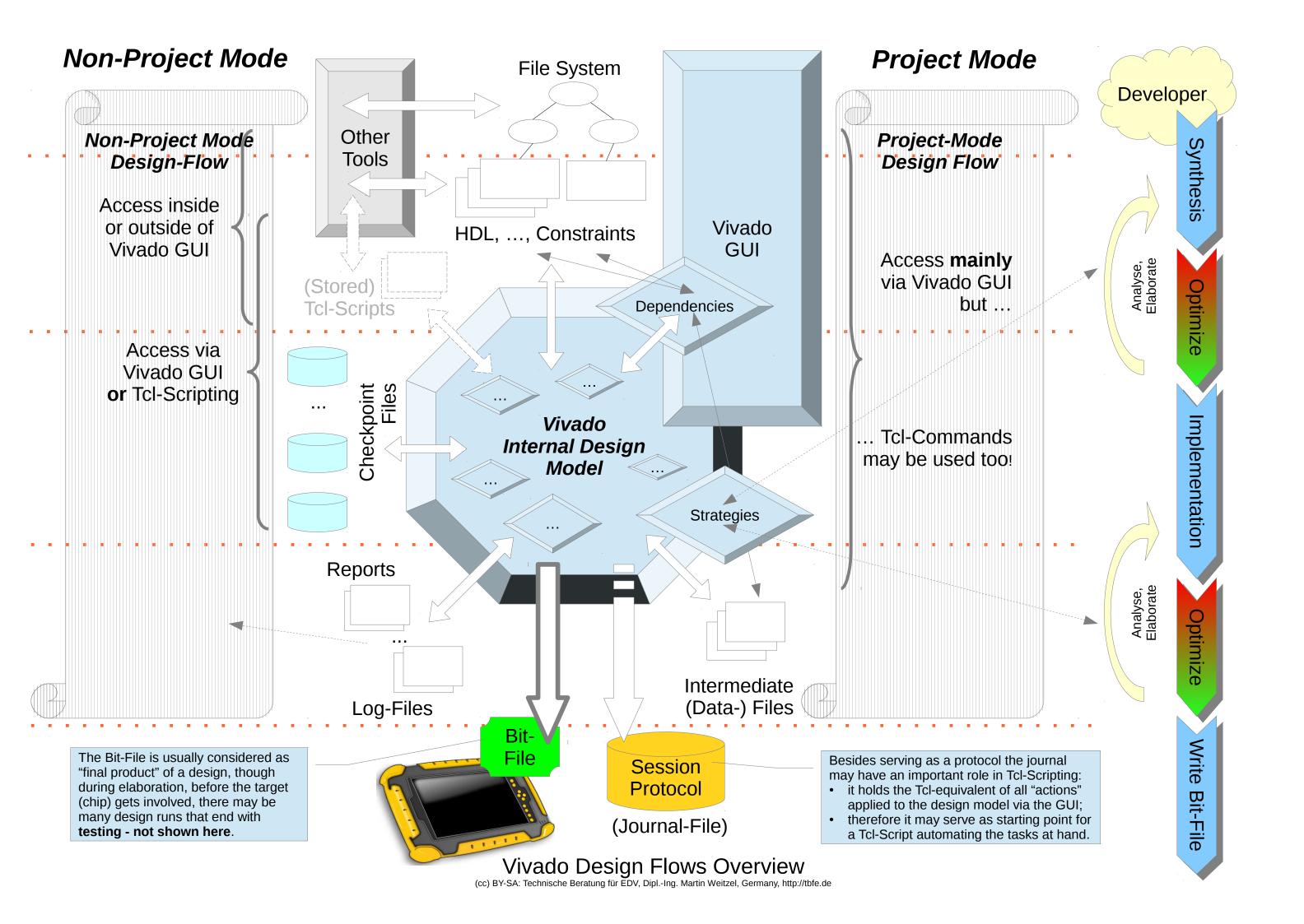
	Tcl (native)		Vivado
	Scarce – some hints in error messages when command execution fails so: RTFM	Syntax Help	All commands have a -help option, providing extensive explanations (close to the full manual page)
	Rather weak – stronger for (historically) newer commands compared to the "good ol" & ancient" commands	Uniformity	very strong (especially in comparison native Tcl commands – which need to be used nevertheless)
	Command Collections used for grouping, e.g. array set (get all elements of an array) array get (get all elements of an array) array size (get number of array elements) array names (get list of array indices)	Related Commands	Similar commands lexically grouped by common prefix, e.g.: •get_xyz (access xyz element of design model) •set_xyz (modify xyz element of design model) •report_xyz (generate xyz report) •
	Prominent exception: commands for <i>list</i> -processing, e.g.: olist time time olindex olsort		Similar command typically grouped under the same name, with an option to change their behaviour, e.g.: •create_file_set •create_fileset -constrset •create_fileset -simset
	 Minimalistic approach (for economy), i.e.: most commands with a "result" produce it as return value so, to "print" it to the console use: puts [] and to save it in a file open a channel store return value of open: set chan [open] 	Other (General)	Regular approach (for convenience), e.g. all report_xyz commands •by default produce their output on the console (window) •have a -file option to store the report in a file •have a -return_string option to deliver the report via

as a "matter of taste and style" and for economy because of memory limitations in the early 1990s, when development of Tcl started

Vivado vs. Tcl Syntax

largely bloats command look-up table (but not any more an issue considering CPU power and main memory size available today)

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"Non-Project Mode" is sometimes confused with using the Vivado Tcl-Commands only.

> It is well possible to mix Vivado **Tcl-Commands** and using the GUI.

Use the Vivado GUI for any nonrepetitive or mostly explorative elaboration and as a convenient way to view reports.

Non-Project Mode	Activity	Project Mode
Explicitely get HDL-Sources into Internal Model • read_vhdl • read_verilog	Preparing the Design Model	Manage file dependencies automatically via File Sets: create_project add_files
• read_xdc		• current_fileset
		• import
		open_projectcurrent_projectclose_project

Elaborating the Design

There are too many command to list exhaustively, so just some typical examples are given:

- get_cells (select and query design objects)
- set_property (modify design objects)
- report ... (generate various kinds of reports and summaries)

Run synthesis tools (various options allow to specify details) synth_design	Synthesis	Select and run tools depending on changes made (various options, including some for load-sharing		
Run implementation tools (rich on options, especially for optimization) opt_design place_design phys_opt_design route_design	Implementation	on compile servers): • launch_runs • wait_on_run		

Generating Target File

- write_bitstream (various options to select different formats and encoding)
- write verilog
- write vhdl
- write xdc

Creating the *Bitstream File* is typically the overall goal when using Vivado.

Usually these phases overlap and are repeated, depending on reports and other kinds of checks and verifications, including simulation (not shown here). If files – especially Verilog or VHDL – are modified, they need to be read again explicitely.

Vivado Modes and Tcl Commands

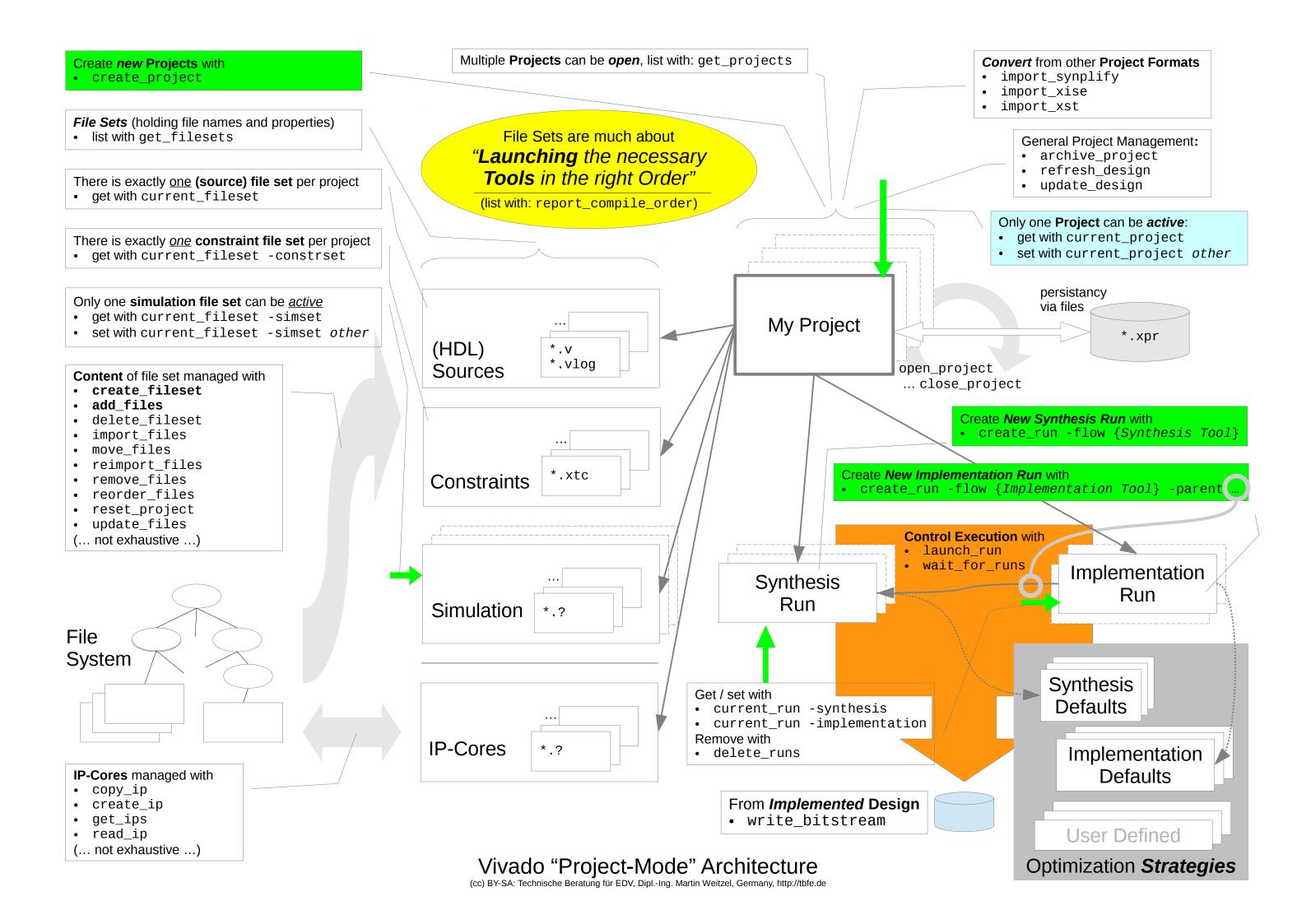
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"Project Mode" is sometimes confused with using the Vivado **GUI only.**

> It is well possible to mix using the **Vivado GUI** and Tcl-Commands.

Use Vivado Tcl-Commands to automate anything that is systematic and repetitive.

Usually these phases overlap and are repeated, depending on reports and other kinds of checks and verifications. If files Verilog or VHDL Files are modified, Vivado knows about dependencies and will launch the tools as required in the right order.



Concrete time values chosen for a rough orientation only (!)

accord to technical achievments around 2010...2015
still widely vary because of wide variations in technoloy

≥ ≈50 msec (only soft realtime)

μsecs ... msecs (maybe hard realtime)

nsecs ... μsecs (hard realtime)

psecs ... nsecs

fsecs ... psecs ...

High-Level Control, GUI, Web-Interface ...

... secs .. minutes ... (hours ... years)?

"User-Land" Processes

Critical Application Specific Software Components

Device Drivers (including Kernel Modifications)

Software Defined Logic in FPGA

Application Specific Hardware

Custom Built Hardware

"World of Scripting", e.g.

- JavaScript
- Perl
- Python
- Ruby
- Shell
- Tcl

... Though you may also find

- Java
- Scala
- C/C++
- Go
- ...

C/C++ (maybe Assembler too)

C/C++ and – in rare cases – Assembler

VHDL / Verilog

"Classic" Electric Engineering / Electronic Design

Softeare Layers vs. Real Time

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