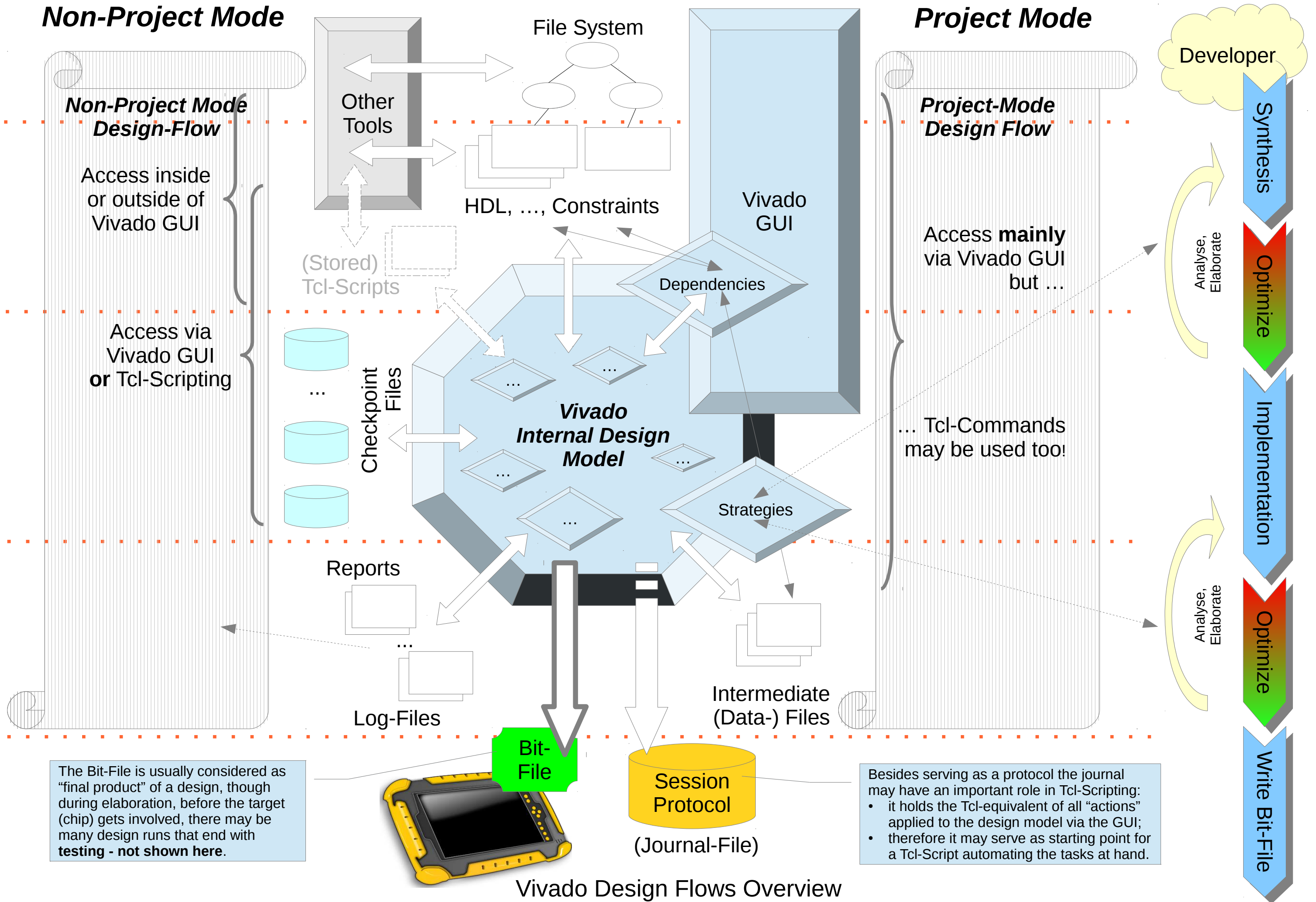
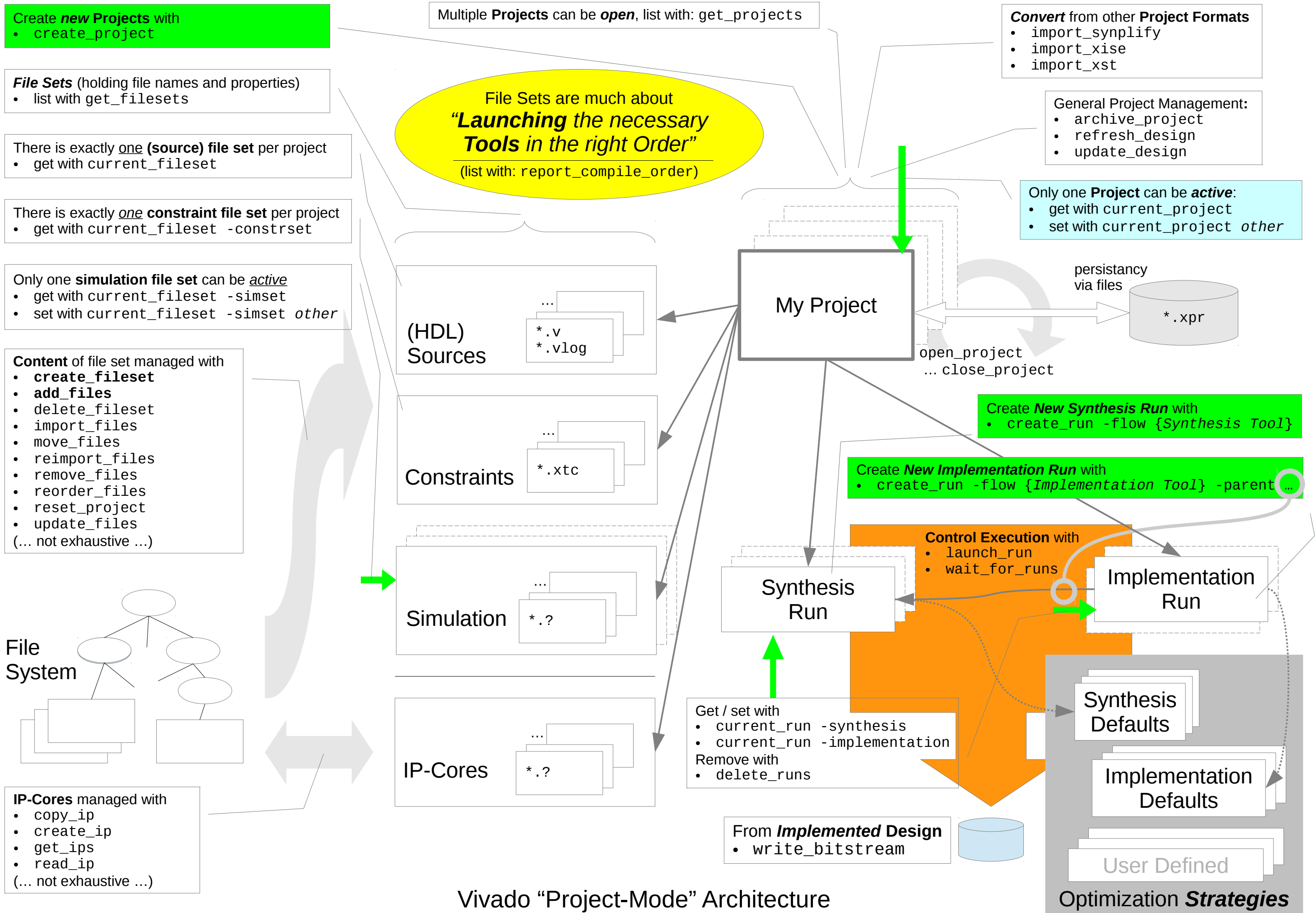


Non-Project Mode

Project Mode



Vivado Design Flows Overview



Vivado “Project-Mode” Architecture
(cc) BY-SA: Technische Beratung für EDV, Dipl.-Ing. Martin Weitzel, Germany, <http://tbfe.de>

“Non-Project Mode”
is sometimes
confused with using
the Vivado Tcl-
Commands only.

“Project Mode” is
sometimes confused
with using the Vivado
GUI only.

It is well
possible to
mix Vivado
Tcl-Commands
and using the
GUI.

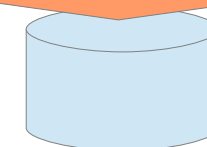
It is well
possible to mix
using the
Vivado GUI
and Tcl-
Commands.

Use the Vivado
GUI for any non-
repetitive or mostly
explorative
elaboration and as
a convenient way
to view reports.

Use Vivado Tcl-
Commands to
automate anything
that is systematic
and repetitive.

Non-Project Mode	Activity	Project Mode
Explicitely get HDL-Sources into Internal Model <ul style="list-style-type: none">• read_vhdl• read_verilog• read_xdc	Preparing the Design Model	Manage file dependencies automatically via File Sets: <ul style="list-style-type: none">• create_project• add_files
		• current_fileset
		• import_...
		<ul style="list-style-type: none">• open_project• current_project• close_project
Elaborating the Design		
There are too many command to list exhaustively, so just some typical examples are given: <ul style="list-style-type: none">• get_cells (select and query design objects)• set_property (modify design objects)• report_... (generate various kinds of reports and summaries)• ...		
Run synthesis tools (various options allow to specify details) <ul style="list-style-type: none">• synth_design	Synthesis	Select and run tools depending on changes made (various options, including some for load-sharing on compile servers): <ul style="list-style-type: none">• launch_runs• wait_on_run
Run implementation tools (rich on options, especially for optimization) <ul style="list-style-type: none">• opt_design• place_design• phys_opt_design• route_design	Implementation	
Generating Target File		
<ul style="list-style-type: none">• write_bitstream (various options to select different formats and encoding)• write_verilog• write_vhdl• write_xdc		

Creating the **Bitstream File** is typically the overall goal when using Vivado.



Vivado Modes and Tcl Commands

Usually these phases overlap and are repeated, depending on reports and other kinds of checks and verifications, including simulation (not shown here). If files – especially Verilog or VHDL – are modified, they need to be read again explicitly.

Usually these phases overlap and are repeated, depending on reports and other kinds of checks and verifications. If files Verilog or VHDL Files are modified, Vivado knows about dependencies and will launch the tools as required in the right order.