Comparch Journaling

12/23/23
I was traveling to Memphis,TN, and was on the road for most of the day, but I reviewed the document that was worked on and planned on meeting with my team to further discuss responsibilities and tasks that will be distributed. I was informed that they met for 90 minutes, and saw that they accomplished quite a bit, when we met in the classroom initially we decided on an accumulator, while two of our members wanted to do a stack we came to a consensus that this was the most likely to emphasize simplicity in our overall design.

1/8/24
I have not been able to make much progress with the design since we have not been able to meet together outside of class as a team, but I want to be more involved with the project than I currently am. While I missed the first meeting where a lot of the design decisions were determined, I don't want to make this a habit in the future as we work on later milestones.

1/12/2024
Met with Eleanor briefly to discuss milestone points that were missed in milestone 1 and how tasks will be distributed in the future as well as communication from here on forth over the RTL design and decisions on the registers that will be used and if we had enough as well. I began looking over the RTL to get a better understanding so that when we start on milestone 3 I am ready to coding and understand the calling conventions.

1/14/2024
We met for about an hour and discussed what tasks were left of the milestone. My main task was working on the memory map and looking over the calling conventions agreed upon for use in Verilog. Since we are not using any reserved space in memory besides within registers we just have a text/code, static memory, dynamic and stack memory in general for the stack pointer. Was tasked as a team to individually go over the RTL for a sanity check to make sure that it logically makes sense before continuing on to the milestone 3 and working on the datapath. Overall I had a bit more responsibilities and am working on having a much bigger contribution for the next milestone 3.

1/22/24
My two tasks that were assigned to me was writing the control signals and describing the control, and adding control units to the list of components. Adding the control units to the list of components was done fairly quickly, with just listing the inputs and outputs from the control and stating its behaviors. I think that Dan needed the control signals draw on the datapath and that was done over the weekend, which I did not know until I went to the document to see that it was already completed. I blame this on the tasks not being allocated very well, if you were doing anything with the datapath you would probably need to work on any of the tasks pertaining to that. On the next milestone I am hoping to do more of the coding so that I can have more tasks to do because right now it's disproportionate and I am currently the team member that is lacking in work done for the team, which I do not want to be. The work that I have started on is adding

to the project setup and the inputs for our control signals in verilog on vscode and I am hoping to get a lot more work in before our Thursday meeting.

1/28/2024

I have been working on writing the test-bench and base code for the register specifically for PC, Reggie, MDR, IR, and ALUout. I was originally given the register(PC, Reggie, MDR, IR, and ALUout), the immediate generator, and mem. But it seems that we didn't allocate enough tasks to everyone and Thomas wanted to take a few to work on some of the project so I just ended up doing the register code as well as the testbench code for the register. I would like to pick up more work in the subsequent milestone and keep it in the future probably because writing the register was pretty straight forward since all I am doing is changing whether or not the register is being written to and when to reset it so the code was very straightforward.
Elenaor worked on the finite state machine and I looked over it to make sure it looked okay, and overall I had a lot more work to do this time around and hope to work on the lab 7 due next week as well as pick up more work for when we start the brunt of integrating all of the components in this last milestone. I have been sick the past few days but am hoping to finish strong on this project.

2/3/24-2/5/24

I worked on the the lab 7 for the memory , in which I wrote the memory, controlled memory, connected memory control, and the test bench for each respective file. I had an away meet for track earlier this week and several assignments outside of two exams this week so was not able to do as much as I would have liked on the integration. Now that I only have three exams left for the quarter before it ends I can focus on the integration of my assigned parts and whatever is left to be allocated. I would say this past weekend I wrote about 550 lines for lab 7 and spent about 11-12 hours on this lab over the course of the weekend/Monday, just making sure that the testing was written correctly. I am a bit confused on whether or not the code for my test bench for the control is enough testing or do I need to do more extensive testing?

2/8/24

After my team meeting I was supposed to demo with Dr. Williams but realized that the connected control testbench was far from completed so had to implement a few changes before I could demo. After finishing up the test bench, I demoed with him and went over some new changes for memory that the client is requesting. The memory was originally 2^16 byte addressed memory but the new client is stating that that is too expensive and wants us to change our memory to word addressed memory. In order for this to work, I first need to make the connection I first wrote out that the connection with bytes and word to:
1 byte is 8 bits
16 bits is 1 word
2 bytes is 1 word
Therefore I will need to shift my bit by 1 in order to change our original byte addressed memory to word addressed via a memory wrapper. With this there are a few design decisions I will need

to discuss with my teammates on the memory map. I was going to hold off on doing this until we can get everyone in one place seeing that Elenaor will be busy the entire weekend with ROTC, which she informed us ahead of time, and I have a track meet all of Saturday morning and will not be getting back in the evening.

2/11/24
I have begun writing the memory wrapper that will be used to meet the client's new requirements as well as the assigned tasks given on teams.

2/12/24
I was busy today working with NSBE for an annual campus-wide event but began working on finishing the memory wrapper.

There has been a lot of tension on the team lately because Thomas has been a bit condescending in his statements toward me. For instance, earlier today, "I'm assuming Jada hasn't started yet so I'll get started on her stuff." He stated this at 12:38, I made a statement in the chat that I was working on it and he stated that he was finished with it at 12:42, which was not even 6 minutes. It's moments like this that we get to the end of the week during our meeting with Dr. Williamson and I have to sit there in front of my teammates and state the one thing I did because once again my tasks were done for me.

It is unprofessional to state this in a group chat, and humiliating even. I feel undervalued when the tasks that were assigned to me are done by him, and then later he becomes resentful when he does this work when he is not supposed to.

Thomas is very quick to be frustrated without actually communicating said frustrations to me, as well as making underhanded comments about my performance. I am trying my absolute best, and while I might not have a great grasp of the concepts as well as he does, I still try my hardest to get things done.

I am frustrated by his harassing me throughout the day and stating that I am making excuses when I am taking my time in my coding since he decided to not follow the original integration plan that Dan thoughtfully planned out (which would have worked fine).

I am very worried that we will put everything together in our integration testing and not only will it not work but he will be quick to point fingers stating he did all this work when it's supposed to be a team effort to offload the amount that one single individual is doing.

I dislike confrontation, but it never feels as though we are on the same page of the project. From the very beginning, it feels like there was not very much effort to see when all of us could meet, seeing that most of our schedules are not compatible: Thomas and I being student-athletes, Elenaor being in ROTC, and Dan being in Theatre.

I feel very disconnected from the group because when I don't perform as well it feels very much like there is resentment towards me. When deciding to meet as a group and knowing that most of us were very much traveling, the literal day that the winter break started was where it started. That already threw me out of the loop, especially with design decisions made. The only input I had was to, during the first meeting we had before the break, do the Accumulator.

I appreciate that Elenaor has helped me with some of my tasks when I have struggled with understanding parts of it as well as Dan. With each milestone, I have tried to pick up more work but always come to find that my work has already been done because of some imaginary daytime (that was not discussed during any team meeting but when Thomas wanted to start working) deadline(such as getting threats of taking my work if not done by 1:00 pm, which is such an arbitrary time).
It just sometimes feels like a hostile work environment, I am neurodivergent and it just can be very difficult to work at normal times of the day(So I typically work more at night because I get a lot more done during this time).

Currently, I am finishing stage 2 of the integration and the memory tonight and will be stopping by during office hours after discussing with my team via the work day or probably during the meeting time I will be going to Dr. Williamson's office. I feel as though any time I hear from my teammates, Thomas is yet again looking down on me, and honestly, I am very tired of it.

He states that he wants the project to be done by Wednesday but did not follow the integration plan for something like that to happen nor is he thinking about how any of us on the team may have exams throughout the week. I have three exams, during the 10th week and four final exams on Monday and Tuesday.

2-12-2024

So quite a bit has happened today, I was finishing up integrating the memory file into the vscode and had to do some debugging to make sure that the sizes of each component was correct. I talked with Eleanaor and heard from a different perspective of how I was being viewed in this situation and took time to fix the root of the problem. Which was that I did not have the Stage 2 done and we are trying to finish integration testing. I understand that I need to work on things earlier than said deadline so that my teammates and I are on the same page, and understand that Thomas was not being malicious as much as he just was frustrated that I was not done when I was supposed to be for stage 2.

We met for four hours yesterday to make sure all of the stages were compiling and the testbenches were passing for all 5 stages. Then we called it a night since some of us have an exam on Tuesday.

I went to Dr. Williamson’s office to discuss how exactly was I supposed to bring in the code from the lab 7 into our actual code and made a list of the things that needed to be accomplished:
-Need to add the memory text file to the git repo for testing

-make an additional test bench for the memory wrapper which meets the new quota made by the client to go from byte addressed memory to word addressed memory
-finish the stage 2 testbench
-simulate the testbenches on modelsim to make sure that the memory can be written and read from the text file so essentially check to make sure that it is working.

All of these tasks were accomplished and now the assembler is being worked on and looks like we have to make some changes to the branch mem since we are going from byte addr to word addr memory and it can no longer reach that spot in memory that we had originally in the document. Other than that it looks like we are making better progress, this was the first time in a while in which we as a group met up and it was very fun and not nearly as tense as our previous meetings at all. I felt comfortable to ask for help and get and receive input on my work so hoping that everything starts coming together since we have completed the stages now and are now integrating and entering the debugging stage.