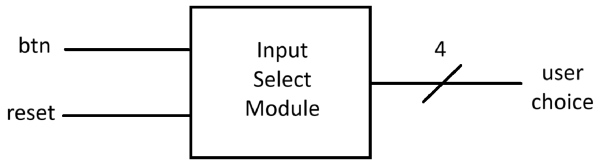
Input Select Module

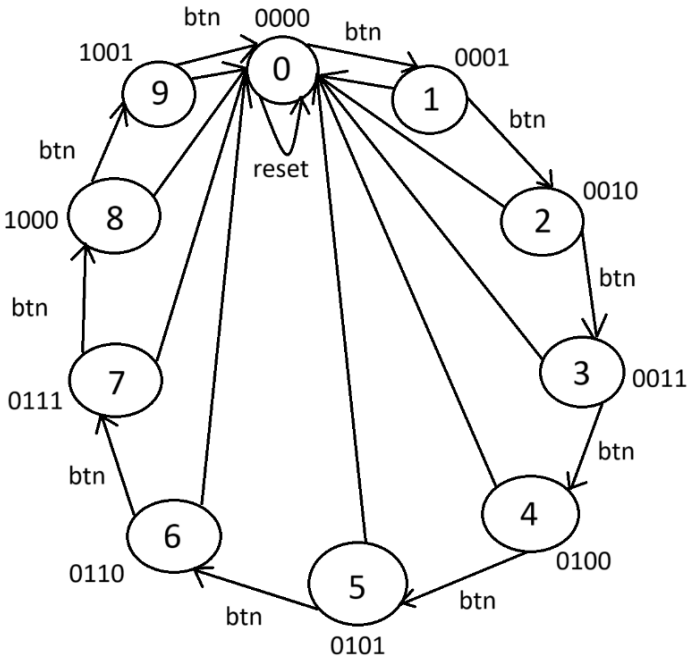
Inputs
btn -> increment button
reset -> reset button

Outputs
user_choice -> 4 bit user choice

This module is a simple counter that increments 4 bit user_choice from 0 to 9 on the positive edge of a button. If user_choice is 9, incrementing sets user_choice back to 0. Reset can be used to set user_choice to 0 at any time.



State Diagram



This represents the states and transitions of user_choice

Full Adder Module

Truth Table

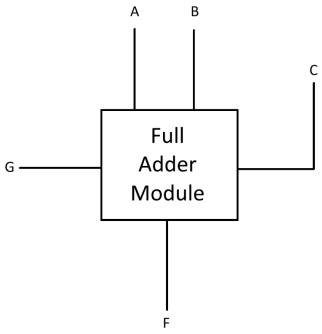
A	B	C	F	G
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

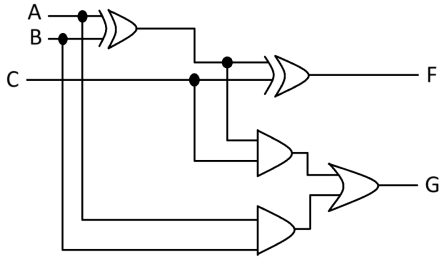
Inputs

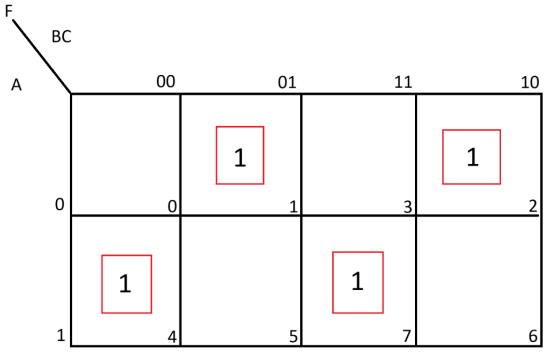
A -> input bit
B -> input bit
C -> carry in

Outputs

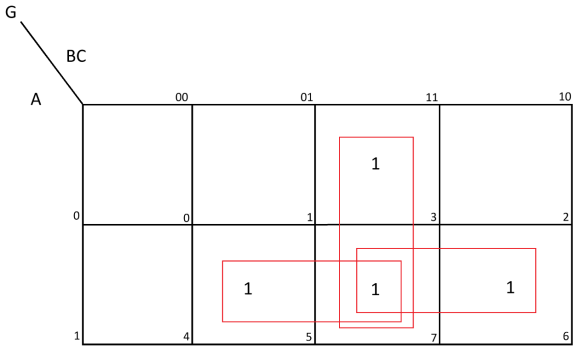
F -> sum
G -> carry out







F = ∑m(1,2,4,7)
F = A'B'C + A'BC' + AB'C' + ABC
F is 1 when an odd number of inputs are 1.
XOR is 1 when an odd number of inputs are 1.
F = (A ^ B) ^ C
F = A ^ B ^ C

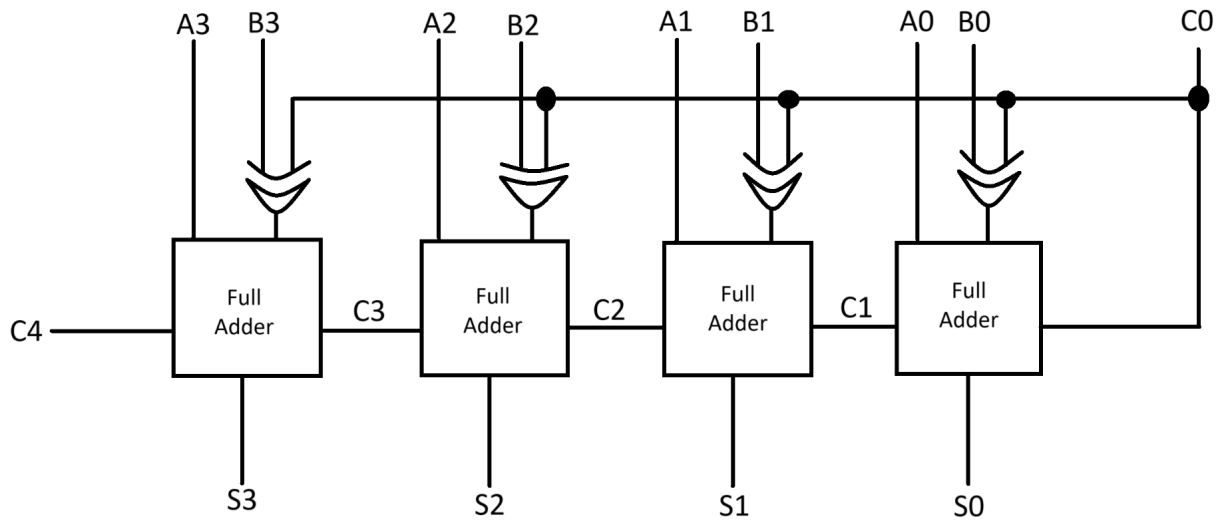


G = ∑m(3, 5, 6, 7)
G = -11 + 1-1 + 11-
G = BC + AC + AB

Ripple Carry Adder Subtractor Module

Inputs
A -> 4 bits
B -> 4 bits
C0 -> carry in (mode select)

Outputs
S -> 4 bit sum or difference
C4 -> carry out

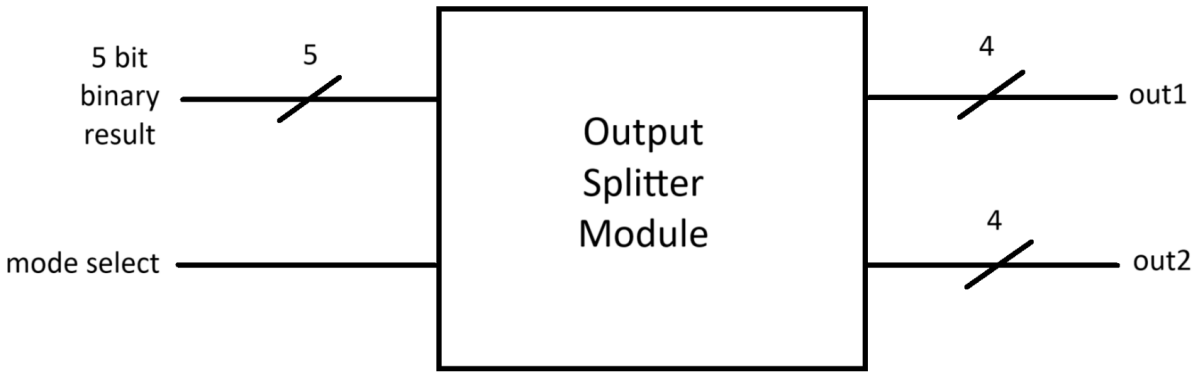


This module takes two 4 bit inputs A and B and a carry in C0 that functions as the mode selector. If the carry in is 0, A and B are added. If the carry in is 1, subtraction is performed by inverting the bits of B and adding 1 from the carry in. The module has a 5 bit output. The sum S represents the lower 4 bits of the output. C4 represents the most significant 5th bit of the output.

Output Splitter Module

Inputs	**Outputs**
bin -> 5 bit binary result from adder	out1 -> 4 bits to decoder
mode_select -> mode select	out2 -> 4 bits to decoder

This module takes the 5 bit result from the adder subtractor and uses case statements to split it into two 4 bit outputs that can be properly decoded by the 4 bit 7 segment decoder. There are case statements for each possible output from -9 to 18. This module also takes the mode selector as an input. When mode select is 1 (subtraction), the module flips the most significant bit of the 5 bit result before interpreting it. This has to be done to ensure the proper output on the display.



Still Needs

- **Equations**
- **Logic Circuit**

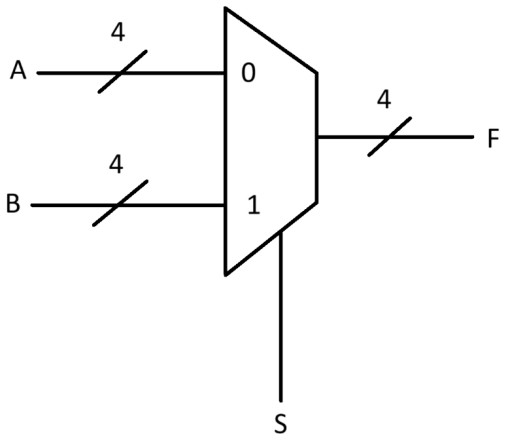
Output Splitter Truth Table

Decimal	A	B	C	D	E	I3	I2	I1	I0	J3	J2	J1	J0
0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	1	0	0	0	0	0	0	0	1
2	0	0	0	1	0	0	0	0	0	0	0	1	0
3	0	0	0	1	1	0	0	0	0	0	0	1	1
4	0	0	1	0	0	0	0	0	0	0	1	0	0
5	0	0	1	0	1	0	0	0	0	0	1	0	1
6	0	0	1	1	0	0	0	0	0	0	1	1	0
7	0	0	1	1	1	0	0	0	0	0	1	1	1
8	0	1	0	0	0	0	0	0	0	1	0	0	0
9	0	1	0	0	1	0	0	0	0	1	0	0	1
10	0	1	0	1	0	0	0	0	1	0	0	0	0
11	0	1	0	1	1	0	0	0	1	0	0	0	1
12	0	1	1	0	0	0	0	0	1	0	0	1	0
13	0	1	1	0	1	0	0	0	1	0	0	1	1
14	0	1	1	1	0	0	0	0	1	0	1	0	0
15	0	1	1	1	1	0	0	0	1	0	1	0	1
16	1	0	0	0	0	0	0	0	1	0	1	1	0
17	1	0	0	0	1	0	0	0	1	0	1	1	1
18	1	0	0	1	0	0	0	0	1	1	0	0	0
-9	1	0	1	1	1	1	0	1	0	1	0	0	1
-8	1	1	0	0	0	1	0	1	0	1	0	0	0
-7	1	1	0	0	1	1	0	1	0	0	1	1	1
-6	1	1	0	1	0	1	0	1	0	0	1	1	0
-5	1	1	0	1	1	1	0	1	0	0	1	0	1
-4	1	1	1	0	0	1	0	1	0	0	1	0	0
-3	1	1	1	0	1	1	0	1	0	0	0	1	1
-2	1	1	1	1	0	1	0	1	0	0	0	1	0
-1	1	1	1	1	1	1	0	1	0	0	0	0	1

2 to 1 Multiplexer Module

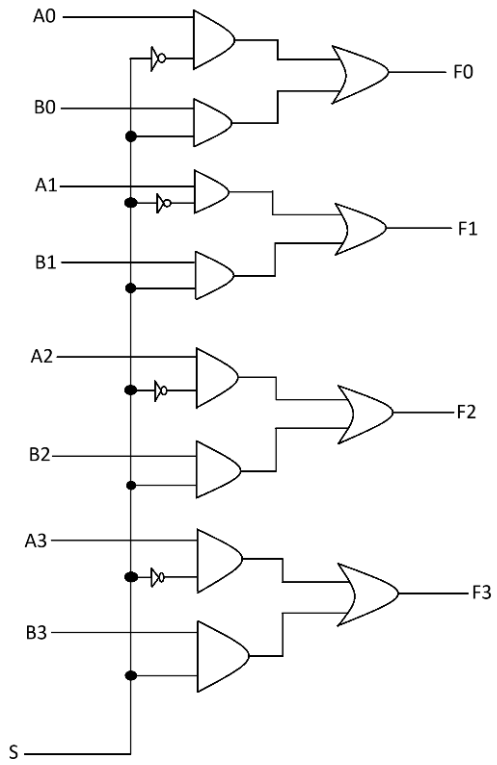
Inputs
A -> 4 bit binary
B -> 4 bit binary
S -> Selector

Outputs
F -> 4 bit binary



F = S ? B : A;
If S is 1, select B. Otherwise, select A.

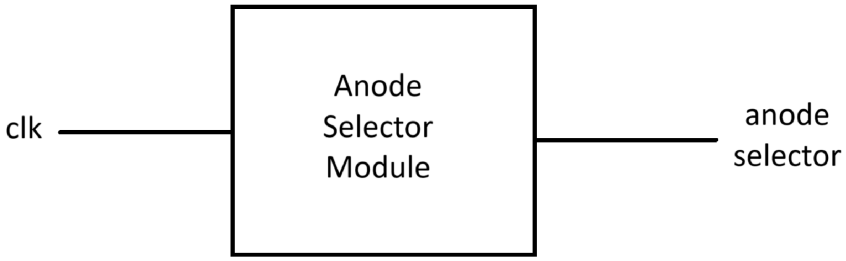
S	F
0	A
1	B



Anode Selector Module

Inputs
clock

Outputs
anode selector



At the positive edge of the clock, toggle the anode selector.

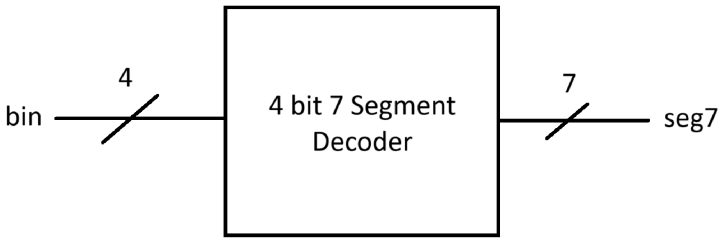
Clock (rising edge)	Anode Selector (current)	Anode Selector (next)
0 -> 1	0	1
0 -> 1	1	0

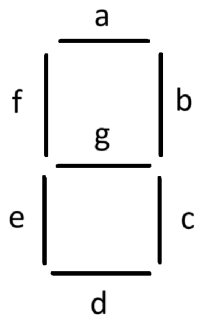
4 Bit 7 Segment Decoder Module

Inputs
bin -> 4 bit binary input

Outputs
seg7 -> 7 bit LED cathode outputs, active high assumes common anode LEDs

A	B	C	D	a	b	c	d	e	f	g
0	0	0	0	1	1	1	1	1	1	0
0	0	0	1	0	1	1	0	0	0	0
0	0	1	0	1	1	0	1	1	0	1
0	0	1	1	1	1	1	1	0	0	1
0	1	0	0	0	1	1	0	0	1	1
0	1	0	1	1	0	1	1	0	1	1
0	1	1	0	1	0	1	1	1	1	1
0	1	1	1	1	1	1	0	0	0	0
1	0	0	0	1	1	1	1	1	1	1
1	0	0	1	1	1	1	1	0	1	1
1	0	1	0	X	X	X	X	X	X	X
1	0	1	1	X	X	X	X	X	X	X
1	1	0	0	X	X	X	X	X	X	X
1	1	0	1	X	X	X	X	X	X	X
1	1	1	0	X	X	X	X	X	X	X
1	1	1	1	X	X	X	X	X	X	X





Still Needs

- **K map**

Top Module

Inputs
btn1
btn2
reset
mode selector
equals switch
clock
anode selector

Outputs
seg7