Small-Signal Modeling for MOSFET

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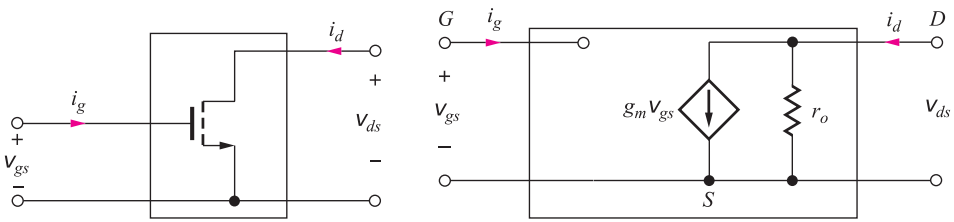
Small Signal Model

MOSFET Small Signal Model

Intro

- It's required to have a linear model, as in the other devices, that is valid for small *Vs* & *Is* changes to use all the info acquired so far to analyze it in ac
- We consider a MOSFET as a 3-terminal device (Source, Drain and Gate) and we explore the changes when it is operated as a 4-terminal one (Source, Drain and Gate + Back-gate)
- Small-Signal model is based on a 2-port network, in which the input port are defined as v_{gs} and i_g
- The output variables are defined as v_{ds} and i_d



- Those variables are defined as:

$$i_g = g_\pi v_{gs} + g_r v_{ds} \qquad i_d = g_m v_{gs} + g_0 v_{ds}$$

Intro

- Above parameters can be re-written as
  $g_\pi = \frac{i_g}{v_{gs}} |_{v_{ds}=0} \frac{\partial i_G}{\partial v_{GS}} |_{Q-point}$ $g_m = \frac{i_d}{v_{gs}} |_{v_{ds}=0} \frac{\partial i_{DS}}{\partial v_{GS}} |_{Q-point}$
  $g_r = \frac{i_g}{v_{ds}} |_{v_{gs}=0} \frac{\partial i_G}{\partial v_{DS}} |_{Q-point}$ $g_0 = \frac{i_d}{v_{ds}} |_{v_{gs}=0} \frac{\partial i_{DS}}{\partial v_{GS}} |_{Q-point}$
- It is possible to evaluate such parameters of the large-signal model for I_D of the active MOS
  $i_D = \frac{K_n}{2}(v_{GS} - V_{TN})^2(1 - \lambda v_{DS})$

Intro

- By considering the follow condition $v_{DS} \geq v_{GS} - V_{TN}$ & $i_G = 0$ where $K_N = \mu_n C_{ox}(\mathrm{W/L})$ $g_\pi = \frac{\partial i_G}{\partial v_{GS}} |_{V_{DS}=0}$
  $g_m = \frac{\partial i_{DS}}{\partial v_{GS}} |_{Q-point} = K_n(V_{GS} - V_{TN})(1 - \lambda V_{DS}) = \frac{2I_D}{V_{GS}-V_{TN}}$
  $g_r = \frac{\partial i_G}{\partial v_{DS}} |_{V_{GS}=0}$
  $g_0 = \frac{\partial i_{DS}}{\partial v_S} |_{Q-point} = \lambda \frac{K_n}{2}(V_{GS} - V_{TN})^2 = \frac{\lambda I_D}{1+\lambda V_{DS}} = \frac{I_D}{\lambda^{-1}+V_{DS}}$
  As i_G is always 0, ergo v_{GS} and v_{DS}, g_π and g_r are also zero
- As the gate terminal is isolated from the channel, it is expected that the input resistnace of the MOSFEt is ∞
- In a similar way as for the BJT Transconductance:
  $g_m = \frac{I_D}{\frac{V_{GS}-V_{TN}}{2}}$ Output resistance: $r_0 = 1/g_0 = \frac{\frac{1}{\lambda}+V_{DS}}{I_D} = \frac{1}{\lambda I_D}$

Intrinsic voltage Gain

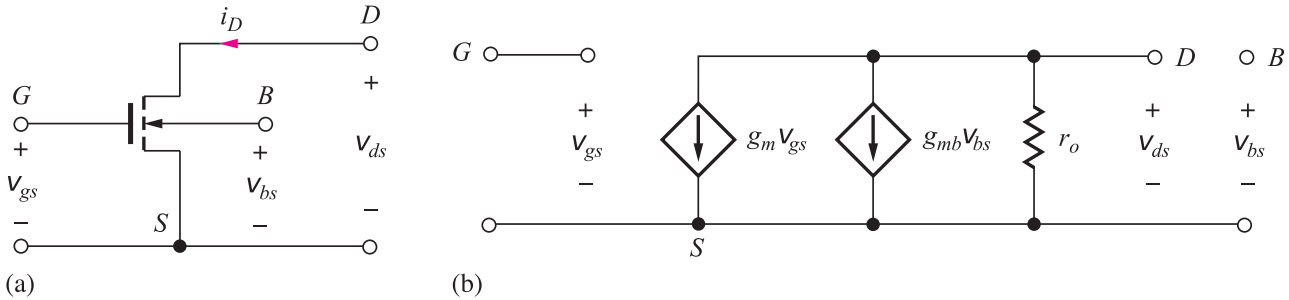
- Another key difference among BJT and MOSFET relies in the variation of the intrinsec voltage gain μ_f
- It is defined as $\mu_f = g_m r_0 = \frac{\frac{1}{\lambda} + V_{DS}}{\frac{V_{GS} - V_{TN}}{2}}$ and $\mu_f \approx \frac{2}{\lambda(V_{GS} - V_{TN})} \approx \frac{1}{\lambda}\sqrt{\frac{2K_n}{I_D}}$ all this under the condition that $\lambda V_{DS} \ll 1$
- μ_f for the MOSFET decreases as the operating current increases, ergo, the largest is the operation current , the smaller is the voltage gain capability

Small-Signal Operation

- Linear operation limits for the MOSFET can be obtained by using the simplified drain current (λ=0) $i_D = \frac{K_n}{2}(v_{GS} - V_{TN})^2$ for $v_{DS} \leq v_{GS} - V_{TN}$
- By expanding the equations related to $v_{GS} = V_{GS} + v_{gs}$ & $i_D = I_D + i_d$, we've
  $I_D + i_d = \frac{K_n}{2}(v_{GS} - V_{TN})^2 + 2v_{gs}(v_{GS} - V_{TN}) + v_{gs}^2$ as
  $I_D = (K_n/2)(v_{GS} - V_{TN})^2$, we've got
  $i_d = \frac{K_n}{2}[2v_{gs}(v_{GS} - V_{TN}) + v_{gs}^2]$ to keep linearity, we've
  $v_{gs}^2 \ll 2v_{gs}(v_{GS} - V_{TN})$ or $v_{gs} \ll 2(v_{GS} - V_{TN})$ by using a facto to "ensure" the inequality $v_{gs} \leq 0.2(v_{GS} - V_{TN})$
- As MOSFEt can be biased with $(v_{GS} - V_{TN})$ that can be several volts larger than for BJT, ergo, it can drive larger voltages for v_{gs} useful for RF amplifiers
- Drain current is defined as $\frac{i_d}{I_D} = \frac{g_m v_{gs}}{I_D} = \frac{0.2(v_{GS} - V_{TN})}{\frac{v_{GS} - V_{TN}}{2}} \leq 0.4$

Body Effect at 4-terminal MOSFET

- When background terminal is not connected to source, another controlled source needs to be added to the small-signal model



$I_D = \frac{K_n}{2}(v_{GS} - V_{TN})^2$ and
$V_{TN} = V_{TO} + \gamma(\sqrt{v_{SB} + 2\phi_F} - \sqrt{2\phi_F})$

- As drain current depends on the threshold voltage and it changes as does v_{SB}, ergo a back-gate transconductance is defined as: $g_{mb} = \frac{\partial i_D}{\partial v_{BS}} \mid_{Q-point} = -\frac{\partial i_D}{\partial v_{BS}} \mid_{Q-point} =$
$-\left(\frac{\partial i_D}{\partial V_{TN}}\right)\left(\frac{\partial V_{TN}}{\partial v_{SB}}\right) \mid_{Q-point}$

Body Effect at 4-terminal MOSFET

- By evaluating the gradients

$$\frac{\partial i_D}{\partial V_{TN}} \mid_{Q-point} = -K_n(v_{GS} - V_{TN}) = -g_m$$

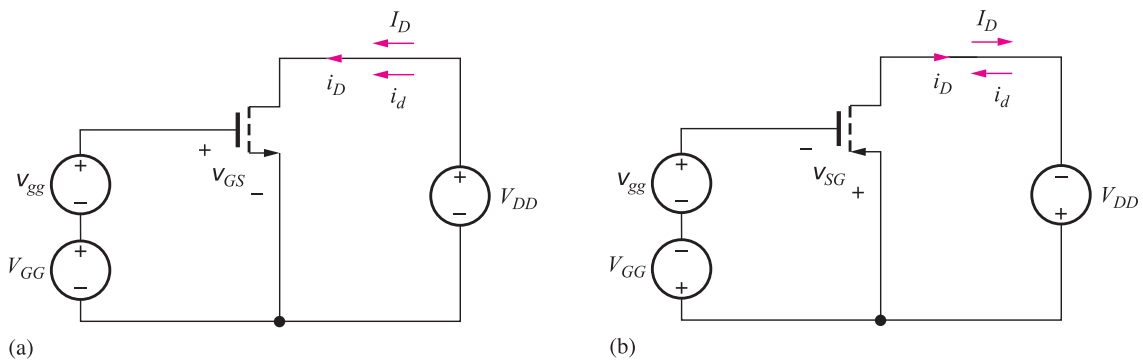
and

$$\frac{\partial V_{TN}}{\partial v_{SB}} \mid_{Q-point} = \frac{\gamma}{2\sqrt{V_{SB} + 2\phi_F}} = \nu$$

- where ν represents the back-gate transconductance $g_{mb} = -(-g_m)\nu$ or $g_{mb} = \nu g_m$, where it works only for 0 to 1

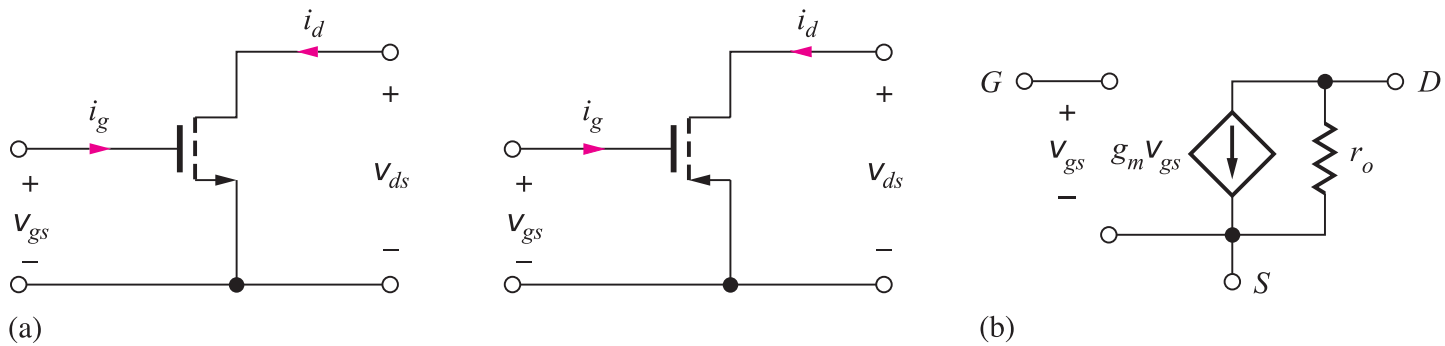
Small-Model Signal for a PMOS

- In a similar way as for the BJT pnp or npn for MOSFET, NMOS and PMOS have a similar behavior
- Both are biased by a dc source V_{GG} allowing the Q-point current I_D, for each case a v_{gg} is added for each case in series to V_{GG} allowing to increase the gate-source on each transistor



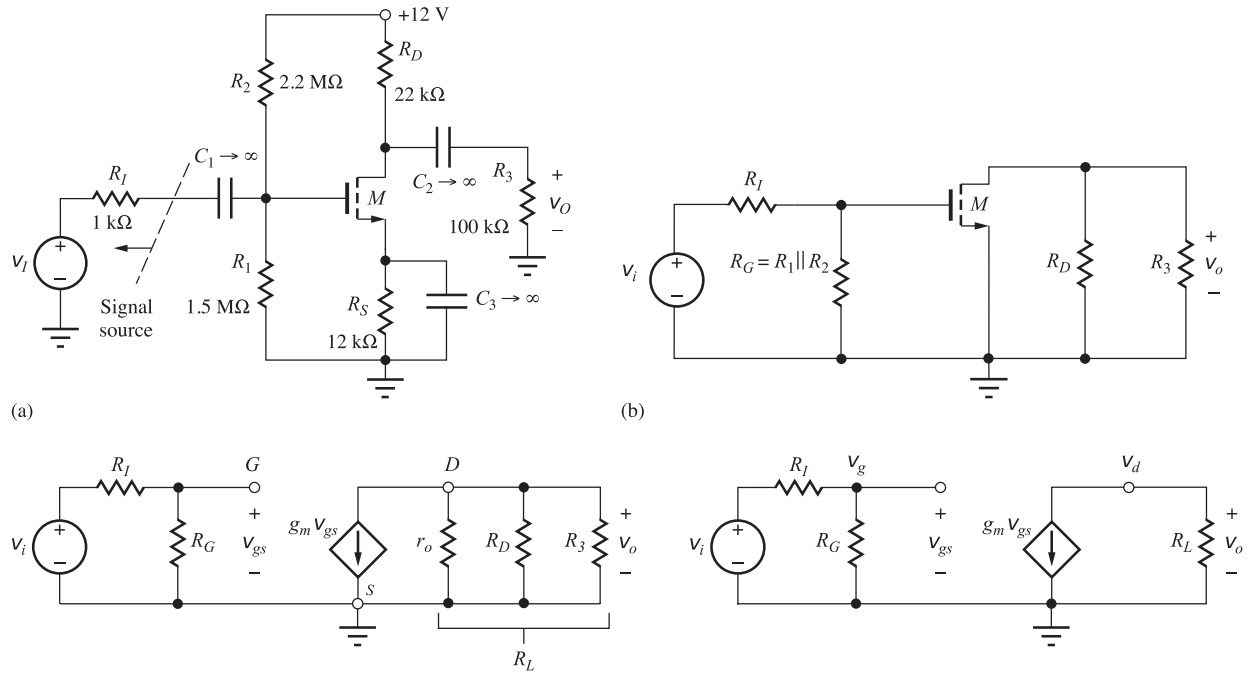
Small-Model Signal for a PMOS

- For the NMOS, the total gate-source and drain current are $v_{GS} = V_{GG} + v_{gg}$ and $i_{DS} = I_D + i_d$
- For the PMOS $v_{SG} = V_{GG} - v_{gg}$ and $i_{DS} = I_D - i_d$



Common Source Amplifier

- We are now with the basic enough knowledge, ish, to analyze the small-signal characteristics of a common-source amplifier that considers an enhanced n-channel within a 4-resistor network



- We've analyze this array before, the key difference that appears in here is that r_π as an open circuit

Common Source Amplifier

- In a similar way, the gain for a common-source terminal is defined as:

$$A_{vt}^{CS} = \frac{v_d}{v_g} = \frac{v_0}{v_g}$$

where $v_0 = -g_m v_{gs} R_L$ and $A_{vt}^{CS} = -g_m R_L$

- Source Voltage Gain is written as

$$A_v^{CS} = \frac{v_0}{v_i} = \left(\frac{v_0}{v_g}\right)\left(\frac{v_g}{v_i}\right) = A_v^{CS}\left(\frac{v_g}{v_i}\right)$$

where $v_g = v_i \frac{R_G}{R_G + R_I}$ ergo, the general gain voltage for a common-source amp is defined as

$$A_v^{CS} = -gmR_L\left(\frac{R_G}{R_G + R_I}\right)$$

Input Resistance for the Common Emitter and Source Amp

- The small-signal can be larger in a MOSFET than in a BJT as well as the input impedance
- Input resistance R_{in} coupled to C_1. R_{in} is the total resistance of the signal source by v_i and R_i

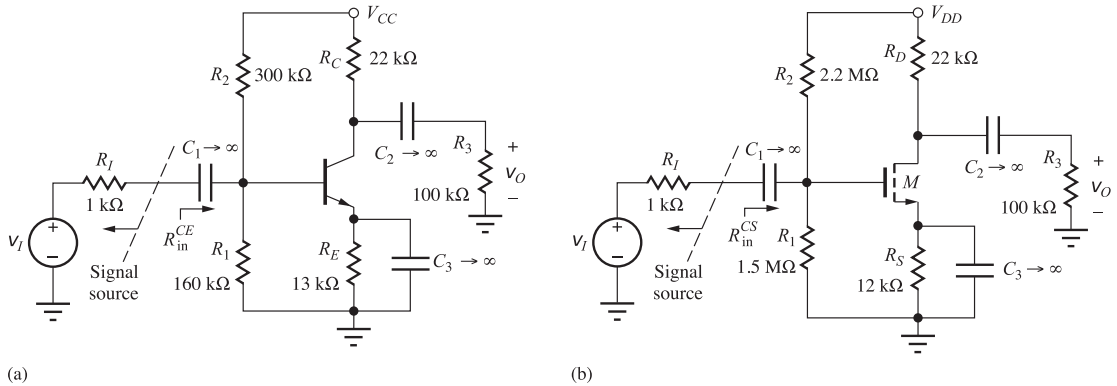
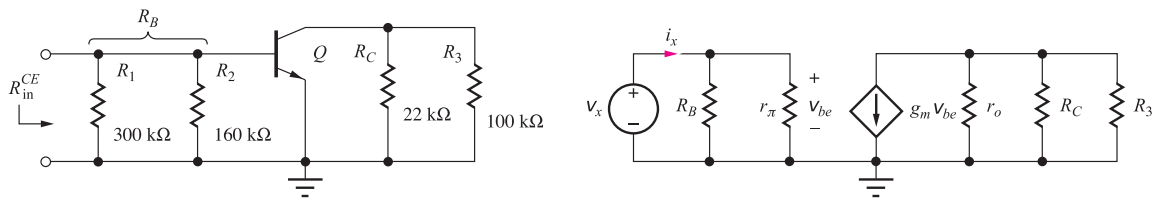


Figure13.29 (a) Input resistance def nition for the common-emitter amplif er. (b) Input resistance def nition for the common-source amplif er.



Input/Output Resistance for the Common Emitter and Source Amp

- For a common emitter for a BJT
  $v_x = i_x(R_B \,||\, r_\pi)$ and $R_{in}^{CE} = \frac{v_x}{i_x} = R_B \,||\, r_\pi = R_1 \,||\, R_2 \,||\, r_\pi$
- As $r_\pi \to \infty$ $v_x = i_x R_G$ and $R_{in}^{CS} = R_G$
- as for the output, we've $i_x = \frac{v_x}{R_C} + \frac{v_x}{r_0 + g_m v_{be}}$
- As there is no excitation at base we've $\frac{v_{be}}{R_l} + \frac{v_{be}}{R_B} + \frac{v_{be}}{r_\pi} = 0$,
  R_{out}^{CE} is defined as
  $R_{out}^{CE} = \frac{v_x}{i_x} = r_0 \,||\, R_C$ for $I_C R_C = V_{CC}/3$
  $R_{out}^{CS} = \frac{v_x}{i_x} = r_0 \,||\, R_D$ for $I_D R_D = V_{DD}/2$

Small Signal Limit

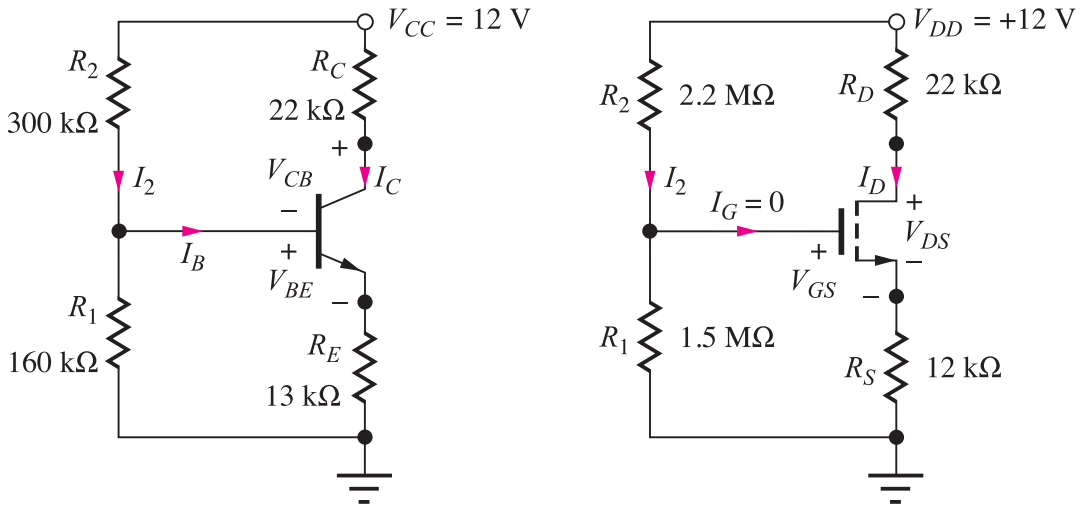
- By considering that ... $v_g = v_{gs} + g_m v_{gs} R_S = (1 + g_m R_S) v_{gs}$ $\mid v_{gs} \mid \leq 0.2(V_{GS} - V_{TN}) \rightarrow v_g 0.2(V_{GS} - V_{TN})(1 + g_m R_S)$
- The permissible input signal is increased by a factor of $(1 + g_m R_S)$ that is larger than 1
- In order to get a large gain as possible, the gain equation is $A_{vt}^{CS} = -\frac{g_m R_L}{1+g_m R_S}$, in here denominator should be as small as possible by setting almost $R_S = 0$,ergo $A_{vt}^{CS} = -g_m R_L$, $R_{iG} = \infty$, $R_{iD} = r_0$
- As for an amplifier with a large source resistance $A_{vt}^{CS} = -\frac{g_m R_L}{1+g_m R_S} \approx -\frac{R_L}{R_S}$, in here the gain is dependentless of the device

Small Signal Limit

- For an inverting amplifier in a CS configuration, R_S adds a feedback to the amp, by considering an input signal as v_g, output signal, i_d and feedback signal v_s, the close loop gain is reduced by a factor
  $1 + g_m R_S \rightarrow A = \frac{i_D}{v_{gs}} = g_m \rightarrow \beta = \frac{v_S}{i_d} = R_S$
  $A' = \frac{i_d}{v_g} = \frac{g_m v_{gs}}{v_{gs} + (g_m v_{gs}) R_S} = \frac{A}{1 + A\beta}$

Power Disipation

- Power dissipation of the amplifiers can be obtained from dc equivalent circuits. The power supplied is dissipated by the resistors and transistors

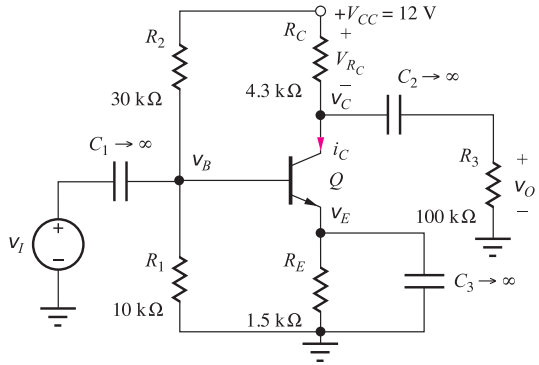


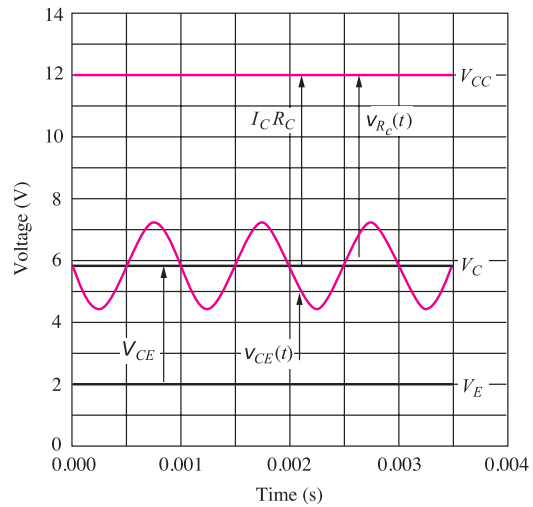
$P_D = V_{CB}I_C + V_{BE}(I_B + I_C) = (V_{CB} + V_{BE})I_C + V_{BE}I_B$ Total power supplied to the amp is: $P_S = V_{CC}(I_C + I_2)$

- Not too different for the MOSFET, the power dissipated by the transistor is $P_D = V_{DS}I_D + V_{GS}I_G = V_{DS}I_D$ and the total power supplied is: $P_S = V_{DD}(I_D + I_2)$

Signal Range

- The relationship between Q-point and the amplitude that can be developed at the output of the amplifier is analyzed





- BJT must remain in the active region at all times that needs the collector-emitter voltage remain larger than base-emitter voltage $v_{CE} \geq V_{BE}$ or $v_{CE} \geq 0.7V$ and the amplitude at collector should be $V_M \leq V_{CE} - V_{BE}$

Signal Range

- the positive power supply shows an additional skill to the swing signal $v_{R_c}(t) = I_C R_C + V_M \sin \omega t \geq 0$
- As voltage across the resistor cannot be negative or V_C at the transistor collector cannot exceed the power supply voltage V_{CC}, ergo V_M of the ac signal at the collector must be smaller than the voltage across R_C at Q-point or $V_M \leq I_C R_C$
- Signal at collector is limited by the smallest limit such as $V_M \leq min[I_C R_C.(V_{CE} - V_{BE})]$
- for a MOSFET, it is required to work on the pinch-off or v_{DS} should be larger than $v_{GS} - V_{TN}$
  $v_{DS} = V_{DS}?V_M \sin \omega t \geq V_{GS} - V_{TN}$, in here it is assumed that $v_{gs} \ll V_{GS}$, for a MOSFET, V_M has to follow the condition of $V_M \leq min[I_D R_D, (V_{DS} - (V_{GS} - V_{TN}))]$