Small-Signal Modeling and Linear Amplification

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Intro

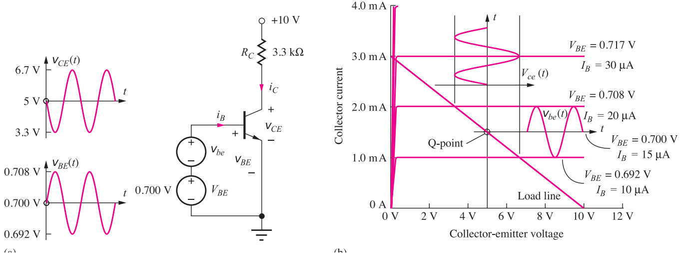
- A BJT is a not too bad amplifier when biased in the forward-active region
- FET should be operated in saturation or pinch-off region to be used as amplifiers
- We're going to refer to forward active region and FET in the saturation region as "active region" to be used as **linear amplifiers**
- among these regions, transistors can provide high-voltage, current and power gains
- In order to get the lower and upper cutoff frequencies among other sweet things, the input and output resistance need to be calculated

Intro

- To stabilize the operation point in the active region, the transistor requires to be bias
- Once stabilized, the transistor can be used as an amplifier
- Q-point controls quite a few other characteristics such as:
    1. Transistor Small signal parameters
    2. Voltage gain, input resistance and output resistance
    3. Maximum input & output signal amplitudes
    4. Power consumption

BJT as an amplifier

- If we consider that BJT is biased in the active region bu the dc applied to V_{BE}
- By considering a V_{BE}=0.7 V, it sets the Q-point as (I_C, V_{CE})=1.5 mA, 5 V as I_B=15μm



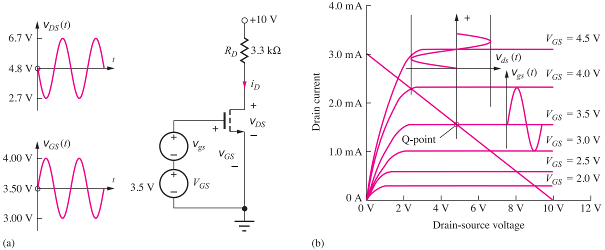
- I_B & V_{BE} are depicted as key parameters as output, although usually I_B is only shown

BJT as an amplifier

- To amplify, the input signal must be injected in a manner that causes the transistor voltages to vary
- The base-emitter voltage is forced to vary the Q-point value by signal source v_{be} placed in series with dc bias V_{BE}
- As depicted in above Fig. v_{BE}= 8 mV produces a change in i_{be}=5μm & $i_c = \beta_F i_b$
- v_{CE} on the BJT is expressed as $v_{CE} = 10 - i_C R_C = 10 - 3300 i_C$
- If the changes in operating Is & Vs are small enough "small signals", i_C and v_{CE} waveforms will be undistorted replicas of the input signals
- Small signal operation is **device dependent**

MOSFET as an amplifier

- In this configuration, v_{GS} is forced to vary the Q-point value (V_{GS}= 3.5 V) by the signal source v_{GS} in series with V_{GS}
- Resulting voltage signals at MOSFET output shown in Fig. sets the Q-point (I_D, V_{DS}) at (1.56 μm, 4.8 V) & $v_{GS} = 1V_{pp}$, causes a i_D= 1.25 mA



- $v_{DS} = 10 - 3300 i_D$

Coupling Capacitors

- Voltages v_{BE} or v_{SD} biasing techniques are not very keen methods to establish the Q-point due to the operating point is highly dependent on the transistor parameters
- To use a transistor as an amplifier, ac signals are required to be used without disturbing the Q-point established by bias network
- A key method to avoid disturbing the Q-point is to use ac coupling through capacitors
- Values for these capacitors are chosen to have negligible impedances in frequency range of interest & capacitors provide open circuits to dc so the Q-point is not disturbed
- When bias the amplifier circuit, transient currents charge the capacitors, so the final steady-state operating point is not affected

Coupling Capacitors

- As an example of how to do it is depicted by a 4-resistor net before and after capacitor coupling
- Input signal is coupled through C_1 and the signal developed at colector is coupled to R_3 by using C_2
- C_1 & C_2 are known as coupling capacitors or dc blocking capacitors. Both are considered quite large, so the reactance $(1/\omega C)\,|_\omega$ will be negligible
- C_3 is know as bypass capacitor. C_3 gives a low impedance path for ac current to "bypass" emitter R_4, that is need for Q-point stability, can be removed when ac signals are considered

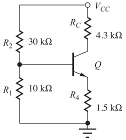


Figure 13.3 Transistor biased in the active region using the four-resistor bias network (see Sec. 5.11 for an example).

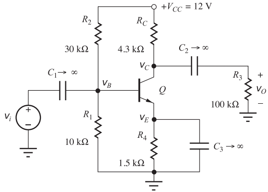
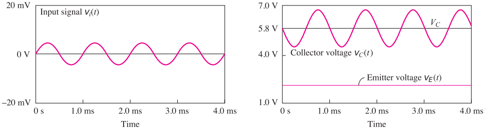


Figure 13.4 Common-emitter amplif er stage built around the four-resistor bias network. C_1 and C_2 function as coupling capacitors, and C_3 is a bypass capacitor.

Coupling Capacitors

- By performing a simualtion, a 5 mV@1kHz signal is applied to the base terminal through C_1
- It produces a signal at colector node with an amplitud of $\approx$ 1.1 V centered at V_C= 5.8 V
- There is a phase shift of π among input/output, ergo the amplifier has a gain voltage of

$$V_v = \frac{V_C}{V_i} = \frac{1.1\angle 180^\circ}{0.005\angle 0^\circ} = 220\angle 180^\circ = -220$$



- Voltage at emitter is stable as Q-point is larger that 2 V, the very low impedance of C_3 denies any voltage signal to be generated at emitter

Circuit Analysis for ac & dc Equivalent Circuits

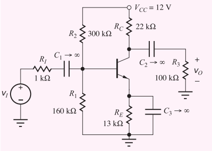
- Circuit analysis can be simply by breaking it into 2 parts: separate ac & dc analyses
- Q-point is found through the circuit using dc equivalent circuit. In here, capacitors are open and inductors are short circuits
- Once Q-point has been found, we search for the response of the circuit in ac through ac equivalent circuit
- In here, we assume that reactance os coupling capacitors in negligible at operating frequency, $\mid Z_C \mid = 1/\omega C = 0$
- Capacitor are replaced by short circuits, in a similar way, we replace inductors as $\mid Z_L \mid = \omega L \rightarrow \infty$, so inductors are open circuits
- As voltage plugged to a dc source voltage cannot change, those points are grounds in the ac equivalent circuit
- Current through a dc current source is constant even if the voltage vary, ergo, dc current sources are open circuits for the ac equivalent circuit

How to analyze for ac & dc Equivalent Circuits

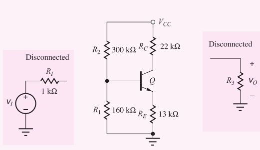
- Amplifier analysis is performed by using 2-part process
- cd Analysis
  1. Find the dc equivalent circuit and change *Cs* with open circuits and *Ls* by short circuits
  2. Find the Q-point form equivalent circuit using appropriate large-signal model for te transistor
- ac Analysis
  1. Find the ac equivalent circuit by changing *Cs* by short circuits and *Ls* by open circuits.
  2. dc sources are replaced by short circuits dc sources by open circuits in the ac equivalent circuit
  3. Replace the transistor by its small-signal model
  4. Analyze the ac characteristics by using the small.signal ac equivalent ciruit from previos step
  5. Combine results from dc and ac to obtain the total voltages and currents in the network

Exampli gratia

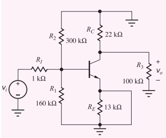
- In here we've got the main circuit



- By applying the recipe above described for dc



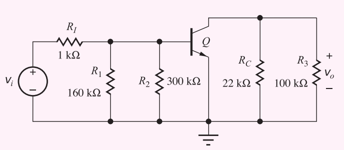
- The equivalent circuit obtained is



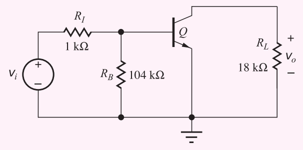
(c)

Exampli gratia

- Re-shaping the circuit we've got

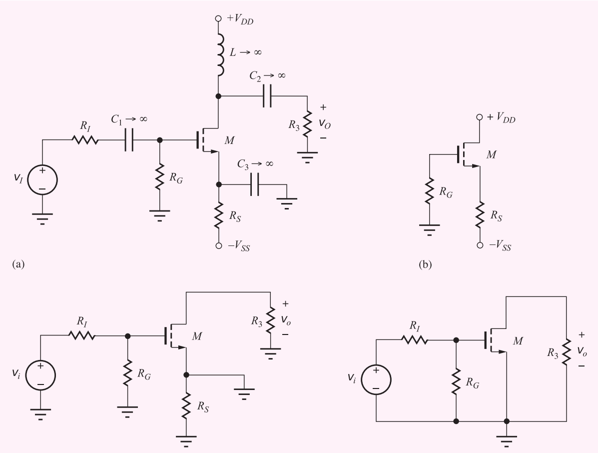


- Solving the basic circuit we obtained



Exampli gratia

- Considering a circuit with Ls and Cs

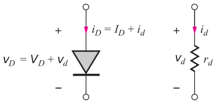


intro

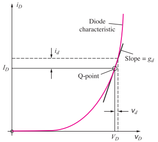
- For ac analysis, we need to use the techniques learned
- it is required that current and voltages must be small enough to ensure that circuit behaves linearly
- So, the time-varying signal components are small signals
- Amplitudes that are considered small are device-dependent
- Small-signal models start with the simplest device, diode, and continues with BJT and FET

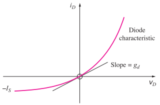
Small Signal for the Diode

- Small signal for the diode is a relationship between small current and voltage variations in the diode around Q-point values
- total terminal *Vs* and *Is* for diode can be written as $v_D = V_D + v_d$ & $i_D = I_D + i_d$, where I_D and V_D are the dc (Q) bias point values, i_d and v_d are the small changes away from the Q-point
- AS diode voltage increases a bit, a similar amount is increased the current, ergo, $i_d = v_d$ if changes are small, it can be named as diode conductance g_d or $i_d = g_d v_d$



$$r_d = \frac{1}{g_d}$$





Small Signal for the Diode

- A shown in graph above depicted, g_d represents the slope of the diode evaluated at Q-point
- It can be written as

$$g_d = \frac{\partial i_D}{\partial v_D} |_Q - point = \frac{\partial}{\partial v_D} \left\{ I_S \left[\exp\left(\frac{v_D}{V_T} \right) - 1 \right] \right\} |_Q - point$$

$$g_d = \frac{I_S}{V_T} \exp\left(\frac{v_D}{V_T} \right) = \frac{I_D + I_S}{VT}$$

- For a forward bias considering $I_D \gg I_S$, the conductance is defined as$d_d \approx \frac{I_S}{V_T}$ or $g_d \approx \frac{I_D}{25mV} = 40 I_D$
- At room temp, g_d is small but not zero for $I_D = 0$ due to the slope at the origin is not zero as portrait at above graph

Small Signal for the Diode

- Further research to define how large can be v_d and i_d before breaks down is required
- ac & dc characteristics can be obtained from the diode equation $i_D = I_S[\exp(\frac{v_D}{V_T}) - 1]$
- Substituing $v_D = V_D + v_d$ and $i_D = I_D + i_d$

$$I_D + i_d = I_S \left[\exp\left(\frac{V_D + v_d}{V_T} \right) - 1 \right] = I_S \left[\exp\left(\frac{V_D}{V_T} \right) \exp\left(\frac{v_d}{V_T} \right) - 1 \right]$$

- Expanding the second term by using Maclaurin's series and collecting all dc and signals

$$I_D + i_d = I_S \left[\exp\left(\frac{V_D}{V_T} \right) - 1 \right] + I_S \exp\left(\frac{V_D}{V_T} \right) \cdots$$

$$\cdots \left[\frac{v_d}{V_T} + \frac{1}{2} \left(\frac{v_d}{V_T} \right)^2 + \frac{1}{6} \left(\frac{v_d}{V_T} \right)^3 + \cdots \right]$$

Small Signal for the Diode

- By performing some mathematical sorcery, we've

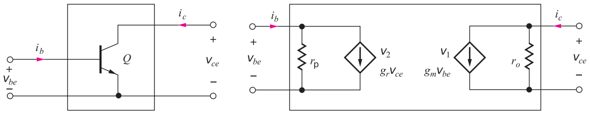
$$i_d = (I_D + I_S)\left[\frac{v_d}{V_T} + \frac{1}{2}\left(\frac{v_d}{V_T}\right)^2 + \frac{1}{6}\left(\frac{v_d}{V_T}\right)^3 + \cdots\right]$$

- As we want v_d to be linear in regard to i_d, we only consider the first term $\frac{v_d}{V_T} \gg \frac{1}{2}\left(\frac{v_d}{V_T}\right)^2$ or $v_d \ll 2V_T = 0.05V$
- Ergo $i_d = g_d v_d$ or $r_d = \frac{1}{g_d}$
- Values for diode conductance or equivalent resistance r_g are defined by the operating point defined as $g_d = \frac{I_D + I_S}{V_T} \approx \frac{I_D}{V_T} = 40 I_D$ and $r_d = \frac{1}{g_d}$

Small Signal for BJTs

- BJT is a 3-terminal device, the small-signal model i based on a 2-port network
- The input port are v_{be} and i_b & the output port variables are v_{ce} and i_c
- A set of 2-port equations as function of above variables are:

$$i_b = g_\pi v_{be} + g_r v_{ce} \qquad i_c = g_m v_{be} + g_o v_{ce}$$



Port variables can be written as time-dependent Vs and Is or as small changes in the total quantities away from the Q-point
$v_{BE} = V_{BE} + v_{be} \qquad v_{CE} = V_{CE} + v_{ce} \qquad i_B = I_B + i_b$
$i_C = I_C + i_c$

Small Signal for BJTs

- It is possible to write y-parameters as function of the small-signal Vs & Is or in terms of derivatives of the complete port variables

  $g_\pi = \frac{i_b}{V_{be}} \mid_{v_{ce}=0} = \frac{\partial i_B}{\partial v_{BE}} \mid_{Q-point}$
  $g_r = \frac{i_b}{V_{ce}} \mid_{v_{be}=0} = \frac{\partial i_C}{\partial v_{CE}} \mid_{Q-point}$
  $g_m = \frac{i_b}{V_{be}} \mid_{v_{ce}=0} = \frac{\partial i_B}{\partial v_{BE}} \mid_{Q-point}$
  $g_0 = \frac{i_b}{V_{ce}} \mid_{v_{be}=0} = \frac{\partial i_C}{\partial v_{CE}} \mid_{Q-point}$

- As previously described transport in BJT are defined as:

  $i_C = I_S \left[\exp\left(\frac{v_{BE}}{V_T}\right)\right]\left[1 + \frac{v_{CE}}{V_A}\right]$
  $i_B = \frac{i_C}{\beta_F} = \frac{I_S}{\beta_{FO}}\left[\exp\left(\frac{v_{BE}}{V_T}\right)\right]$
  $\beta_F = \beta_{FO}\left[1 + \frac{v_{CE}}{V_A}\right]$

Small Signal for BJTs

By evaluating the derivatives we've got

$g_r = \frac{\partial i_B}{\partial v_{BE}} \mid_{Q-point} = 0$

$g_m = \frac{\partial i_C}{\partial v_{CE}} \mid_{Q-point} = \frac{I_S}{V_T}\left[\exp\left(\frac{v_{BE}}{V_T}\right)\right]\left[1 + \frac{v_{CE}}{V_A}\right]_{Q-point} = \frac{I_C}{V_T}$

$g_0 = \frac{\partial i_C}{\partial v_{CE}} \mid_{Q-point} = \frac{I_S}{V_T}\left[\exp\left(\frac{V_{BE}}{V_T}\right)\right] = \frac{I_C}{V_A + V_{CE}}$

As for g_π, it requires further info such as current gain is point-dependent and it needs to be included within the analysis, ergo

$g_\pi = \frac{\partial i_B}{\partial v_{BE}} \mid_{Q-point} = \left[\frac{1}{\beta_F}\frac{\partial i_C}{\partial v_{BE}} - \frac{i_C}{\beta_F^2}\frac{\partial \beta_F}{\partial v_{BE}}\right]_{Q-point} =$
$\left[\frac{1}{\beta_F}\frac{\partial i_C}{\partial v_{BE}} - \frac{i_C}{\beta_F^2}\frac{\partial \beta_F}{\partial i_C}\frac{\partial i_C}{\partial v_{BE}}\right]_{Q-point}$

By using mathematical sorcery for the first term, we've

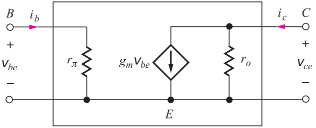
$g_\pi = \frac{1}{\beta_F}\frac{\partial i_C}{\partial v_{BE}}\left[1 - \frac{i_C}{\beta_F}\frac{\partial \beta_F}{\partial i_C}\right]_{Q-point} = \frac{I_C}{\beta_F V_T}\left[1 - \left(\frac{i_C}{\beta_F}\frac{\partial \beta_F}{\partial i_C}\right)_{Q-point}\right]$

Above equation can be simplified by adding a new parameter, because we can... β_0

$g_\pi = \frac{I_C}{\beta_0 V_T}$

where

$$\beta_0 = \frac{\beta_F}{\left[1 - I_C \left(\frac{1}{\beta_F}\frac{\partial \beta_F}{\partial i_C}\right)_{Q-point}\right]}$$



$$g_m = \frac{I_C}{V_T} \cong 40 I_C$$

$$r_\pi = \frac{\beta_o}{g_m}$$

$$r_o = \frac{V_A + V_{CE}}{I_C} \cong \frac{V_A}{I_C}$$

β_0 is the small-signal common-emitter current gain of a BJT

Hybrid π model

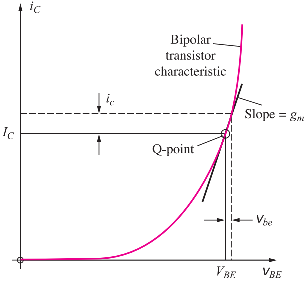
Hybrid π is the small-signal model widely accepted for a BJT. Hybrid π model is shown in above figure. The set of equations that describe such model are:

Transconductance: $g_m = \frac{I_C}{V_T} \approx 40 I_C$

Input resistance: $r_\pi = \frac{\beta_0 V_T}{I_C} = \frac{\beta_0}{g_m}$

Output resistance: $r_0 = \frac{1}{g_0} = \frac{V_A + V_{CE}}{I_C} \approx \frac{V_A}{I_C}$

The transconductance represents the slope of the $i_C - v_{BE}$ characteristics at Q-point



$$i_c = I_s \left[\exp\left(\frac{v_{BE}}{V_T} \right) - 1 \right]$$

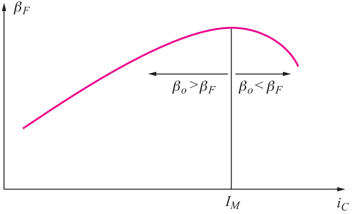
$$i_c = g_m v_{be}$$

Small-Signal Current Gain

The transconductance g_m is strongly related to r_π with the small-signal current gain β_0

$$\beta_0 = \frac{\beta_F}{\left[1 - I_C \left(\frac{1}{\beta_F}\frac{\partial \beta_F}{\partial i_C}\right)_{Q-point}\right]}$$

In practice, the key difference between β_F and β_0 is usually ignored $\beta_0 \approx \beta_F$. dc current gain β_F in a real transistor is function of the operating current



$$\beta_o = \frac{\beta_F}{\left(1 - I_C \left[\frac{1}{\beta_F}\frac{\partial \beta_F}{\partial i_C}\right]_{\text{Q-point}}\right)}$$

Intrinsic Voltage Gain for a BJT

The intrinsic voltage gain μ_F, that is related to the product of g_m and r_0

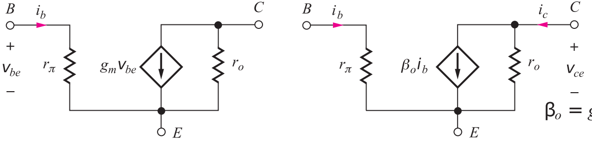
$$\mu_f = g_m r_0 = \frac{V_A + V_{VE}}{V_T} \approx \frac{V_A}{V_T}$$

when

$$V_{CS} \ll V_A$$

Equivalent Forms of Small-Signal Model

The voltage controlled current source $g_m V_{be}$, usually, it is transformed into a current controlled source.
Reorganizing v_{be} in terms of i_b as $v_{be} = i_b r_\pi$, the voltage controlled source can be written as
$g_m v_{be} = g_m r_\pi i_b = \beta_0 i_b$, where $\beta_0 = g_m r_\pi$

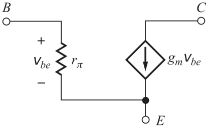


$\beta_o = g_m r_\pi$

$$i_C = \beta_0 i_b + \frac{v_{ce}}{r_0} \approx \beta_0 i_b$$

Simplified Hybrid π Model

- The output resistor r_0 has a minor effect on the performance circuit for voltage gain, so we can neglect it



- However, r_0 might have an important impact, so first we analyze the the voltage gain of the circuit and if it is lower than the intrinsic voltage gain (μ_f), r_0 is neglected and the analysis is once again performed if the result is consistent with previos assumption

Small Signal Definition for BJT

- By considering a small signal operation, it is required that $I's$ & Vs relationships be as linear as possible
- For the active working region of BJT we've found a few issues as:
  $i_C = I_S \left[\exp\left(\frac{v_{BE}}{V_T} \right) \right] = I_S \left[\exp\left(\frac{V_{BE} + v_{BE}}{V_T} \right) \right]$
- Re-shaping it as an exponential product
  $i_C = I_C + i_c = \left[I_S \exp\left(\frac{V_{BE}}{V_T} \right) \right] \left[\exp\left(\frac{v_{be}}{V_T} \right) \right] = I_C \left[\exp\left(\frac{v_{be}}{V_T} \right) \right]$
- So, the collector current is defined as: $I_C = I_S \exp\left(\frac{V_{BE}}{V_T} \right)$
- By expanding through Maclaurin's, the other section we've
  $i_C = I_C \left[1 + \frac{v_{be}}{V_T} + \frac{1}{2} \left(\frac{v_{be}}{V_T} \right)^2 + \frac{1}{6} \left(\frac{v_{be}}{V_T} \right)^3 + \cdots \right]$

Small Signal Definition for BJT

- Linearity requires that i_c needs to be proportional to v_{be}, ergo $\frac{1}{2}\left(\frac{v_{be}}{V_T}\right)^2 \ll \frac{v_{be}}{V_T}$ or $v_{be} \ll 2V_T$, it implies that input signal should be, MUST BE, lower than 50 mV@300K
- The definition for a small signal for BJT is

$$\mid v_{be} \mid \leq 0.005V$$

- If above condition is met, collector current is defined as

$$i_c \approx I_C \left[1 + \frac{v_{be}}{V_T}\right] = I_C + \frac{I_C}{V_T} v_{be} = I_C + g_m v_{be}$$

- If we consider: $i_c = i_C - I_C = I_C \frac{vve}{V_T}$, we found that

$$\frac{i_c}{I_C} = \frac{v_{be}}{V_T} \leq 0.2$$

ergo $i_c \leq 0.2 I_C$

Small Signal model for *pnp* BJT

- The model is similar as for *npn* BJT
- Current flows in opposite directions (surprise)
- Both BJT are biased by a dc current source I_B, to get the Q-point current $I_C = \beta_F I_B$, for both signal current is injected into the base for a BJT npn, we've
  $i_B = I_B + i_b$ and $i_C = I_C + i_c = \beta_F I_B + \beta_F i_b$
  and for pnp
  $i_B = I_B - i_b$ and $i_C = I_C - i_c = \beta_F I_B - \beta_F i_b$

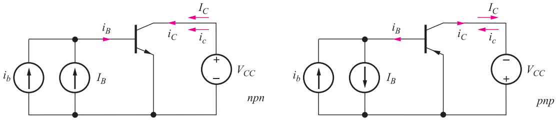
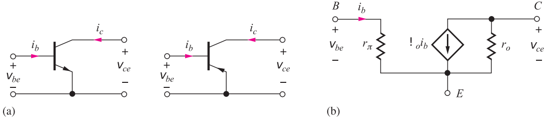
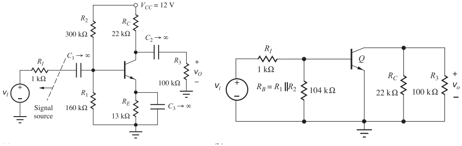


Figure 13.16 dc bias and signal currents for *npn* and *pnp* transistors.



Common-Emitter Amplifier (C-E)

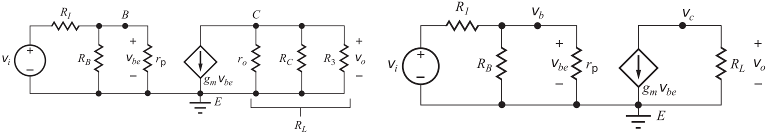
- Once analyzed, it is possible to analyze small-signal characteristics for a common-emitter amplifier as shown elsewhere
- In circuit a), it is considered that $C \to \infty$, we assume that we found the Q-point and know the values for I_C and V_{CE}
- A simplification is applied to reduce both resistors in $R_B \to R_B = R_1 \parallel R_2$



- R_3 is eliminated by the bypass capacitor

Common-Emitter Amplifier (C-E)

- Prior to develop the voltage gain of the amplifier, the transistor must be replaced by its small-signal model as shown in elsewhere
- A final simplification is related to $R_L \to R_L = r_0 \mid\mid R_C \mid\mid R_3$



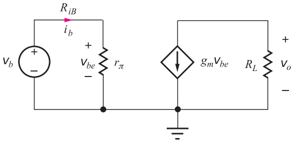
- In this configuration, signal is applied to the base, output signal appears at collector and both are referenced to the emitter terminal (common)

Terminal Voltage Gain

- Overall gain is obtained from source signal and te output voltage across resistor R_3

$$A_v^{CE} = \frac{v_o}{v_i} = \frac{v_o}{v_B} \cdot \frac{v_b}{v_i} = A_{vt}^{CE}\left(\frac{v_b}{vi}\right)$$

- By replacing it by the small.signal model, we've $v_0 = -gmR_L v_b$ or $A_{vt}^{CE} = \frac{v_o}{v_b} = -gmR_L$
- the minus symbol implies that the wave is π out of phase
- The input resistance is the relationship between the v_b and i_b
- Input resistance at the base of the BJT is equal to r_π



Signal Source Voltage Gain

- The voltage gain for a BJT (C_v^{CE}), considers the effect of the source resistance R_I that can be calculated through v_b and v_i

$$v_b = v_I \frac{R_B \mid\mid R_{iB}}{R_I + (R_B \mid\mid R_{iB})}$$

- In order to get the total gain for a common-emitter amplifier we've got

$$A_v^{CE} = A_{vt}^{CE}\left(\frac{v_b}{v_i}\right) = -g_m R_L \left[\frac{R_B \mid\mid r_\pi}{R_I + (R_B \mid\mid r_\pi)}\right]$$

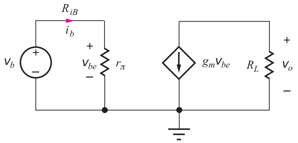
- In here A_{vt}^{CE} places an upper limit on the voltage gain as the division factor should be less than 1

Limits and other key things

- In orer to get the top limit f the configuration, we consider that the source resistance is quite small as $R_I \ll R_B \mid\mid R_{iB}$

$$A_v^{CE} \approx A_{vt}^{CE} = -gmR_L = -g_m(r_0 \mid\mid R_C \mid\mid R_3)$$

- It implies that the total signal appear at the base of the BJT, (-) imply that it is π out of phase
- It also places an upper limit and the gain that can be obtained from this configuration considering an external load resistor, it implies that the total input signal appears across r_π



Guide for the C-E Amp

- It is well known that for designers $r_0 \gg R_C$ and we need to get $R_3 \gg R_C$, ergo load resistance on the collector is R_C or

$$A_v^{CE} \approx A_{vt}^{CE} = -gmR_C = -\frac{I_C R_C}{V_T}$$

- dc voltage dropped across R_C is represented by the $I_C R_C$, by considering that $I_C R_C = \chi V_{CC}$ where $0 \leq \chi \leq 1$ and $V_T = 40V^{-1}$, we can arrange it as:

$$A_v^{CE} \approx -\frac{I_C R_C}{V_T} \approx -40\chi V_{CC}$$

- It is fairly common to consider $1/3$ of the power supply allocated at the colector resistor or $\chi = 1/3 \rightarrow I_C R_C = V_{CC}/3 \Rightarrow A_v \approx -13V_{CC}$ or

$$A_v^{CE} \approx -10V_{CC}$$

when $R_E = 0$

Small-Signal limit for the C-E Amp

- For Small-Signal Operation, the magnitud at base-emitter voltage v_{be} across r_π at small model should be less than 5 mV

$$v_i = v_{be}\left[\frac{R_I + (R_B \mid\mid r_\pi)}{R_B \mid\mid r_\pi}\right]$$

- As $\mid v_{be} \mid$ needs to be less than 5 mV, we've got

$$\mid v_{be} \mid \leq 0.005\left[1 + \frac{R_I}{R_B \mid\mid r_\pi}\right] V$$

ergo

$$v_i \leq 0.005\left[1 + \frac{R_I}{R_B \mid\mid r_\pi}\right]$$

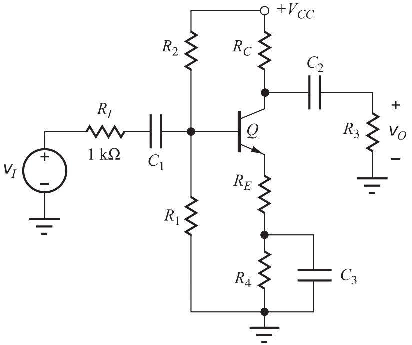
$V \approx 0.005$ for $R_B \mid\mid r_\pi \gg R_I$

Exampli Gratia

Analyze the follow Collector-Emitter Amplifier according to the follow characteristics:

$R_1 = 1\ \text{k}\Omega$ $\quad R_2 = 160\ \text{k}\Omega$ $\quad R_3 = 100\ \text{k}\Omega$ $\quad R_4 = 10\ \text{k}\Omega$

$R_C = 22\ \text{k}\Omega$ $\quad R_E = 3\ \text{k}\Omega$ $\quad V_{CC} = 12\ \text{V}$ $\quad \beta_F = 100$



To be continue $\cdots$