MOSFET: Metal-Oxide-Semiconductor Field Effect Transistor

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A milestone capacitor

- A MOS capactor induce charge at the interfase between the metal and the oxide
- Top electrode has a rather low resistivity made out of metal such as Al and it is known as gate
- A rather thin oxide (SiO_2) isolates the the gate from the substrate or body, second electrode
- The isolation produced by SiO_2 is, probably the key characteristic to use Si as the dominant material (was)
- The semiconductor region can be either n^- or p^+

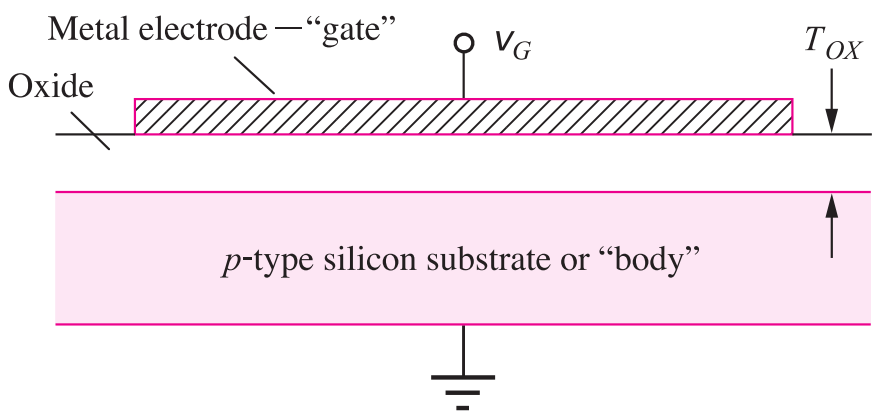
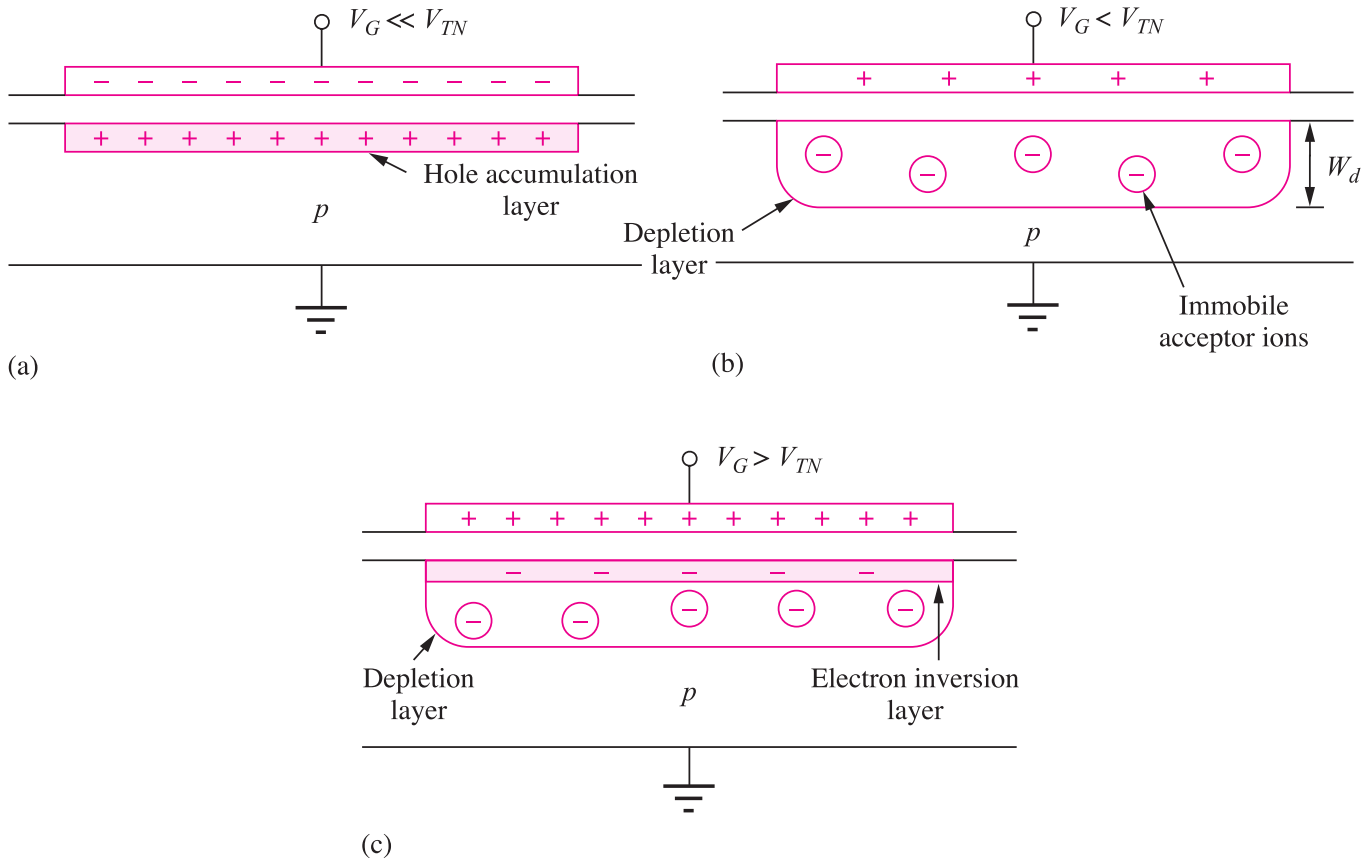


Figure 4.1 MOS capacitor structure on p-type silicon.

A milestone capacitor



Acumulation Region

- When a large negative bias is applied to the gate with respect to the substrate
- The negative charge is balanced by holes attracted to the oxide layer underneath the gate
- For such condition, the hole density at the surface surpasses the original p-type substrate
- Ergo, this operation is known as accumulation region

Depletion Region

- In here the gate is a bit increased. Holes are repeled from the surface due to electrostatics
- Density close the surface is reduced below the substrate doped level
- This condition is known as depletion
- Positive charge on the gate electrode is balanced by the negative charge of the ionized acceptor atoms
- The depletion-region width w_d can range from a fraction of a micron to tens of microns, depending on the applied voltage and substrate doping levels

Inversion Region

- By increasing the bias voltage further, e^- are attracted to the surface
- At some particular voltage, the e^- density overcome the hole density
- At this point the surface has inverted from p-type to n-type inversion layer
- The high density of electrons in the inversion layer is supplied by the electron?hole generation process within the depletion layer
- The voltage at which the surface inversion layer just forms plays an extremely important role in field-effect transistors and is called the threshold voltage V_{TN}

Summary

- At voltages well below threshold, the surface is in accumulation
- Capacitance is high and determined by the oxide thickness
- By increasing the voltage, the depletion layer is formed
- The effective separation of the capacitor plates increases, and the capacitance decreases
- Total capacitance can be modeled as the series combination of the fixed oxide capacitance C''_{ox} and the voltage dependent depletion-layer capacitance C_d
- Inversion layer forms at the surface as VG exceeds threshold voltage V_{TN}

Intro

- MOSFET is a rather simple way to create a transistor
- It is formed by two heavily doped regions through diffusions n-type
- Both diffusions provide a supply of electrons that can move under the gate and terminals

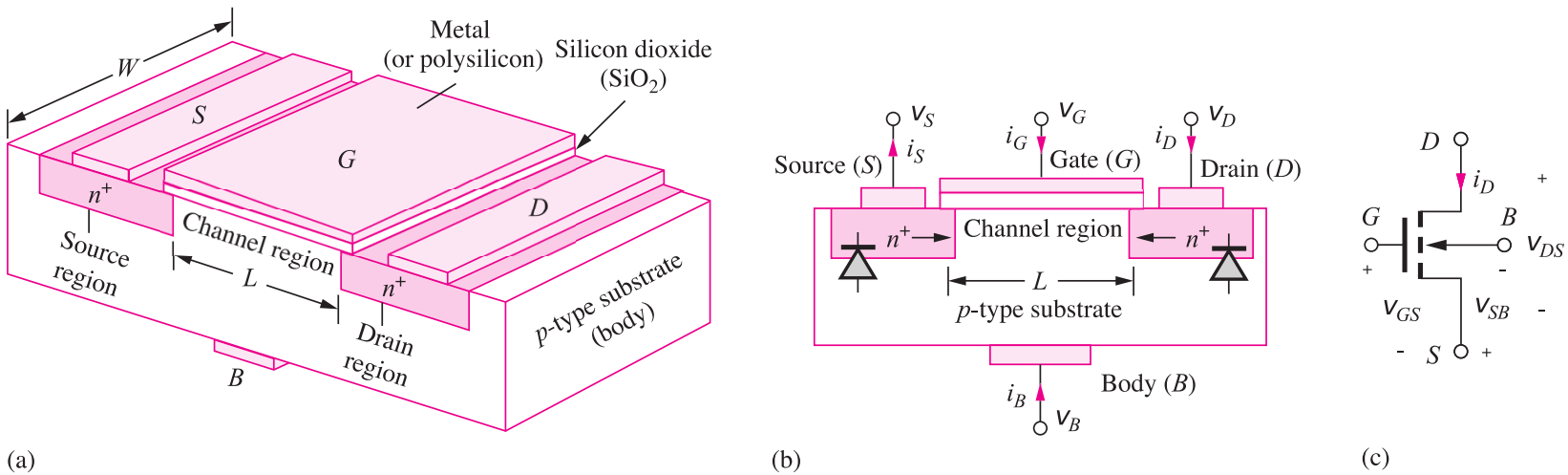


Figure 4.4 (a) NMOS transistor structure; (b) cross section; and (c) circuit symbol for the four-terminal NMOSFET.

Intro

- The central region of the NMOSFET is the MOS capacitor, top electrode of the capacitor is called the gate
- Both heavily doped regions are known as source and drain, formed in the p-type substrate
- Source and Drain supply carriers to form the inversion layer in function fo the gate voltage
- NMOS transistor is the fourth terminal or substrate terminal
- Drain current i_D, source current i_S, gate current i_G, and body current i_B are all defined, with the positive direction of each current indicated for an NMOS transistor
- The key voltages are defined as: gate-source voltage $v_{GS} = v_G - v_S$, the drain-source voltage $v_{DS} = v_D - v_S$ and the source-bulk voltage $v_{SB} = v_S - v_B$

Intro

- Semiconductor region between the source and drain regions directly below the gate is called the channel region
- L represents the channel length, which is measured in the direction of current in the channel. W is the channel width, which is measured perpendicular to the direction of current

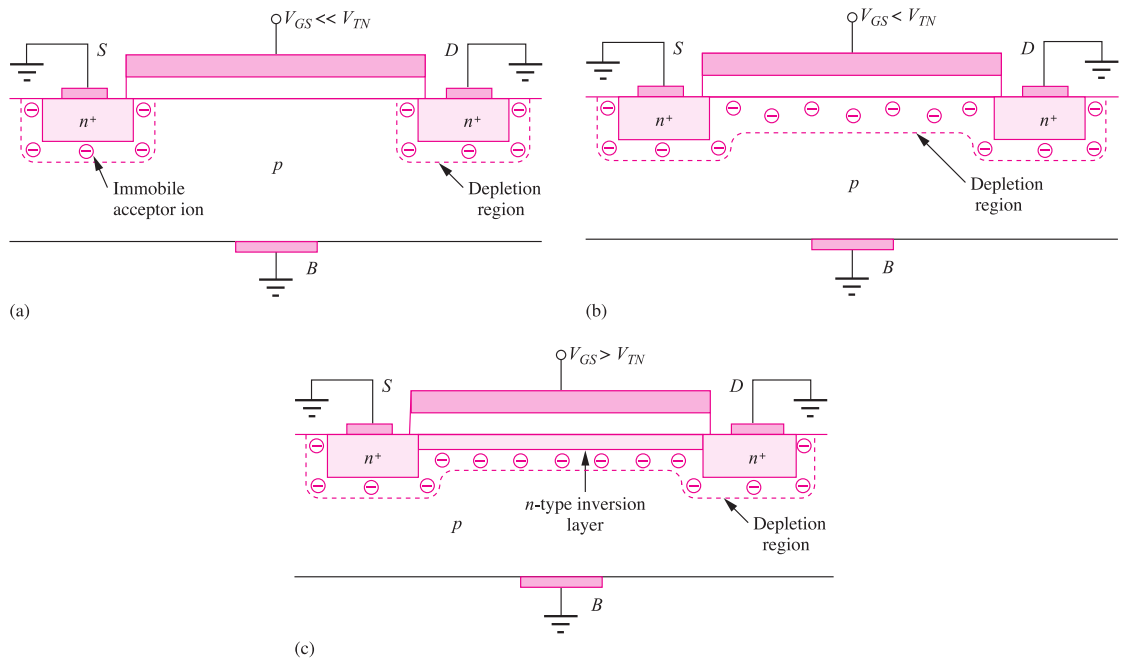


Figure 4.5 (a) V_{GS} V_{TN}. (b) $V_{GS} < V_{TN}$. (c) $V_{GS} > V_{TN}$.

Triode Region Characteristics

- If both i_G and i_B are zero, ergo, $i_S = i_D$

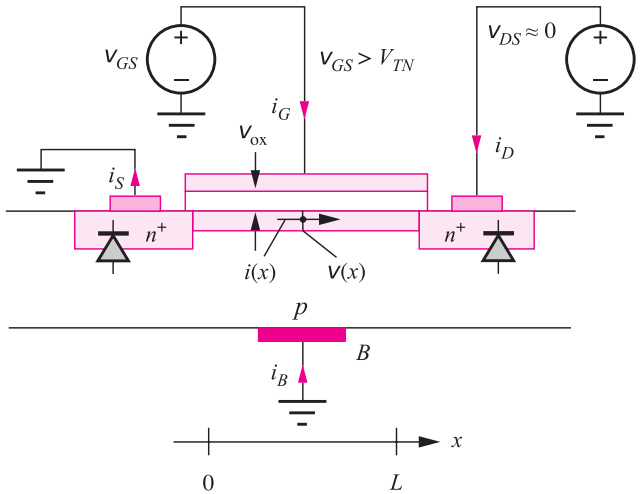


Figure 4.6 Model for determining i-v characteristics of the NMOS transistor.

- The e^- charge per length is defined as $Q' = -WC''_{ox}(V_{ox} - V_{TN})$ C/cm if $v_{ox} > V_{TN}$ where $C'' = \epsilon_{ox}/T_{ox}$, the oxide capacitance per unit area (F/cm^2) ϵ_{ox} = oxide permittivity (F/cm) T_{ox} = oxide thickness (cm) For silicon dioxide, $\epsilon_{ox} = 3.9\epsilon_0$, where $\epsilon_{ox} = 8.854 \times 10^{-14}$ F/cm.

Triode Region Characteristics

- The voltage v_{ox} represents the voltage across the oxide: $v_{ox} = v_{GS} - v(x)$
- The electron drift current at any point in the channel is given by $i(x) = Q'(x)v_x(x)$
- Electrons in the channel is determined by the electron mobility and the transverse electric field in the channel $i(x) = Q'v_x = [-WC''_{ox}(v_{ox} - V_{TN})](-\mu_n E_x)$
- As there is no mechanism to lose current as it goes to the channel, $i(x) = i_D$,

$$i_D = \mu_n C''_{ox} \frac{W}{L} \left(v_{GS} - V_{TN} - \frac{v_{DS}}{2} \right) v_{DS}$$

- The value of $\mu_n C''_{ox}$ is fixed for a given technology and cannot be changed by the circuit designer

Triode Region Characteristics

- $$i_D = K_n' \frac{W}{L} \left(v_{GS} - V_{TN} - \frac{v_{DS}}{2} \right) v_{DS}$$

  or

- $$i_D = K_n \left(v_{GS} - V_{TN} - \frac{v_{DS}}{2} \right) v_{DS}$$

- where $K_n = K_n' W/L$ & $K_n' = \mu_n C_{ox}''$
- K_n and K_n' are the transconductance parameters
- Above equation represents the classic expression for the drain-source current for the NMOS transistor in its linear region or triode region
- A resistive channel directly connects the source and drain

Triode Region Characteristics

- This resistive connection will exist as long as the voltage across the oxide exceeds the threshold voltage at every point in the channel $v_{GS} - v_{DS} \geq V_{TN}$ for $0 \leq x \leq L$
- Voltage in the channel is maximum at the drain end where $v(L) = v_{DS}$
- for triode region,

$$K_n^{'} \frac{W}{L} \left(v_{GS} - V_{TN} - \frac{v_{DS}}{2} \right) v_{DS}$$

  for $v_{GS} - V_{TN} \geq v \geq 0$ and $K_n^{'} = \mu_n C_{ox}^{''}$
- Quiescent operating point or Q-point of the FET is given by (I_D, V_{DS})

Triode Region: Resistance

- Triode i-v characteristics defined by i_D, $K_n^{'}$ and v_D are shown, according to V_{TN} =1V and $K_n = 250\mu A/V^2$
- Output characteristics for the MOSFET are drain current i_D curves as a function of v_{DS}, this is why ti's called linear region

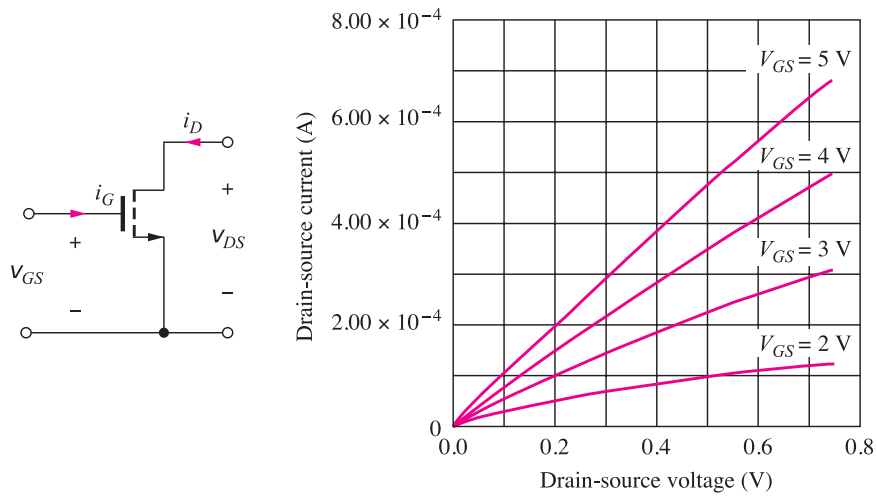


Figure 4.7 NMOS i-v characteristics in the triode region ($V_{SB} = 0$). A three-terminal NMOS circuit symbol is often used when $v_{SB} = 0$.

Triode Region: Resistance

- For a rather small bias such as for V_{GS}=2 V, the condition $v_{DS}/2 \leq v_{GS} - V_{TN}$, produces that $i_D \approx \mu C''_{ox} \frac{W}{L}(v_{GS} - V_{TN})v_{DS}$
- It shows that i_D through the MOSFET is proportional to v_{DS}
- The MOSFET behavior is similar to a resistor connected between drain and source
- The resistor value can be "controlled" by a gate -source voltage
- This behavior originated the name "transfer-resistor" or transistor
- FET resistor at triode region is called on-resistance R_{on}

$$R_{on} = \left[\frac{\partial i_D}{\partial v_{DS}} \Big|_{v_{DS} \to 0} \right]^{-1}_{Q-pt} = \frac{1}{K'_n \frac{W}{L}(V_{GS} - V_{TN})}$$

Also, consider that $R_{on} = v_{DS}/i_D$

Triode Region: Saturation

- General eq. for i_D is valid as far as is resistive channel "directly" connects both source and drain
- When the i_D increases further the triode region, it doesn't continue increase but saturates
- This behavior is depicted in $i - v$ curves for several v_{GS}

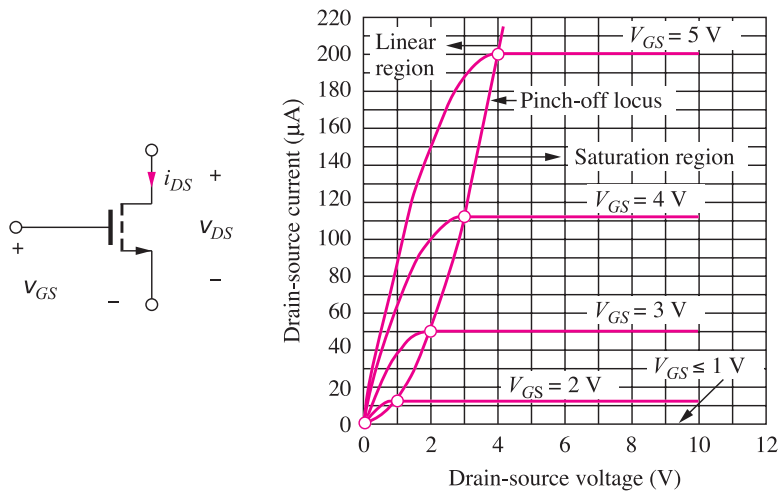
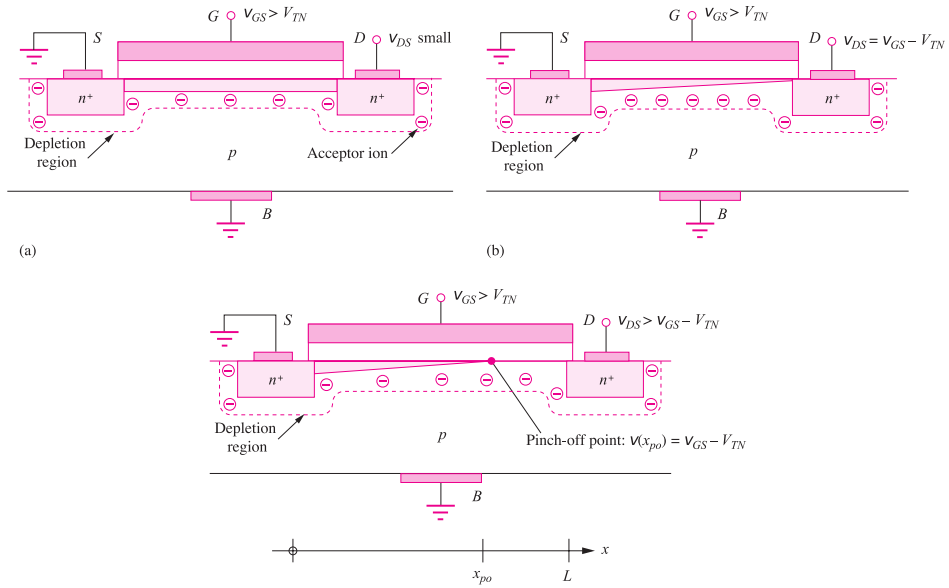


Figure 4.8 Output characteristics for an NMOS transistor with $V_{TN} = 1$ V and $K_n = 25 \times 10^{-6}$ A/V^2($v_{SB} = 0$). A three-terminal NMOS circuit symbol is used when $v_{SB} = 0$.

Triode Region: Saturation



- Saturation come across to analyze the above figure by paying attention to the drain voltage value
- When operating at triode region $v_{DS} < v_{GS} - VTN$, by increasing it to $v_{DS} = v_{GS} - VTN$ the channel disappear at drain, by increasing further $v_{DS} > v_{GS} - VTN$, channel shrinckes and disappear
- As the channel has disappeared or pinched off, source and drain terminals are in no contact

Triode Region: Saturation

- As there is no channel "apparently" there should be no current but it is
- Voltage at pinch-off point in the channel is $v(x_{po}) = v_{GS} - V_{TN}$
- As there is a voltage on the channel $v_{GS} - V_{TN}$, e^- can drift into the channel
- When e^- reach the pinch off point, those are injected into the SCR at the end of the channel and drain
- The $\vec{E}$ sweeps the e^- on to the drain
- When the channel reaches the pinch off point, voltage drops across the inverted channel is constant as a consequence, i_D becomes constant and independent of v_{DS}

Transconductance

- A key characteristic of the transistor i the transconductance (g_m)
- The change between i_D and v_{GS} is the transconductnace

$$g_m = \frac{di_D}{dv_{GS}} \mid_{Q-pt} = \frac{2I_D}{V_{GS} - V_{TN}}$$

- g_m is key for electronics, the larger the device transconductance, the more gain we can expect from the amplifier that uses the transistor

Channel Length Modulation

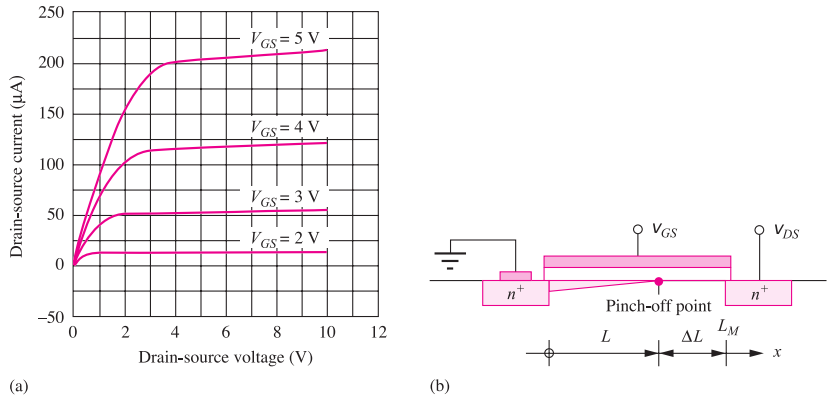


Figure 4.11 (a) Output characteristics including the effects of channel-length modulation. (b) Channel-length modulation.

- Output characteristics shows that i_D is constant once the device enters saturation but it is not
- $i - v$ curves have a small positive slope
- i_D increases as v_{DS} also increases
- i_D increase is a phenomenon called channel-length modulation
- By adding an inverse dependence of v_{DS} once in saturation, we've $i_D = \frac{K_n'}{2}\frac{W}{L}(v_{GS} - V_{TN})^2(1 + \lambda v_{DS})$
- where λ is the channel length modulation parameter. Those are the typicall values for it $0V{-}1 \leq \lambda \leq 0.2V^{-1}$

Depletion mode MOSFETS

- It is possible to fabricate transistor with $V_{TN} \leq 0$
- These are known as depletion-mode transistors
- A nonzero current is possible for v_{GS}, a negative v_{GS} is required to turn the device off
- A process called ion implantation is used to form a built-in n-type channel in the device so source and drain are connected through the resistive channel region
- A $-v_G$ is required to to deplete the n-type channel region and cut the i_{SD}

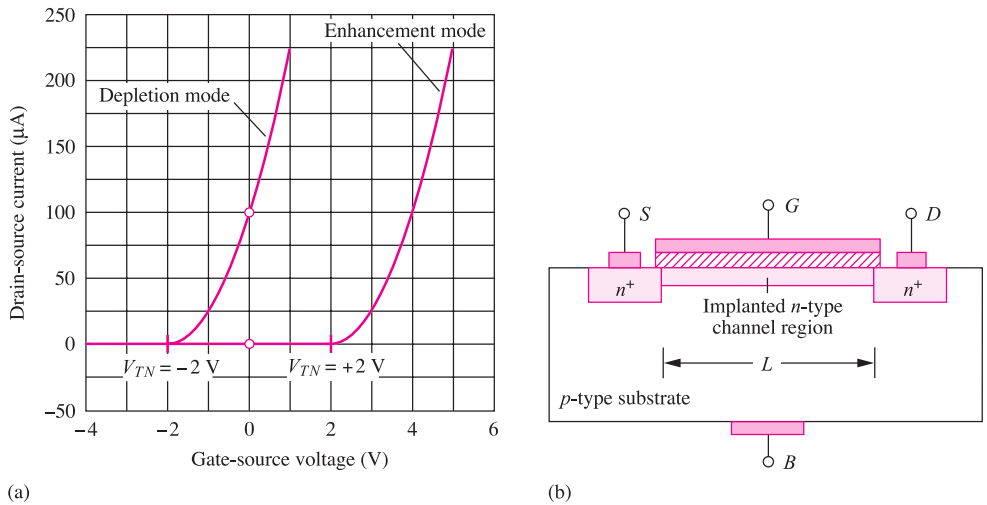
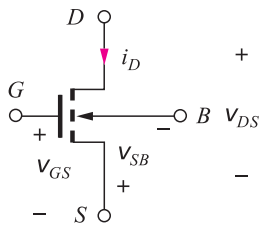


Figure 4.12 (a) Transfer characteristics for enhancement-mode and depletion-mode NMOS transistors. (b) Cross section of a depletion-mode NMOS transistor.

NMOS Mathematical Model Summary



NMOS transistor

NMOS TRANSISTOR MATHEMATICAL MODEL SUMMARY

Equations (4.24) through (4.28) represent the complete model for the i-v behavior of the NMOS transistor.

For all regions,

$$K_n = K_n' \frac{W}{L} \qquad K_n' = \mu_n C_{ox}'' \qquad i_G = 0 \qquad i_B = 0 \tag{4.24}$$

Cutoff region:

$$i_D = 0 \qquad \text{for } v_{GS} \le V_{TN} \tag{4.25}$$

Triode region:

$$i_D = K_n \left[v_{GS} - V_{TN} - \frac{v_{DS}}{2} \right] v_{DS} \qquad \text{for } v_{GS} - V_{TN} \ge v_{DS} \ge 0 \tag{4.26}$$

Saturation region:

$$i_D = \frac{K_n}{2}(v_{GS} - V_{TN})^2(1 + \lambda v_{DS}) \qquad \text{for } v_{DS} \ge (v_{GS} - V_{TN}) \ge 0 \tag{4.27}$$

Threshold voltage:

$$V_{TN} = V_{TO} + \gamma \left(\sqrt{v_{SB} + 2\phi_F} - \sqrt{2\phi_F} \right) \tag{4.28}$$

$V_{TN} > 0$ for enhancement-mode NMOS transistors. Depletion-mode NMOS devices can also be fabricated, and $V_{TN} \le 0$ for these transistors.

P-MOS Transistor

- MOS Transistor with p-channel can also be fabricated
- Behavior for a PMOS is similar as for a NMOS but normal currents and voltages polarities are reversed
- A negative voltage at gate relative to the source is needed ($V_{GS} < 0$) to attract h^+ and create a p-type inversion layer in the channel region
- v_{GS} should be more negative than V_{TP}. In order to keep junctions source-substrate and drain-substrate, v_{SB} and v_{DB} must be less than zero
- It works if $v_{DS} \leq 0$

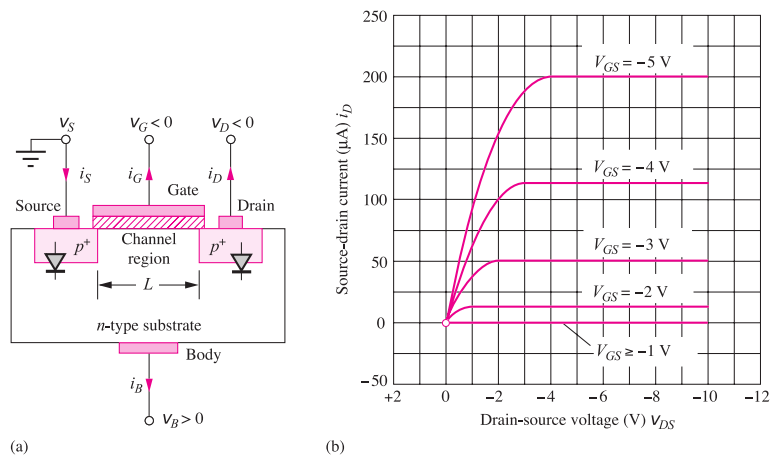
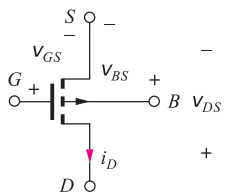


Figure 4.14 (a) Cross section of an enhancement-mode PMOS transistor. (b) Output characteristics for a PMOS transistor with $V_{TP} = -1$ V.

PMOS Mathematical Model Summary



PMOS transistor

PMOS TRANSISTOR MATHEMATICAL MODEL SUMMARY

Equations (4.29) through (4.33) represent the complete model for the i-v behavior of the PMOS transistor.

For all regions,

$$K_p = K_p' \frac{W}{L} \qquad K_p' = \mu_p C_{ox}'' \qquad i_G = 0 \qquad i_B = 0 \tag{4.29}$$

Cutoff region:

$$i_D = 0 \qquad \text{for } V_{GS} \geq V_{TP} \tag{4.30}$$

Triode region:

$$i_D = K_p \left[v_{GS} - V_{TP} - \frac{v_{DS}}{2} \right] v_{DS} \qquad \text{for } 0 \leq |v_{DS}| \leq |v_{GS} - V_{TP}| \tag{4.31}$$

Saturation region:

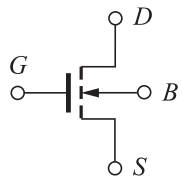
$$i_D = \frac{K_p}{2}(v_{GS} - V_{TP})^2(1 + \lambda |v_{DS}|) \qquad \text{for } |v_{DS}| \geq |v_{GS} - V_{TP}| \geq 0 \tag{4.32}$$

Threshold voltage:

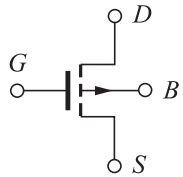
$$V_{TP} = V_{TO} - \gamma \left(\sqrt{v_{BS} + 2\phi_F} - \sqrt{2\phi_F} \right) \tag{4.33}$$

For the enhancement-mode PMOS transistor, $V_{TP} < 0$. Depletion-mode PMOS devices can also be fabricated; $V_{TP} \geq 0$ for these devices.

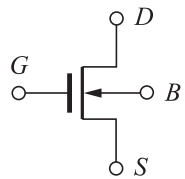
MOS Transistor Circuit Models



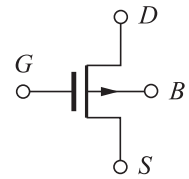
(a) NMOS enhancement-mode device



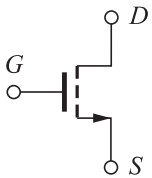
(b) PMOS enhancement-mode device

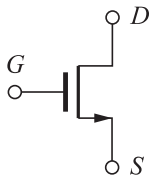


(c) NMOS depletion-mode device

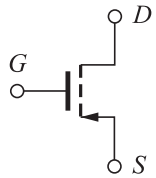


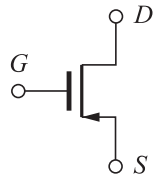
(d) PMOS depletion-mode device



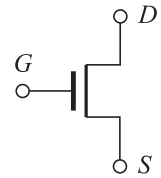


(e) Three-terminal NMOS transistors

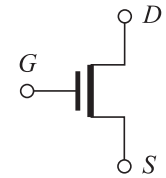




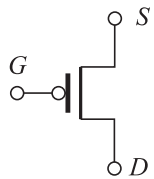
(f) Three-terminal PMOS transistors



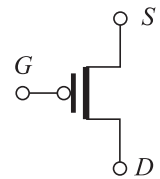
(g) Shorthand notation—NMOS enhancement-mode device



(h) Shorthand notation—NMOS depletion-mode device



(i) Shorthand notation—PMOS enhancement-mode device

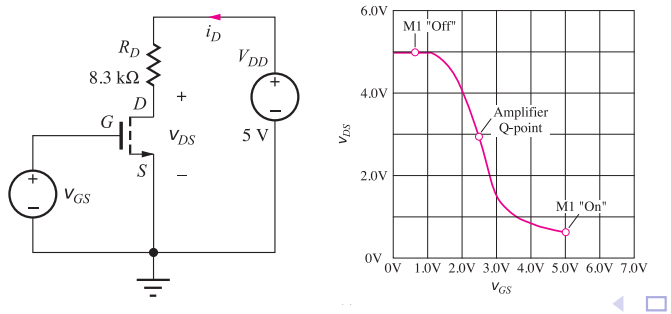


(j) Shorthand notation—PMOS depletion-mode device

Figure 4.15 (a)–(f) IEEE Standard MOS transistor circuit symbols. (g)–(j) Other commonly used symbols.

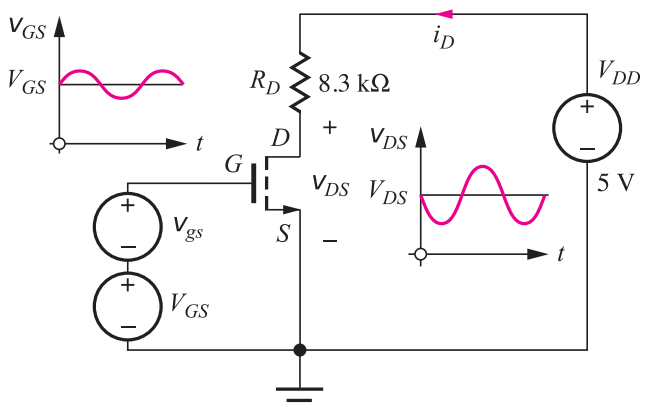
Biasing the NMOS Transistor

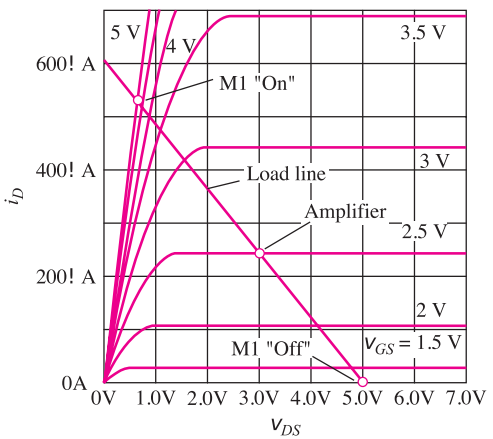
- MOSFET has 3 operation regions: cutoff, triode and saturation
- For proper operation, it is needed to get the Q-point, it is represented by dc values (I_D, V_{DS})
- We need 3 points or 2 and the other can be calculated as such
- For binary circuits, transistor acts as on-off switch, Q-point is set to be either the cut-off region (off) or triode region (on)
- For low v_{GS}, MOSFET is off and the output voltage is 5V or "1", by increasing v_{GS}, output drops and and it is turn-on v= 0.65 V when $v_{GS} = 5V$ that is a "0"
- When MOSFET is on, it drives a large amount of current and v_{DS} reaches 0.65 V. In contrast, whent transistor is off, $v_{DS} = 5$V



Biasing the NMOS Transistor 2

- To amplify, Q-point is located at high-slope quite close to the center of the voltage transfer
- At this point the transistor is operating at saturation, in here voltage, current or power gain can be obtained
- To get a Q-point, a dc bias V_{GS} is applied to the gate and a small ac signal v_{gs} is added to vary the gate voltage around the bias point
- Variation in v_{GS} changes i_D & and amplified replica of ac appears at drain



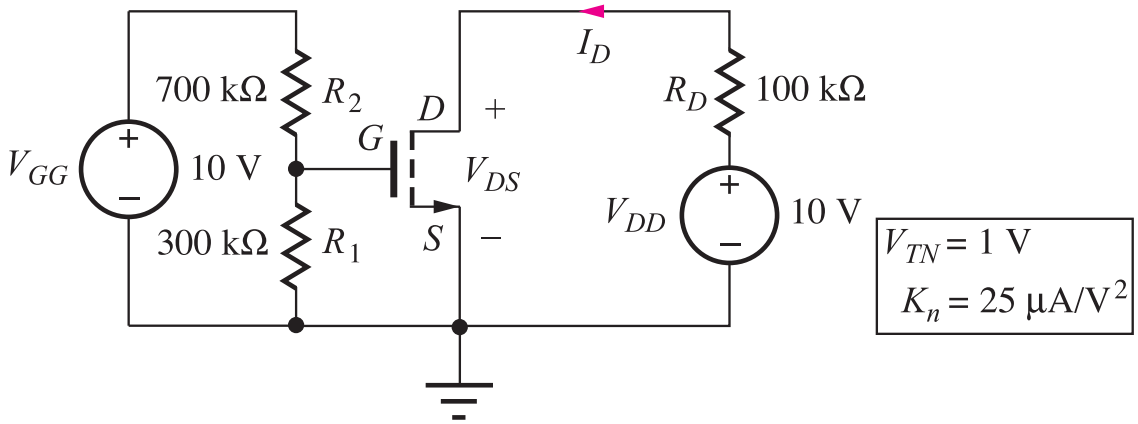


Biasing the NMOS Transistor 2

- The dc load line plots the permissible values of ID and VDS as determined by the external circuit
- Load line equation is given by $V_{DD} = I_D R_D + V_{DS}$
- A few characteristics must met to bias such as: Assume the operation region (saturation), find V_{GS}, check validity, change assumptions and analyze if required
- For Pinch-off $V_{DS} \geq V_{GS} - V_{TN}$, but is $V_{DS} = V_{GS}$ $V_{DS} \geq V_{GS} - V_{TN}$ or $V_{TN} \geq 0$
- Above asumption is valid if $v_{TN} > 0$, it corresponds to an NMOS enhancement mode device
- An enhanced mode device operating at $V_{DS} = V_{GS}$ is always in saturation region. similar arguments are valid for PMOS devices

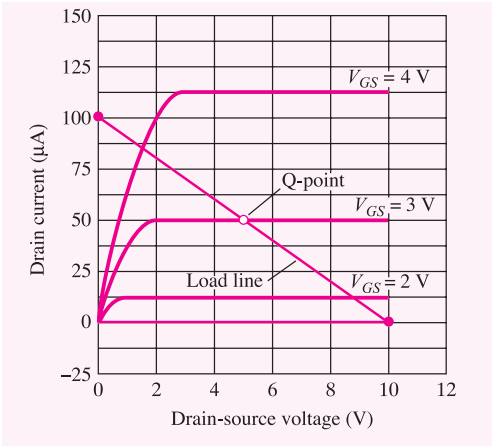
Examples ...

Find the Q-point for a MOSFET... Neglect the channel length modulation and find it if λ=0.02/V



Examples ... 2

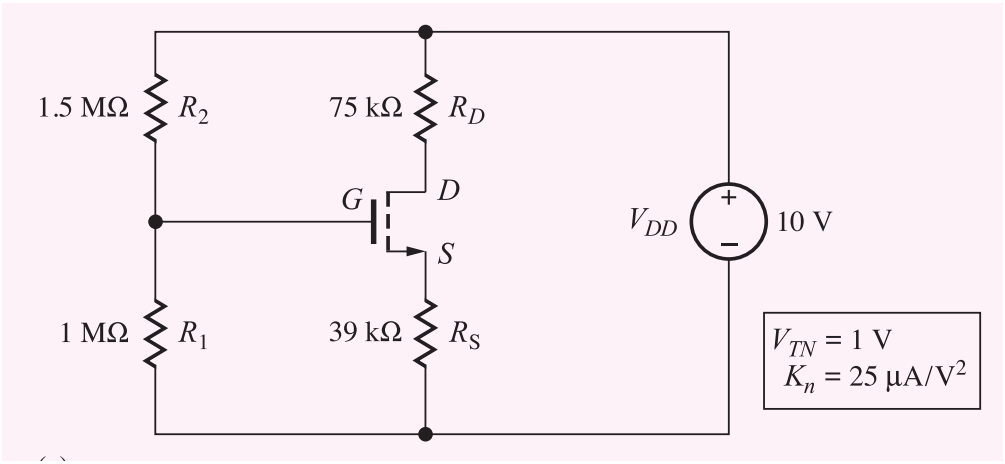
Use the load line analysis (rubbish most of the time), to locate the Q-point for the MOSFET. For the above figure, the line come from: $10 = 100 i_D + v_{DS}$



The NMOS curves cross the load line at several points, v_{GS} determine the intersection point at which the Q-point is. In here, v_{GS}=3 V, Q-point is shown in Fig. that shows v_{DS}= 5 V and $i_D = 50\mu$A

Four Bias Resistor

- The array provides a fixed gate-source bias voltage to the transistor
- A key drawback is that in practice the values of K_n, V_{TN} and λ for the MOSFET will not be known with high precision and the Q-point is not well-controlled
- It is required to consider resistor and power tolerances, drift values for time and temp
- 4-resistor bias provides a well stabilized Q-point



Find the Q-point in the circuit

For an enhancement-mode MOSFET that is operating with $v_{DS} = v_{GS}$, always will be at pinch-off