Single Transistor Amplifier

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Amplification

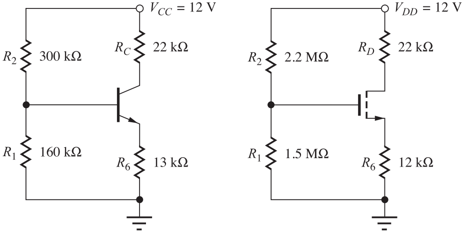
Transistor as an amplifier

Intro

- Previously, we applied the input signal either to the base or gate and the output was taken from collector or drain
- By considering that both transistors have 3-terminals, we can "only" use collector & emitter or drain & source to get the signal
- As before, we're going to use the same 4-resistor configuration, coupling and by-pass capacitors are also used to modify the signal input/output as well as the ac characteristics

Input/Output signals at BJT

- Large signal model for BJT allow us to know where the input signal for a forward bias BJT is



$$i_C = I_S \left[\exp\left(\frac{v_{BE}}{V_T}\right)\right] \quad i_B = \frac{i_C}{\beta_F} = \frac{I_S}{\beta_F}\left[\exp\left(\frac{v_{BE}}{V_T}\right)\right]$$

$$i_E = \frac{I_S}{\alpha_F}\left[\exp\left(\frac{v_{BE}}{V_T}\right)\right]$$

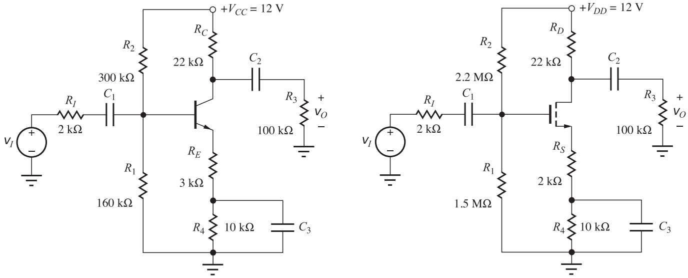
- To increase 'Is' quite a bit, we also need to increase v_{BE} as $v_{BE} = v_B - v_E$
- A signal needs to be added to base or emitter, collector has no effect whatsoever in terminal currents

Input/Output signals at BJT

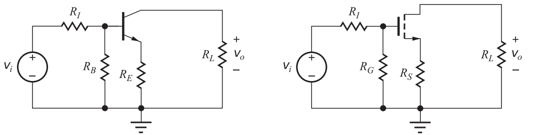
- By increasing I_C & I_E create larger voltages across R_C and R_6
- As i_B is a β factor smaller than i_C or i_E, base is no used for output signal
- As for the FET, $i_S = i_D = \frac{K_n}{2}(v_{GS} - V_{TN})^2$ and $i_G = 0$
- To vary significantly Is, v_{GS} need to change as $v_{GS} = v_G - v_S$
- Input signal can be injected though gate or source at FET
- By varying drain voltage, has a minor effect on terminal currents ($\lambda \neq 0$), ergo drain is not appropriate for signal injection
- On the other hand, gate terminal is not used as output terminal due to $i_G = 0$
- There are 3-main families of amplifiers: Common-Emitter/Common-Source (C-E/C-S), Common-Base/Common-Gate (C-B/C-G) and Common-Collector/Common-Drain (C-C/C-D)

Common-Emitter/Common-Source (C-E/C-S)

- In those diagramas R_6 has been divided between R_4 and C_2



(a) (b)

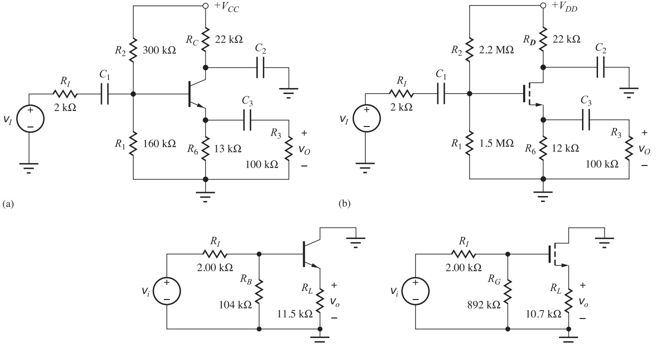


(c) $R_B = R_1 \| R_2$ $R_2 = R_C \| R_3$

(d) $R_G = R_1 \| R_2$ $R_L = R_O \| R_3$

Common-Collector/Common-Drain (C-C/C-D)

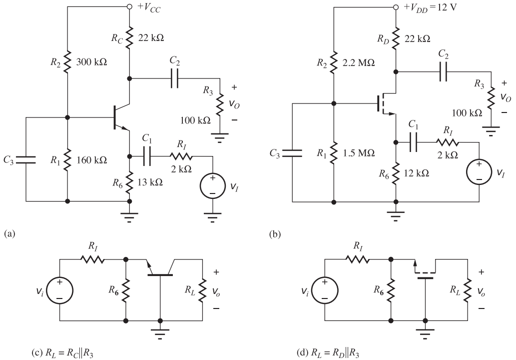
- In here signals are injected into the base/gate and the output is in emitter or source
- Collector/drain are bypassed by C_2
- C-C & C-D amplifiers pride a voltage gain =1, moreover, input signals can be fairly large without exceeding the small-signal limits



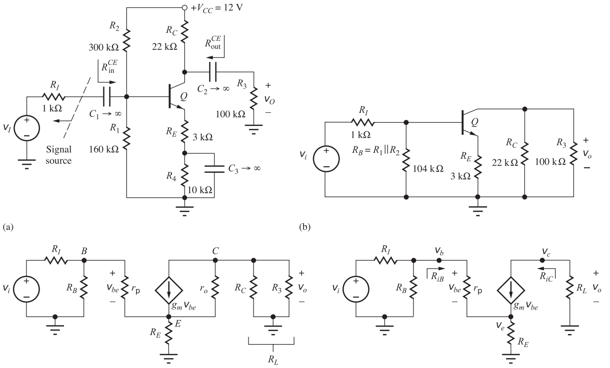
(c) $R_B = R_1 \| R_2 \quad R_L = R_6 \| R_3$ (d) $R_G = R_1 \| R_2 \quad R_L = R_6 \| R_3$

Common-Base/Common-Gate (C-B/C-G)

- *ac* signals are injected into the emitter/source and extracted from the collector/drain
- Base/gate terminals are bypassed by C_2, those are common connections between input/output ports
- It shows a voltage gain at much lower input resistance

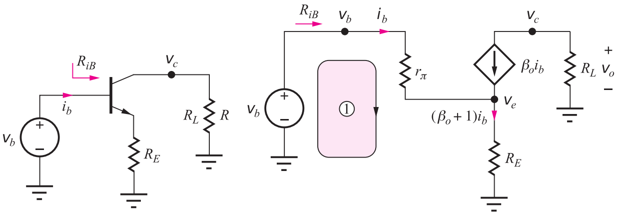


Common-Emitter Amplifier



- We consider that we found Q-point and values for I_C and V_{CE} and $R_B = R_1 \,||\, R_2$, R_4 is eliminated due to C_3 and $R_L = R_C \,||\, R_3$
- NOTE: r_0 is removed due to we already know ;)

Common-Emitter Amplifier



- Terminal voltage gain is defined as $A_v^{CE} = \frac{v_0}{vi} = \left(\frac{v_0}{v_b}\right)\left(\frac{v_b}{v_i}\right) = A_v^{CE}\left(\frac{v_b}{v_1}\right)$ where $A_{vt}^{CE} = \left(\frac{v_c}{v_b}\right)$
- as $v_c = -\beta_0 i_b R_L$, we've got that

$$A_{vt}^{CE} = \frac{v_c}{V_b} = -\frac{\beta_0 R_L}{r_\pi + (\beta_0 + 1)R_E} \approx -\frac{g_m R_L}{1 + g_m R_E}$$

where $\beta_0 \gg 1$ and $\beta_0 = g_m r_\pi$

Common-Emitter Amplifier

- The input resistance is defined as

$$R_{iB} = \frac{v_b}{i_b} = r_\pi + (\beta_0 + 1)R_E \approx r_\pi(1 + g_m R_E)$$

- The overall input resistance $R_{in}^{CE} = R_B \mid\mid R_{iB}$
- The voltage gain of the amplifier, that includes the source resistance, the v_b at the BJT is

$$v_b = v_i \frac{R_B \mid\mid R_{iB}}{R_I + (R_B \mid\mid R_{iB})}$$

- As a result of the above equations, the total voltage gain is defined as

$$A_v^{CE} = A_v^{CE}\left(\frac{v_b}{v_i}\right) = -\left(\frac{g_m R_L}{1 + g_m R_E}\right)\left[\frac{R_B \mid\mid R_{iB}}{R_I + (R_B \mid\mid R_{iB})}\right]$$

Common-Emitter Amplifier

- If we consider that the source resistance is small $R_I \ll R_B \mid\mid R_{iB}$, we've $A_v^{CE} = A_{vt}^{CE} = -\frac{g_m R_L}{1+g_m R_E}$
- In order to get a large signal as possible we consider a zero resistance at emitter $R_E = 0$ $A_v^{CE} \approx -g_m R_L = -g_m(R_C \mid\mid R_3)$ and $A_v^{CE} \approx -10V_{CC}$
- To amplify the condition for voltage at emitter is: $v_e = (\beta_0 + 1)i_b R_E = \frac{(\beta_0+1)R_E}{r_\pi+(\beta_0+1)R_E} v_b \approx \frac{g_m R_E}{1+g_m R_E} v_b \approx v_b$
- As for current $i_E \approx \frac{v_b}{R_E}$, $v_0 = -i_c R_L = -\alpha_0 i_e R_L \approx -i_e R_L$, ergo $A_{vt}^{CE} = -\frac{g_m R_L}{1+g_m R_E} \approx -\frac{R_L}{R_E}$

Common-Emitter Amplifier

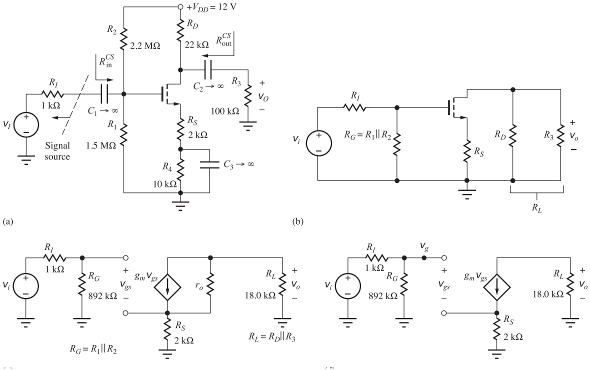
- Resistance at the BJT collector R_{iC} is defined by $R_{th} = R_B \mid\mid R_I$, ergo $R_{iC} = r_0 \left(1 + \frac{\beta_0 R_E}{R_{th}+r_\pi+R_E}\right) + (R_{th} + r\pi) \mid\mid R_E \approx r_0 \left(1 + \frac{\beta_0 R_E}{R_{th}+r_\pi+R_E}\right)$ by having a few considerations we've got

$$R_{iC} \approx r_0[1 + g_m(R_E \mid\mid r_\pi)] = r_0 + \mu_f(R_E \mid\mid r_\pi)$$

- The output resistance is defined as

$$R_{out}^{CE} = R_C \mid\mid R_{iC} = R_C \mid\mid r_0 \left(1 + \frac{\beta_0 R_E}{R_{th} + r\pi + R_E}\right)$$

Common-Source Amplifier



- In a similar way as for the previous configuration we've got that the source voltage gain is $A_{vt}^{CS} = -\frac{g_m R_L}{1+g_m R_S}$
- The Common-Source voltage gain general expression is defined as $A_v^{CS} = -\frac{g_m R_L}{1+g_m R_S}\left(\frac{R_G}{R_G+R_I}\right)$

Common-Source Amplifier

- Gain for large R_S $A_{vt}^{CS} = -\frac{g_m R_L}{1+g_m R_S} \approx -\frac{R_L}{R_S}$
- When there is a low resistance at source $A_v^C \approx -g_m R_L = -g_m(R_D \parallel R_3)$
- The common-source output resistance is defined as $R_{out}^{CS} = R_D \parallel R_{iD} = R_D \parallel r_0(1 + g_m R_S) \approx R_D$

Common-Collector Amplifier

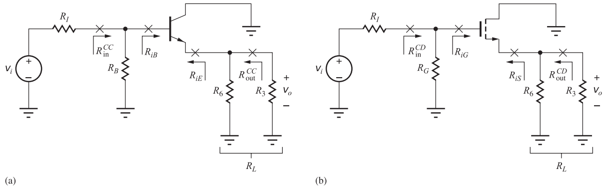
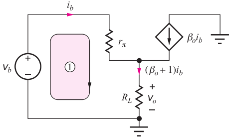


Figure 14.15 (a) ac equivalent circuit for the C-C amplif er. (b) ac equivalent circuit for the C-D amplif er.



- The voltage gain is defined as $v_0 = (\beta_0 + 1)i_b R_L$, where $R_L = R_3 \,||\, R_6$
- the input current is related to the applied voltage as $v_b = i_b r_\pi + (\beta_0 + 1)i_b R_L = i_b[r_\pi + (\beta_0 + 1)R_L]$

Common-Source Amplifier

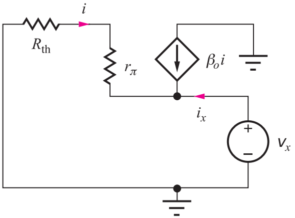
- The input resistance is defined as $R_{iB} = \frac{v_b}{i_b} = r_\pi + (\beta_0 + 1)R_L \approx r_\pi(1 + g_m R_L)$
- As for R_{in}, we've $R_{in}^{CC} = R_B \mid\mid R_{iB} = R_B \mid\mid r_\pi(1 + g_m R_L)$, where $R_L = R_6 \mid\mid R_3$
- The overall gain voltage is defined as

$$A_v^{CC} = A_{vt}^{CC}\left[\frac{R_B \mid\mid R_{iB}}{R_I + (R_B \mid\mid R_{iB})}\right]$$

- for the MOSFET it is $A_v^{CC} = A_{vt}^{CC}\left(\frac{v_b}{v_i}\right)$ ergo,

$$A_v^{CC} = A_{vt}^{CC}\left(\frac{R_G}{R_I + R_G}\right)$$

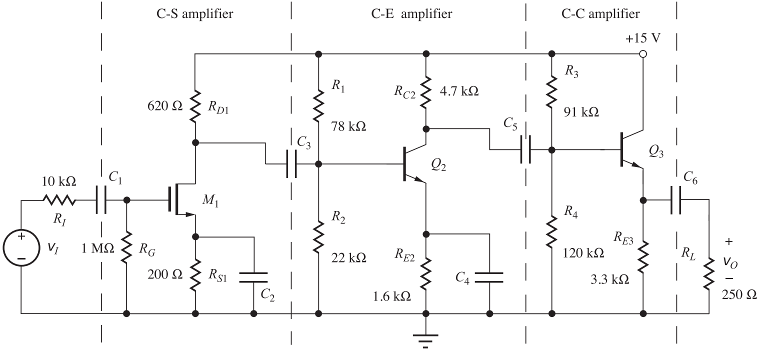
Common-Source Amplifier



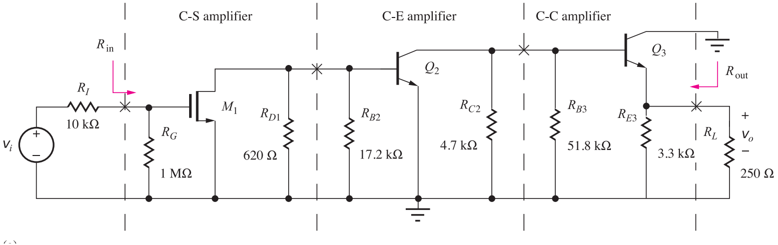
$$R_{iE} = \frac{\mathbf{v_x}}{\mathbf{i_x}}$$

- The output resistance is defined as $i_x = -i - \beta_0 i = \frac{v_x}{r\pi + R_{th}} - \beta_0 \left(-\frac{v_x}{r\pi + R_{th}}\right)$, rearranging terms $R_{iE} = \frac{r_\pi + R_{th}}{\beta_0 + 1} \approx g_m^{-1} + R_{th}\beta_0^{-1}$, fixing the terms and considering that $\beta_0 \gg 1$ $R_{iS} = gm^{-1}$
- The current gain is defined as $A_{it}^{CC} = \frac{i_1}{i} = \beta_0 + 1$ and $A_{it}^{CD} = \infty$

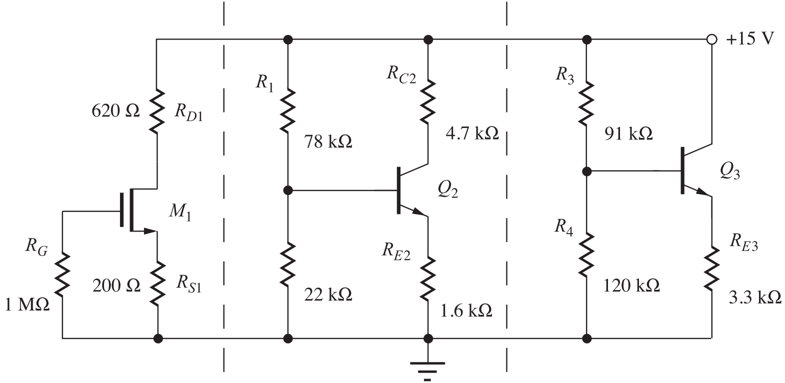
Multistage ac Coupled Amplifiers



Multistage ac Coupled Amplifiers



Multistage ac Coupled Amplifiers



Common-Source Amplifier

- In this example, C_1, C_3, C_5, and C_6 are coupling capacitors that provide dc isolation between stages
- It allows independent design of the bias circuitry
- $C_2 and C_4$ are bypass capacitors that are used to get the highest voltage gain from both configurations
- First stage is as CS amp, it has a high input impedance with ish voltage gain, second stage is a CE amp, it gives high voltage gain and the third is a voltage follower, it has los output resistance
- According to:
  M_1:K_n=10mA/V^2,V_{TN}=-2V, $\lambda = 0.02V^{-1}$
  Q_2:β_F=150, V_A= 80V, V_{BE}=0.7V
  Q_3:β_F 80, V_A=60V, V_{BE}=0.7V