

Ve320 Introduction of Semiconductor Device

Homework 7

Due Date: Aug. 03

Ex 7.1

- (a) Consider a Schottky diode at $T = 300\text{ K}$ that is formed with tungsten on n-type silicon. Use following Fig.1 to determine the barrier height. Assume a doping concentration of $N_d = 10^{16}\text{ cm}^{-3}$ and assume a cross-sectional area $A = 10^{-4}\text{ cm}^2$. Given that $A^* = 120\text{ A/K}^2 \cdot \text{cm}^2$, determine the forward-bias voltage required to induce a current of
- (i) $10\mu\text{A}$,
 - (ii) $100\mu\text{A}$,
 - (iii) 1mA .
- (b) Repeat part (a) for a temperature of $T = 350\text{ K}$. (Neglect the barrier lowering effect.)

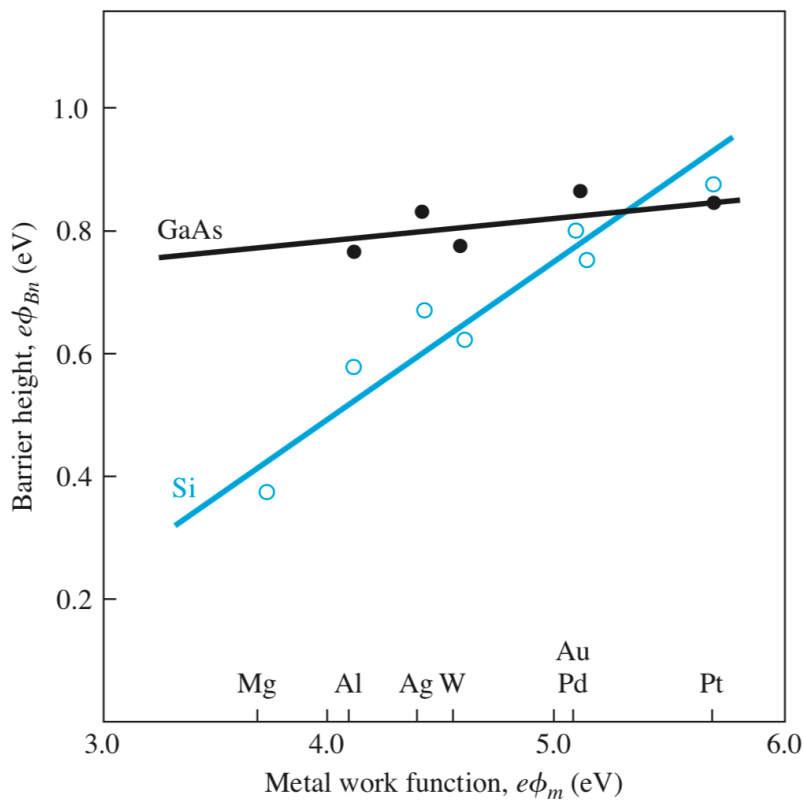


Figure 1. Experimental barrier heights as a function of metal work functions for GaAs and Si.

Ex 7.2

A pn junction diode and a Schottky diode each have cross-sectional areas of $A = 8 \times 10^{-4}\text{ cm}^2$. The reverse saturation current densities at $T = 300\text{ K}$ for the pn

junction diode and Schottky diode are $8 \times 10^{-13} \text{ A/cm}^2$ and $6 \times 10^{-9} \text{ A/cm}^2$, respectively. Determine the required forward-bias voltage in each diode to yields currents of

- (a) $150 \mu\text{A}$,
- (b) $700 \mu\text{A}$,
- (c) 1.2 mA .

Ex 7.3

The dc charge distributions of four ideal MOS capacitors are shown in the Following Fig.2. For each case:

- (a) Is the semiconductor n or p type?
- (b) Is the device biased in the accumulation, depletion, or inversion mode?
- (c) Draw the energy- band diagram in the semiconductor region.

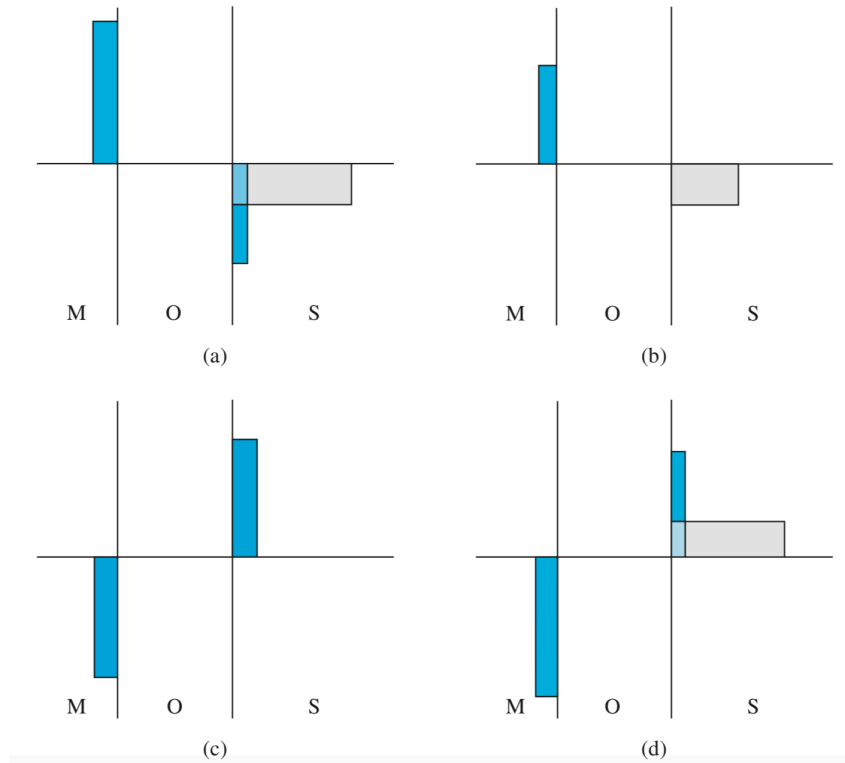


Figure 2. Figure for Ex 2.3.

Ex 7.4

- (a) Consider an n^+ polysilicon–silicon dioxide–n-type silicon MOS structure. Let $N_a = 4 \times 10^{15} \text{ cm}^3$. Calculate the ideal flat-band voltage for $t_{ox} = 20 \text{ nm} = 200 \text{ \AA}$.
- (b) Considering the results of part (a), determine the shift in flat-band voltage for
 - (i) $Q'_{ss} = 4 \times 10^{10} \text{ cm}^{-2}$, and
 - (ii) $Q'_{ss} = 10^{11} \text{ cm}^{-2}$.
- (c) Repeat parts (a) and (b) for an oxide thickness of $t_{ox} = 12 \text{ nm} = 120 \text{ \AA}$.

Ex 7.5

The high-frequency C–V characteristic curve of a MOS capacitor is shown in the following Fig.3. The area of the device is $2 \times 10^{-3} \text{cm}^2$. The metal–semiconductor work function difference is $\phi_{ms} = -0.50 \text{V}$, the oxide is SiO_2 , the semiconductor is silicon, and the semiconductor doping concentration is $2 \times 10^{16} \text{cm}^{-3}$.

- Is the semi- conductor n or p type?
- What is the oxide thickness?
- What is the equivalent trapped oxide charge density?
- Determine the flat-band capacitance.
- Indicate which points correspond to flat-band, inversion, accumulation, threshold, and depletion modes.

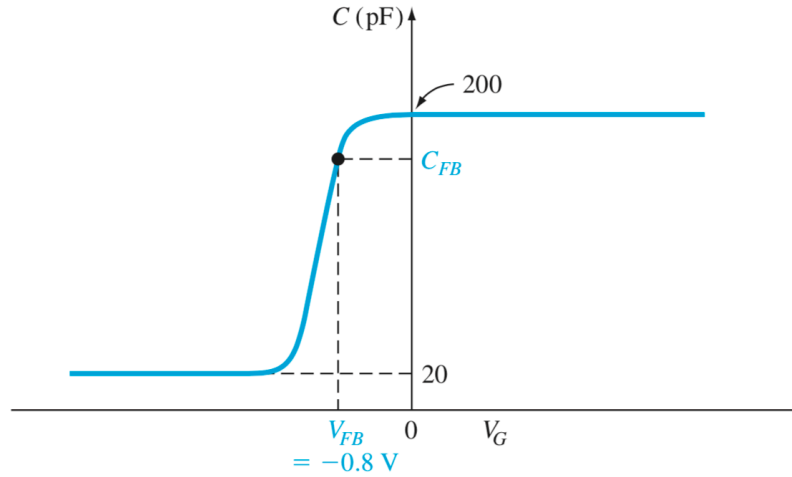


Figure 3. Figure for Ex 7.5.

Ex 7.6

The parameters of an n-channel MOSFET are $k'_n = 0.6 \text{mA/V}^2$ and $V_T = 0.8 \text{V}$. The drain current is 1mA with applied voltages of $V_{GS} = 1.4 \text{V}$, $V_{SB} = 0$, and $V_{DS} = 4 \text{V}$.

- What is the W/L value?
- What is the value of I_D for $V_{GS} = 1.85 \text{V}$, $V_{SB} = 0$, and $V_{DS} = 6 \text{V}$?
- Determine the value of I_D for $V_{GS} = 1.2 \text{V}$, $V_{SB} = 0$, and $V_{DS} = 0.15 \text{V}$.

Ex 7.7

Consider an ideal p-channel MOSFET with the following parameters: $V_T = -0.35 \text{V}$, $\mu_p = 210 \text{cm}^2/\text{V} \cdot \text{s}$, $t_{ox} = 11 \text{nm} = 110 \text{\AA}$, $W = 35 \mu\text{m}$, and $L = 1.2 \mu\text{m}$.

- Plot I_D versus V_{SD} for $0 \leq V_{SD} \leq 3 \text{V}$ and for $V_{SG} = 0, 0.6, 1.2, 1.8$, and 2.4V . Indicate on each curve the $V_{SD}(\text{sat})$ point.

- (b) Plot $\sqrt{I_D(sat)}$ versus V_{SG} for $0 \leq V_{SG} \leq 2.4 V$.
- (c) Plot I_D versus V_{SG} for $0 \leq V_{SG} \leq 2.4 V$ and for $V_{SD} = 0.1 V$.

Ex 7.8

Assume that the subthreshold current of a MOSFET is given by:

$$I_D = 10^{-15} \exp\left(\frac{V_{GS}}{(2.1)V_t}\right)$$

over the range $0 \leq V_{GS} \leq 1$ volt and where the factor 2.1 takes into account the effect of interface states. Assume that 10^6 identical transistors on a chip are all biased at the same V_{GS} and at $V_{DD} = 5 V$.

- (a) Calculate the total current that must be supplied to the chip at $V_{GS} = 0.5, 0.7$, and $0.9 V$.
- (b) Calculate the total power dissipated in the chip for the same V_{GS} values.

Ex 7.9

Consider an n-channel silicon MOSFET. The parameters are $k'_n = 75 \mu A/V^2$, $W/L = 10$, and $V_T = 0.35 V$. The applied drain-to-source voltage is $V_{DS} = 1.5 V$.

- (a) For $V_{GS} = 0.8 V$, find
- (i) the ideal drain current,
 - (ii) the drain current if $\lambda = 0.02 V^{-1}$, and
 - (iii) the output resistance for $\lambda = 0.02 V^{-1}$.
- (b) Repeat part (a) for $V_{GS} = 1.25 V$.

Ex 7.10

The parameters of an n-channel enhancement-mode MOSFET are $V_T = 0.40 V$, $t_{ox} = 20 nm = 200 \text{\AA}$, $L = 1.0 \mu m$, and $W = 10 \mu m$.

- (a) Assuming a constant mobility of $\mu_n = 475 cm^2/V \cdot s$, calculate I_D for $V_{GS} = V_T = 2.0 V$ when biased at
- (i) $V_{DS} = 0.5 V$,
 - (ii) $V_{DS} = 1.0 V$,
 - (iii) $V_{DS} = 1.25 V$,
 - (iv) $V_{DS} = 2.0 V$.
- (b) Consider the piecewise linear model of the carrier velocity versus V_{DS} shown in the following Fig.4. Calculate I_D for the same voltage values given in part (a). [You may refer to Equation (11.17) in textbook.]
- (c) Determine the $V_{DS}(sat)$ values for parts (a) and (b).

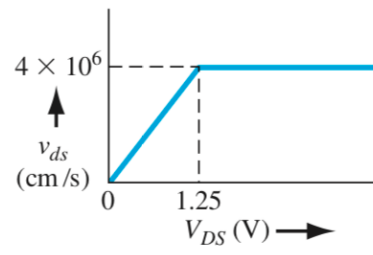


Figure 4. Figure for Ex 7.10.