VARISCITE LTD.

DART-MX8M-PLUS V1.x Datasheet

NXP i.MX 8M PLUS™ - based System-on-Module

VARISCITE LTD.

DART-MX8M-PLUS Datasheet

Variscite Ltd.
4, Hamelacha Street
Lod
P.O.B 1121
Airport City, 70100
ISRAEL

Tel: +972 (9) 9562910
Fax: +972 (9) 9589477

1. Document Revision History

Revision	Date	Notes
1.0	October 21, 2020	Initial - Preliminary
1.01	Dec, 2020	-Correct Table 1 Hardware Configuration Options “LD” to “DSCM” configuration (DSI export locations) -Update all related tables for “DSCM” configuration -Removed note for CAN Bus availability on Industrial grade only.
1.02	Feb, 2021	NVCC_3V3 output power supply capabilities section added
1.03	Mar, 2021	Added Section 8.21.1.1 for NVCC_SAI1_SAI5 Updated notes for pin referenced to NVCC_SAI1_SAI5
1.04	Apr, 2021	Updated Reliability data section 10
1.05	May, 2021	Updated Mechanical drawing section 11.3 Updated ECSPI Features list section 8.13
1.06	Jul, 2021	Updated Sections 5.1.4, 5.1.8-9, 5.1.11-14 according to NXP’s updated RM Rev 1 Updated section 9.5 Table 71 Updated section 8.11 Features
1.07	Nov 04, 2021	Updated Block Diagram Added EEPROM section 5.7
1.08	Feb 13, 2022	Added note for CAN-FD section 8.12
1.09	Mar 16, 2021	Added Ethernet PHY ADIN1300 – Updated sections 4.3, 5.6, 7.3, 8.5 Updated section 5.3

2. Table of Contents

3. List of Tables

4. Overview

4.1 General Information

The DART-MX8M-PLUS offers a high-performance processing for a low-power System-on-Module. The product is based on the i.MX 8M Plus family which is a set of NXP products focused on machine learning applications, combining state-of-art multimedia features with high-performance processing optimized for low-power consumption.

The i.MX 8M Plus Media Applications Processor is built to achieve both high performance and low power consumption and rely on a powerful, fully coherent core complex based on a quad Cortex-A53 cluster and Cortex-M7 low-power coprocessor, audio digital signal processor, machine learning and graphics accelerators.

This heterogeneous multicore processing architecture enables the device to run an open operating system like Linux and an RTOS like FreeRTOS™ on the Cortex-M7 core for time and security critical tasks.

The DART-MX8M-PLUS provides an ideal building block for simple integration with a wide range of products in target markets requiring high-performance processing with low power consumption, compact size and a very cost-effective solution.

Supporting products:

- DT8MCustom-Board – evaluation board
  - ✓ Carrier Board, compatible with DART-MX8M-PLUS
  - ✓ Schematics
- VAR-DVK-MX8MP full development kit, including:
  - ✓ DT8MCustom-Board
  - ✓ DART-MX8M-PLUS
  - ✓ Display and touch
  - ✓ Accessories and cables
- O.S support
  - ✓ Linux BSP
  - ✓ Android

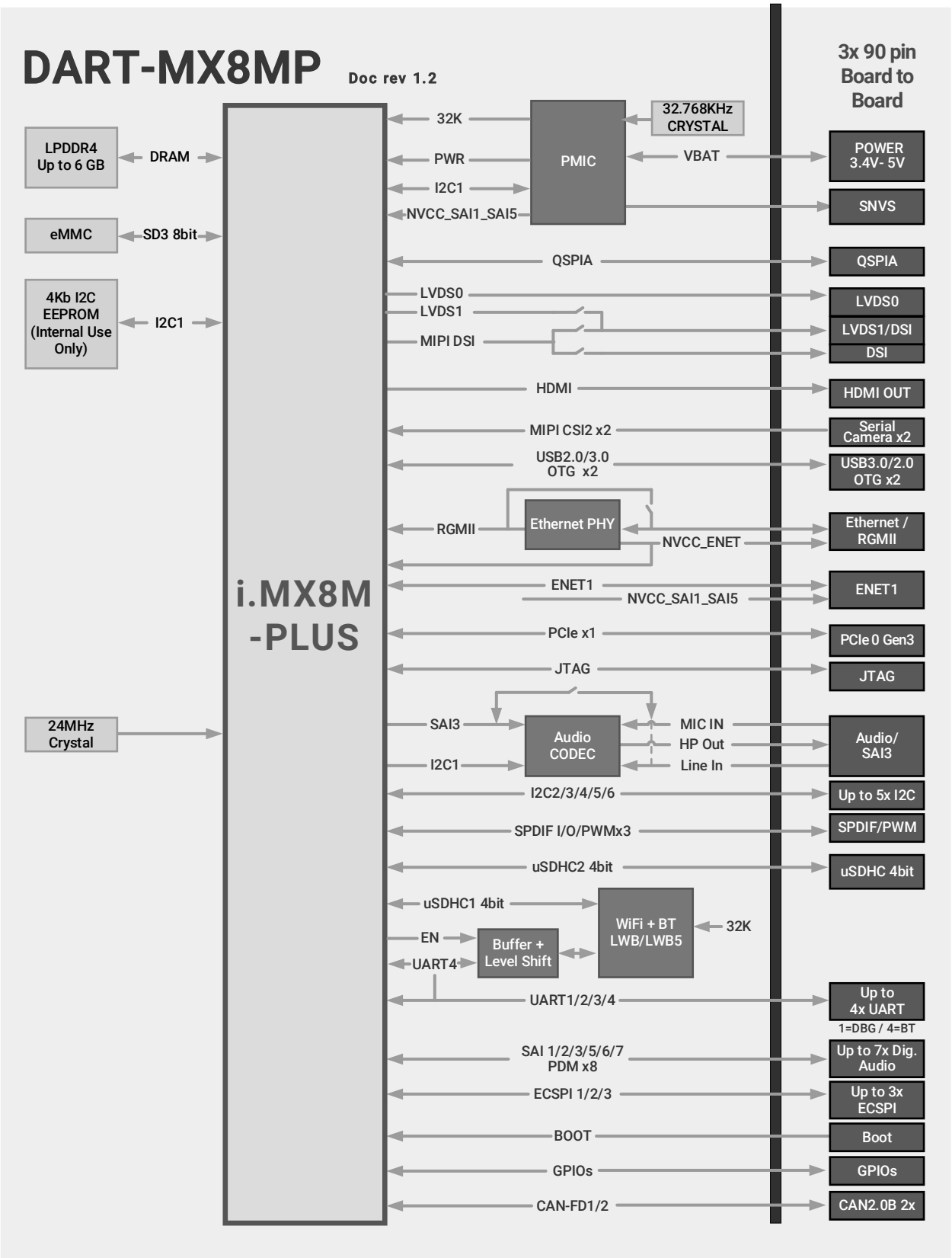
✓ Contact Variscite support services for further information: support@variscite.com.

4.2 Feature Summary

- NXP i.MX8M-PLUS series SOC
  - 4x Cortex A53 up to @ 1.8 GHz
  - 1x Cortex M7 @ 800 MHz
  - 1x Hi-Fi DSP @ 800 MHz
- GPU and the AI/ML accelerators specs
  - Neural Processing Unit (NPU): Delivers up to 2.3 TOPS
- Memory
  - Up to 6GB LPDDR4 RAM @ 2000Mhz
  - 8-bit up to 64GB eMMC boot and storage
- Display Support
  - 2x LVDS interface 4-lane each, up to 1080p60
  - HDMI 2.0a
  - 1x MIPI DSI with up to 4 data lanes
- Networking
  - 2x 10/100/1000 Mbit/s Ethernet Interface
  - Certified Wi-Fi 802.11 ac/a/b/g/n
  - Bluetooth: 4.2/BLE
- Camera
  - Up to 2x MIPI CSI – CMOS Serial camera Interface 4 lanes
  - 375 Mpixel/s HDR ISP (Image Sensor Processor)
- Audio
  - Analog Stereo line in
  - Analog headphones out
  - Digital microphone
  - Up to 6x Digital audio (SAI)
  - 8-channel PDM microphone input
  - SPDIF
- USB
  - 2x USB 3.0/2.0 Host/Device
- Other Interfaces
  - SDIO/MMC
  - 1x PCIe v3.0
  - Resistive touch controller
  - Serial interfaces (ECSPI, FlexSPI, I2C, UART, CAN, JTAG)
  - GPIOs
  - JTAG
- Single power supply: 3.4V – 5V
- Dimensions (W x L x H): 55 mm x 30 mm x 4.56mm
- Industrial temperature range -40°C to 85°C

4.3 Block Diagram

Figure 1 : DART-MX8M-PLUS Block Diagram



5. Main Hardware Components

This section summarizes the main hardware building blocks of the DART-MX8M-PLUS.

5.1 NXP i.MX 8M Plus

5.1.1 Overview

The i.MX 8M Plus family focuses on machine learning and vision, advanced multimedia, and industrial IoT with high reliability. It is built to meet the needs of Smart Home, Building, City and Industry 4.0 applications.

- Powerful quad or dual Arm® Cortex®-A53 processor with a Neural Processing Unit (NPU) operating at up to 2.3 TOPS.
- Real-time control with Cortex-M7. Robust control networks supported by dual CAN FD (IT version) and dual Gigabit Ethernet, one of which, with Time Sensitive Networking (TSN).
- The multimedia capabilities include video encode (including h.265) and decode, 3D/2D graphic acceleration, and multiple audio and voice functionalities.
- Dual Image Signal Processors and two camera inputs for an effective Vision System.
- High industrial reliability with DRAM inline ECC and ECC on on-chip RAM.

5.1.2 i.MX 8M Plus Block Diagram

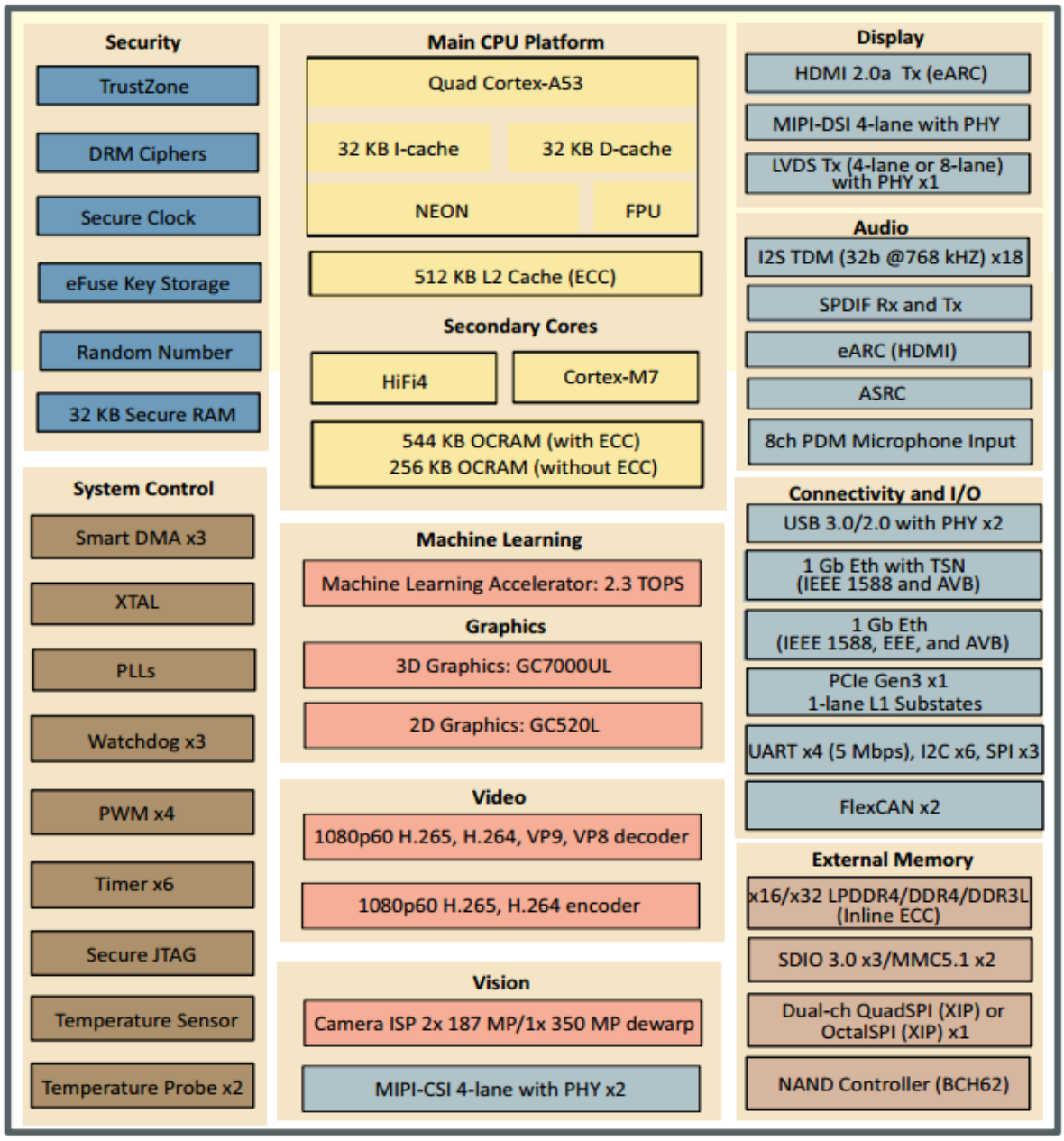


Figure 2 : i.MX 8M Plus Block Diagram

5.1.3 ARM Cortex-A53 MPCore™ Platform

The i.MX 8M Plus family Applications Processors are based on the ARM Cortex-A53 MPCore™ platform, which has the following features:

- Quad symmetric Cortex-A53 processors operation up to 1.8 GHz, including:
  - 32 KB L1 Instruction Cache
  - 32 KB L1 Data Cache
  - Media Processing Engine (MPE) with NEON technology supporting the Advanced Single Instruction Multiple Data architecture
  - Floating Point Unit (FPU) with support of the VFPv4-D16 architecture
- Support of 64-bit Armv8-A architecture
  512 KB unified L2 cache

5.1.4 Arm Cortex M7 Platform

The Cortex-M7 Core Platform includes the following:

- Low power microcontroller available for customer application:
  - 32 KB L1 Instruction Cache
  - 32 KB L1 Data Cache
  - 256 KB TCM
- Available customer applications include:
  - Low power standby mode
  - IoT device control
  - ML applications

5.1.5 System Bus and Interconnect

System bus and interconnect include the following:

- Network interconnect (NoC) AXI arbiter
- Quality of service controller (QoSC) to configure priorities and limits of AXI transactions
- Performance monitor (PERFMON) to monitor AXI bus activity
- Debug monitor (DBGMON) to record AXI transactions preceding a system reset

5.1.6 Clocking and Resets

Clocking and resets include:

- Clock control module (CCM) provides centralized clock generation and control
  - Simplified clock tree structure
  - Unified clock programming model for each clock root
  - Multicore awareness for resource domains
- System reset controller (SRC) provides reset generation and distribution

5.1.7 Interrupts and DMA

Interrupts and DMA include:

- 160 shared peripheral interrupts routed to Cortex-A53 Global Interrupt Controller GIC) and Cortex-M7 nested vector interrupt controller (NVIC) for flexible interrupt handling
- Three Smart direct memory access (SDMA) engines. Although these three engines
- are identical to each other, they are integrated into the processor to serve different peripherals.
    - SDMA-1 is a general-purpose DMA engine which can be used by low speed peripherals including UART, SPI and also other peripherals.
    - SDMA-2 and SMDA-3 is used for audio interface, including SAI-1/2/3/5/6/7, SPDIF and PDM audio input

5.1.8 On-Chip Memory

The on-chip memory system consists of the following:

- Boot ROM (256KB)
- On-Chip RAM - OCRAM (576KB)
- Audio Processor System RAM - OCRAM_A (256KB)
- On-Chip RAM for State Retention - OCRAM_S (36KB)

5.1.9 External Memory Interface

The external memory interfaces supported on this chip include:

- 32-bit DRAM Interface:
    - LPDDR4-4000
    - DDR4-3200
- 8-bit NAND FLASH, including support for Raw MLC/SLC devices, BCH ECC up to 62-bit, and ONFi3.2 compliance (clock rates up to 100 MHz and data rates up to 200 MB/sec)
- eMMC 5.1 FLASH (2 interfaces)
- SPI NOR FLASH (3 interfaces)
- FlexSPI FLASH with support for XIP (for Cortex-M7 in low-power mode) and support for either one Octal SPI, or parallel read mode of two identical Quad SPI FLASH devices

5.1.10 Timers

- The timers on this chip include:
- One local generic timer integrated into each Cortex-A53 CPU
- Global system counter with timer bus interface to Cortex-A53 MPCore generic timers
- One local system timer (SysTick) integrated into the Cortex-M7 CPU
- Six general purpose timer (GPT) modules
- Three watchdog timer (WDOG) modules
- Four pulse width modulation (PWM) modules

5.1.11 Graphics Processing Unit (GPU)

The chip incorporates the following Graphics Processing Unit (GPU) features:

• One GPU for 2D and composition acceleration

- Supports multi-source composition
- Supports one-pass filter
- Supports tile format

• One GPU for 3D processing

- Two Shader Execution Units
- Supports OpenGL ES 1.1, 2.0, 3.0, 3.1
- Supports OpenCL 3.0
- Supports OpenVG 1.1
- Supports OpenGL 4.0
- Supports EGL 1.5
- Supports Vulkan 1.1
- Supports tile format

5.1.12 Graphics Processing Unit (VPU)

The chip incorporates the following Video Processing Unit (VPU) features:

- Video Decode:
  - 1080p60 HEVC/H.265 Main, Main 10 (up to level 5.1) (VPU G2)
  - 1080p60 VP9 Profile 0, 2 (VPU G2)
  - 1080p60 VP8 (VPU G1)
  - 1080p60 AVC/H.264 Baseline, Main, High decoder (VPU G1)
- Video Encode:
  - 1080p60 AVC/H.264 encoder
  - 1080p60 HEVC/H.265 encoder
- TrustZone support

5.1.13 Machine Learning: NPU (Neural Processing Unit)

- 2.3 TOP/s Neural Network performance available for user applications
  - Speech recognition (e.g., Deep Speech 2)
  - Image recognition (e.g., ResNet-50)
  - Object detection (e.g., MobileNet-SSD)

5.1.14 Display Interfaces

The chip has the following display support:

- Three LCDIF Display Controllers:
  - One LCDIF drives MIPI DSI
  - One LCDIF drives LVDS Tx
  - One LCDIF drives HDMI Tx
  - Supports 8-bit / 16-bit / 18-bit / 24-bit / 32-bit pixel depth
  - Supports up to 1080p60 display per LCDIF, if no more than 2 instances used simultaneously
  - Supports 1x1080p60 + 2x720p60 if all 3 instances used simultaneously
  - Supports one layer
- MIPI Interface:
  - One 4-lane MIPI DSI interface
  - Two 4-lane MIPI CSI interfaces
- Two 4-lane LVDS interfaces
- ISI (Image Sensor Interface):
  - The ISI is a simple camera interface that supports image processing and transfer
  - via a bus master interface for up to 2 cameras
- Two Camera ISP (Image Signal Processor):
  - When one camera is used, supports up to 12MP@30fps or 4kp45
  - When two cameras are used, each supports up to 1080p80
- HDMI 2.0a
  - HDMI 2.0a Tx supporting one display
    - Resolutions of: 740x480p60, 720x480p60, 1280x720p60, 1920x1080p60
- Audio support
  - 32 channel audio output support
  - 1 S/PDIF audio eARC input support

5.1.15 Audio

Audio include the following:

- Audio DSP
- S/PDIF Input and Output, including a Raw Capture input mode
- Six external SAI (synchronous audio interface) modules supporting I2S, AC97, TDM, codec/DSP and DSD interfaces, comprising one SAI with 8 TX and 8 RX lanes, one SAI with 4 TX and 4 RX lanes, two SAI with 2 TX and 2 RX lanes, and two SAI with 1 TX and 1 RX lanes.
- PDM Microphone Interface module which supports up to 8-microphones (4 lanes)
- Asynchronous Sample Rate Converter (ASRC) module which supports:
  - Processing of up to 32 audio channels
  - 4 context groups
  - 8 kHz to 384 kHz sample rate
  - 1/16 to 8x sample rate conversion ratio

5.1.16 General Connectivity Interfaces

The chip contains a rich set of general connectivity interfaces, including:

- One PCI Express (PCIe):
  - Single lane supporting PCIe Gen 3
  - Dual mode operation to function as root complex or endpoint
  - Integrated PHY interface
  - Supports L1 low power substate
- Two USB 3.0 Type C controllers with integrated PHY interface
  - Backwards compatibility with USB 2.0
  - Spread spectrum clock support
- Three Ultra Secure Digital Host Controller (uSDHC) interfaces
  - MMC 5.1 compliance with HS400 DDR signaling to support up to 400 MB/sec
  - SD/SDIO 3.01 compliance with 200 MHZ SDR signaling to support up to 100 MB/sec
  - Support for SDXC (extended capacity)
- Two Ethernet controllers, capable of simultaneous operation
  - One Gigabit Ethernet controller with support for EEE, Ethernet AVB and IEEE1588
  - One Gigabit Ethernet controller with support for TSN, EEE, Ethernet AVB and IEEE1588
- Two controller area network (FlexCAN) modules, each optionally supporting Flexible Data-rate (FD)
- Four universal asynchronous receiver/transmitter (UART) modules
- Six I2C modules
- Three SPI modules

5.1.17 Security

Security functions are enabled and accelerated by the following hardware:

- RDC – Resource Domain Controller:
  - Supports 4 domains and up to 8 regions
- Arm TrustZone including the TZ architecture:
  - ARM Cortex-A53 MPCore TrustZone support
- On-chip RAM (OCRAM) secure region protection using OCRAM controller
- High Assurance Boot (HAB)
- Cryptographic Acceleration and Assurance Module (CAAM)
  - Support Widevine and PlayReady content protection
  - Public Key Cryptography (PKHA) with RSA and Elliptic Curve (ECC) algorithms
  - Real-time integrity checker (RTIC)
  - DRM support for RSA, AES, 3DES, DES
  - Side channel attack resistance
  - True random number generation (RNG)
  - Manufacturing protection support
- Secure Non-Volatile Storage (SNVS), including Secure Real Time Clock (SRTC)
- Secure JTAG Controller (SJC)

5.1.18 Multicore Support

Multicore support contains:

- Resource domain controller (RDC) to support isolation and safe sharing of system resources
- Messaging unit (MU)
- Hardware Semaphore (SEMA42)
- Shared bus topology

5.1.19 GPIO and Pin Multiplexing

- General-purpose input/output (GPIO) modules with interrupt capability
- Input/output multiplexing controller (IOMUXC) to provide centralized pad control

5.1.20 Power Management

The power management unit consists of:

- Temperature sensor with programmable trip points
- Flexible power domain partitioning with internal power switches to support efficient power management

5.1.21 System Debug

The system debug features are:

- ARM CoreSight debug and trace architecture
- Embedded Trace FIFO (ETF) with 4 KB internal storage to provide trace buffering
- Unified trace capability for Quad Cortex-A53 and Cortex-M7 CPUs
- Cross Triggering Interface (CTI)
- Support for 5-pin (JTAG) debug interfaces

5.2 Memory

5.2.1 RAM

The DART-MX8M-PLUS is available with up to 4 GB of LPDDR4 memory running at maximum 4000 MTS.

5.2.2 Non-volatile Storage Memory

The DART-MX8M-PLUS is available with a non-volatile MLC eMMC storage memory with optional densities of up to 64GB. It is used for Flash Disk purposes, O.S. run-time-image, Boot-loader and application/user data storage.

5.3 Audio (WM8904)

The WM8904 is a high performance ultra-low power stereo CODEC optimized for portable audio applications.
The device features stereo ground-referenced headphone amplifiers using the Wolfson 'Class-W' amplifier techniques. It incorporates an innovative dual-mode charge pump architecture - to optimize efficiency and power consumption during playback.
The ground-referenced headphone output eliminates AC coupling capacitors, and both outputs include common mode feedback paths to reject ground noise. Control sequences for audio path setup can be pre-loaded and executed by an integrated control write sequencer to reduce software driver development and minimize pops and clicks via SilentSwitch™ technology. The input impedance is constant with PGA gain setting. A stereo digital microphone interface is provided, with a choice of two inputs. A dynamic range controller provides compression and level control to support a wide range of portable recording applications. Anti-clip and quick release features offer good performance in the presence of loud impulsive noises. ReTuneTM Mobile 5-band parametric equalizer with fully programmable coefficients is integrated for optimization of speaker characteristics. Programmable dynamic range control is also available for maximizing loudness, protecting speakers from clipping and preventing premature shutdown due to battery droop. Common audio sampling frequencies are supported from a wide range of external clocks, either directly or generated via the FLL.

Features:

- 3.0mW quiescent power consumption for DAC to headphone playback
- DAC SNR 96dB typical, THD -86dB typical
- ADC SNR 91dB typical, THD -80dB typical
- 2.4mW quiescent power consumption for analogue bypass playback
- Control write sequencer for pop minimized start-up and shutdown
- Single register writes for default start-up sequence
- Integrated FLL provides all necessary clocks - Self-clocking modes allow processor to sleep - All standard sample rates from 8kHz to 96kHz
- Stereo digital microphone input
- 2 single ended inputs per stereo channel
- Digital Dynamic Range Controller (compressor / limiter)
- Digital sidetone mixing
- Ground-referenced headphone driver

5.4 Wi-Fi + BT

DART-MX8M-PLUS module can be configured either for Dual band or Single Band Wi-Fi® and Bluetooth® add on modules. Both realize the necessary PHY/MAC layers to support WLAN applications in conjunction with a host processor over a SDIO interface.
The modules also provide a Bluetooth/BLE platform through the HCI transport layer. Both WLAN and Bluetooth share the same antenna port.

DART-MX8M-PLUS Wi-Fi and BT Key Features:

- IEEE 802.11 ac/a/b/g/n (Dual Band Option)
- IEEE 802.11 b/g/n (Single Band Option)
- Bluetooth 2.1+EDR, and BLE 4.2
- U.F.L connector for external antenna
- Latest Linux and Android drivers supported directly by LSR and Cypress
- Wi-Fi/BT module Broad certifications with multiple antennas: FCC (USA), IC (Canada), ETSI (Europe), Giteki (Japan), and RCM (AU/NZ)
- Industrial operating Temperature Range: -40 to +85

5.4.1 DART-MX8M-PLUS Dual Band Option

The DART-MX8M-PLUS contains LSR's certified high-performance Sterling-LWB5™ Dual band 2.4/5 GHz Wi-Fi® and Bluetooth® Smart Ready Multi-Standard Module based upon the Cypress (formerly Broadcom) CYW43353 chipset supporting 802.11 ac/a/b/g/n, BT 2.1+EDR, and BLE 4.2 wireless connectivity.

5.4.2 DART-MX8M-PLUS Single Band Option

The DART-MX8M-PLUS contains Laird's certified high-performance Sterling-LWB™ 2.4 GHz Wi-Fi® and Bluetooth® Smart Ready Multi-Standard Module based upon the Cypress (formerly Broadcom) CYW4343W chipset supporting IEEE 802.11 b/g/n,
BT 2.1+EDR, and BLE 4.2 wireless connectivity.

5.5 PMIC

The DART-MX8M-PLUS features Dual Freescale/NXP's PCA9450CHN chip as a Power Management Integrated circuit (PMIC) designed specifically for use with NXP's i.MX 8M Plus series of application processors. The PCA9450CHN regulates power rails required on SOM from a single 3.3V power supply. The PMIC is fully programmable via the I2C interface and associated register map.
Additional communication is provided by direct logic interfacing including interrupt, watchdog and reset.

5.6 10/100/1000 Mbps Ethernet Transceiver

The SOM can be ordered with an Integrated Ethernet Transceiver,
Qualcomm Atheros AR8033 or Analog Devices ADIN1300.
Please contact sales@variscite.com for inquiries about P/N assembled on your SOM.

5.6.1 Qualcomm Atheros AR8033 Ethernet Transceiver

Key features include:

- 10BASE-Te/100BASE-TX/1000BASE-T IEEE 802.3 compliant
- 1000BASE-T PCS and auto-negotiation with next page support
- Green ETHOS power saving modes with internal automatic DSP power saving scheme
- IEEE 802.3az EEE
- Fully integrated digital adaptive equalizers, echo cancellers, and Near End Crosstalk (NEXT) cancellers
- Robust Cable Discharge Event (CDE) protection of ±6 kV
- Robust operation over up to 140 meters of CAT5 cable
- Automatic Channel Swap (ACS)
- Automatic MDI/MDIX crossover
- Automatic polarity correction ν IEEE 802.3u compliant auto-negotiation
- Jumbo frame supports up to 10 KB (full-duplex)
- Integrated termination circuitry at the line side

5.6.2 Analog Devices ADIN1300 Ethernet Transceiver

Key features include:

- 10BASE-Te/100BASE-TX/1000BASE-T IEEE® 802.3™ compliant MII, RMII, and RGMII MAC interfaces
- EEE in accordance with IEEE 802.3az
- Start of packet detection for IEEE 1588 time stamp support
- Enhanced link detection
- Configurable LED
- Integrated power supply monitoring and POR
- MII management interface (MDIO) compatible with the IEEE 802.3 Standard Clause 22 and Clause 45 management frame structures.
- Supports cable lengths up to 150 meters at Gigabit speeds and 180 meters when operating at 100 Mbps or 10 Mbps.
- Automatic MDI/MDIX crossover
- Autonegotiation capability in accordance with IEE 802.3 Clause 28
- Supports a number of power-down modes: hardware, software, and energy detect power-down, and EEE LPI mode
- On-chip cable diagnostics capabilities
- Transmit drivers are voltage mode with on-chip terminations

5.7 EEPROM

The SOM uses 4Kbit serial EEPROM to store memory calibration and manufacturing parameters. This EEPROM is connected to I2C1 bus and intended only for holding the above information. The SOM may not boot if the contents of EEPROM device are corrupted.

6. DART-MX8M-PLUS Hardware Configuration

The table below lists the Hardware configurations options orderable for the DART-MX8M-PLUS.

Table 1 Hardware Configuration Options

Option	Description
EC	Ethernet PHY assembled on SOM
AC	Audio Codec assembled on SOM
WBD	Dual band 2.4/5 GHz Wi-Fi and BT/BLE combo assembled on SOM
WB	Single band 2.4GHz Wi-Fi and BT/BLE combo assembled on SOM
DSCM	DSI Compatibility Mode: DSI lanes exported via SOM connector pins instead of LVDS1 lanes – as in DART-MX8M and DART-MX8M-Mini; By default, DSI exported on other pins.

NOTE

Other orderable options are available and are not part of this datasheet.
Please refer to Variscite official website for complete list of configuration options.

7. External Connectors

7.1 Board to Board Connector

- The DART-MX8M-MINI exposes three 90-pin board-to-board connectors.
- The recommended mating connector is: **Hirose Electric Co Ltd PN: DF40C-90DS-0.4V(51)**

7.2 Wi-Fi & BT Connector

In Modules with Wi-Fi **"WB"** or **"WBD"** Configuration - a combined Wi-Fi + BT antenna connector is assembled.

- Connector type: **U.FL JACK connector**
- Cable and antenna shall have a 50 Ohm characteristic impedance

7.3 DART-MX8M-PLUS Connector Pin-out

Tables under this section lists the SOM connectors pinout with each pin listed for all the available ball names related to the assembly hardware configuration options.

Table 2: PIN-OUT Tables Mnemonics

Column Heading		Meaning
PIN#	**Jx.YY**	Pin number on a connector: Jx : Can be J1 J2 or J3 YY : Can be 1 to 90
ASSY		Can be any of the **options listed in Table 1**. **"NO"** - will be added to above option - means the option is not part of the SOM part number. **Blank** - pin listed have no hardware configuration option **NC** - Pin is Not Connected
BALL NAME		Name of the ball for the specific ASSY option
GPIO	**GPIOx_y**	SOC pin GPIO Alternate function number including: **x- GPIO bank** **y-Bit number in the bank**
NOTES		This column displays any special note related to the specific pin with the specific ASSY The notes will repeat also in the function tables.
BALL		Source device and it's pin number.
	XX.YY	XX: Source Chip can be: SOC.yy – pins connected to the iMX8M SoC AR8033.yy/ ADIN1300.yy – pins connected the Ethernet Controller (***"EC" Configuration***) WM8904.yy - pins connected the Audio Codec (***"AC" Configuration***) YY : Pin/Ball number of source chip.

NOTE

A. Some pins may appear in several consecutive lines if additional chip function used on SOM; Relates to the DART-MX8M-MINI orderable hardware configuration.
B. In case a chip is added due to an orderable configuration the chip function must be used.

7.3.1 DART-MX8M-PLUS J1 Pin-out

Table 3: DART-MX8M-PLUS J1 Pinout

PIN#	ASSY	BALL NAME	GPIO	NOTES	BALL
J1.1		GPIO1_IO00	GPIO1_IO00		SOC.A7
J1.2	No EC	ENET_TD1	GPIO1_IO20	Powered by NVCC_ENET pin	SOC.AE26
J1.2	EC	ETH_TRX1_P		Signal source is Ethernet PHY.	AR8033.14/ ADIN1300.14
J1.3	No EC	ENET_TX_CTL	GPIO1_IO22	Powered by NVCC_ENET pin	SOC.AF24
J1.3	EC	NC		With "EC" configuration this pin in Not Connected.	NC
J1.4	No EC	ENET_TD0	GPIO1_IO21	Powered by NVCC_ENET pin	SOC.AC25
J1.4	EC	ETH_TRX1_N		Signal source is Ethernet PHY.	AR8033.15/ ADIN1300.15
J1.5	No EC	ENET_TXC	GPIO1_IO23	Powered by NVCC_ENET pin; Includes series EMI filter	SOC.AE24
J1.5	EC	ETH_LED_LINK10_100		Signal source is Ethernet PHY.	AR8033.26/ ADIN1300 - GND
J1.6	No EC	ENET_TD2	GPIO1_IO19	Powered by NVCC_ENET pin	SOC.AF26
J1.6	EC	ETH_TRX0_N		Signal source is Ethernet PHY.	AR8033.12/ ADIN1300.13
J1.7	No EC	ENET_RXC	GPIO1_IO25	Powered by NVCC_ENET pin; Includes series EMI filter	SOC.AE29
J1.7	EC	ETH_LED_LINK1000		Signal source is Ethernet PHY.	AR8033.24/ ADIN1300.26 (via level shifter)
J1.8	No EC	ENET_TD3	GPIO1_IO18	Powered by NVCC_ENET pin	SOC.AD24
J1.8	EC	ETH_TRX0_P		Signal source is Ethernet PHY.	AR8033.11/ ADIN1300.12
J1.9	No EC	ENET_RX_CTL	GPIO1_IO24	Powered by NVCC_ENET pin	SOC.AE28
J1.9	EC	ETH_LED_ACT		Signal source is Ethernet PHY.	AR8033.23/ ADIN1300.21 via inv. FET
J1.10	No EC	ENET_RD0	GPIO1_IO26	Powered by NVCC_ENET pin	SOC.AG29
J1.10	EC	ETH_TRX2_P		Signal source is Ethernet PHY.	AR8033.17/ ADIN1300.16
J1.11		ENET_MDIO	GPIO1_IO17	Shared on SOM with "EC"; Signal after bidirectional open drain level translator; 3.3V level; Include 2.37K pull up on DART;	SOC.AH29
J1.12	No EC	ENET_RD1	GPIO1_IO27	Powered by NVCC_ENET pin	SOC.AG28
J1.12	EC	ETH_TRX2_N		Signal source is Ethernet PHY.	AR8033.18/ ADIN1300.17
J1.13		ENET_MDC	GPIO1_IO16	Shared on SOM with "EC"; Signal after bidirectional open drain level translator; 3.3V level;	SOC.AH28
J1.14	No EC	ENET_RD2	GPIO1_IO28	Powered by NVCC_ENET pin	SOC.AF29
J1.14	EC	ETH_TRX3_P		Signal source is Ethernet PHY.	AR8033.20/ ADIN1300.18
J1.15		NVCC_SNVS_1V8		1.8V Power output from SOM for SNVS domain; Valid with VBAT.	NVCC_SNVS_1V8
J1.16	No EC	ENET_RD3	GPIO1_IO29	Powered by NVCC_ENET pin	SOC.AF28
J1.16	EC	ETH_TRX3_N		Signal source is Ethernet PHY.	AR8033.21/ ADIN1300.19
J1.17		I2C4_SCL	GPIO5_IO20		SOC.AF8

PIN#	ASSY	BALL NAME	GPIO	NOTES	BALL
J1.18		GND		Digital Ground	GND
J1.19		I2C4_SDA	GPIO5_IO21		SOC.AD8
J1.20		ONOFF		SOC input with internal 100K PU; SNVS_1V8 level;	SOC.G22
J1.21		GND		Digital Ground	GND
J1.22		PMIC_RST_B		PMIC input to control SOM power rails and assertion of POR_B; Active-low input for triggering the system to cold or warm reset. Include 100K pull up to SNVS_1V8; On V1.0A engineering samples version this pin connected to SOC.F22 PMIC_ON_REQ. which cannot be pulled low externally and cannot be used for Cold reset externally.	PMIC.8
J1.23	NO WBD	NC		With "No WBD" or "No WB" configuration this pin in Not Connected.	NC
J1.23	WBD	BT_HOST_WAKE		Output from the LWB5 module; Signal level is 1.8V.	LWB5.46
J1.23	WB	BT_HOST_WAKE		Output from the LWB module; Signal level is 3.3V.	LWB.57
J1.24		POR_B		PMIC output (OD with PU) connected to SOC; Can be pulled low externally to cause warm reset. SNVS_1V8 level;	SOC.J29
J1.25	NO WBD	NC		With "No WBD" or "No WB" configuration this pin in Not Connected.	NC
J1.25	WBD	WIFI_HOST_WAKE		Output from the LWB5 module; Signal level is 1.8V.	LWB5.17
J1.25	WB	WIFI_HOST_WAKE		Output from the LWB module; Signal level is 3.3V.	LWB.131
J1.26		PMIC_STBY_REQ		SOC output; Can be used externally to control carrier board power for standby state; Active-high output for going to SUSPEND state; SNVS_1V8 level;	SOC.J24
J1.27		NVCC_3V3		Power output from SOM; Rises with last power rail; Can be used to control base board power.	NVCC_3V3
J1.28		SD2_RESET_B	GPIO2_IO19	Alt function "SD2_RESET_B" can be used to control the SD card power in order to perform SD RESET function; NVCC_SD2_1V8_3V3 level;	SOC.AD28
J1.29		SD1_RESET_B	GPIO2_IO10	Exposed for interfacing to WIFI & BT Host wake function OR as GPIO; Usage: SD1_RESET_B(CARRIER_WIFI_BT_HOST_WAKE) "WB": 3.3V Level; Other configurations 1V8 Level	SOC.W25
J1.30		GND		Digital Ground	GND
J1.31	No EC	NVCC_ENET		Power IN: supply power for ENET pins group	
J1.31	EC	NVCC_ENET		Power OUT: 1.8V from DART PHY - Leave floating!	
J1.32		NAND_DATA01	GPIO3_IO07_1V8	1.8V Level	SOC.L25
J1.33		GND		Digital Ground	GND
J1.34		NAND_CE0_B	GPIO3_IO01_1V8	1.8V Level	SOC.L26

PIN#	ASSY	BALL NAME	GPIO	NOTES	BALL
J1.35	No DSCM	DSI1_CLK_N		Two alternative location exist!	SOC.B18
J1.35	DSCM	NC		Pin not connected with DSCM configuration!	NC
J1.36		NC		Not Connected	NC
J1.37	No DSCM	DSI1_CLK_P		Two alternative location exist!	SOC.A18
J1.37	DSCM	NC		Pin not connected with DSCM configuration!	NC
J1.38		NAND_DQS	GPIO3_IO14_1V8	1.8V Level	SOC.R26
J1.39	No DSCM	DSI1_D0_N		Two alternative location exist!	SOC.B16
J1.39	DSCM	NC		Pin not connected with DSCM configuration!	NC
J1.40		NAND_ALE	GPIO3_IO00_1V8	1.8V Level	SOC.N25
J1.41	No DSCM	DSI1_D0_P		Two alternative location exist!	SOC.A16
J1.41	DSCM	NC		Pin not connected with DSCM configuration!	NC
J1.42	No DSCM	DSI1_D2_N		Two alternative location exist!	SOC.B19
J1.42	DSCM	NC		Pin not connected with DSCM configuration!	NC
J1.43	No DSCM	DSI1_D1_N		Two alternative location exist!	SOC.B17
J1.43	DSCM	NC		Pin not connected with DSCM configuration!	NC
J1.44	No DSCM	DSI1_D2_P		Two alternative location exist!	SOC.A19
J1.44	DSCM	NC		Pin not connected with DSCM configuration!	NC
J1.45	No DSCM	DSI1_D1_P		Two alternative location exist!	SOC.A17
J1.45	DSCM	NC		Pin not connected with DSCM configuration!	NC
J1.46		NAND_DATA03	GPIO3_IO09_1V8	1.8V Level	SOC.N24
J1.47		GPIO1_IO09	GPIO1_IO09		SOC.B8
J1.48		NAND_DATA00	GPIO3_IO06_1V8	1.8V Level	SOC.R25
J1.49		GND		Digital Ground	GND
J1.50		NAND_DATA02	GPIO3_IO08_1V8	1.8V Level	SOC.L24
J1.51		PCIE1_REF_CLK_N			SOC.E16
J1.52		GND		Digital Ground	GND
J1.53		PCIE1_REF_CLK_P			SOC.D16
J1.54		NC		Not Connected	NC
J1.55		GND		Digital Ground	GND
J1.56		NC		Not Connected	NC
J1.57		PCIE1_TX_N			SOC.B15
J1.58		GND		Digital Ground	GND
J1.59		PCIE1_TX_P			SOC.A15
J1.60		PCIE1_RX_N			SOC.B14
J1.61		GND		Digital Ground	GND
J1.62		PCIE1_RX_P			SOC.A14
J1.63		NC		Not Connected	NC
J1.64		GND		Digital Ground	GND
J1.65		NC		Not Connected	NC
J1.66	No DSCM	DSI1_D3_N		Two alternative location exist!	SOC.B20
J1.66	DSCM	NC		Pin not connected with DSCM configuration!	NC
J1.67		GND		Digital Ground	GND
J1.68	No DSCM	DSI1_D3_P		Two alternative location exist!	SOC.A20

PIN#	ASSY	BALL NAME	GPIO	NOTES	BALL
J1.68	DSCM	NC		Pin not connected with DSCM configuration!	NC
J1.69		CSI1_D3_P			SOC.D26
J1.70		GND		Digital Ground	GND
J1.71		CSI1_D3_N			SOC.E26
J1.72		BOOT_MODE3		PD in SOC;	SOC.G12
J1.73		CSI1_D1_P			SOC.D20
J1.74		SD2_CD_B	GPIO2_IO12	NVCC_SD2_1V8_3V3 level;	SOC.AD29
J1.75		CSI1_D1_N			SOC.E20
J1.76		GND		Digital Ground	GND
J1.77		CSI1_D2_N			SOC.E24
J1.78		SD2_DATA2	GPIO2_IO17	NVCC_SD2_1V8_3V3 level;	SOC.AA26
J1.79		CSI1_D2_P			SOC.D24
J1.80		SD2_DATA1	GPIO2_IO16	NVCC_SD2_1V8_3V3 level;	SOC.AC29
J1.81		CSI1_D0_P			SOC.D18
J1.82		SD2_CLK	GPIO2_IO13	NVCC_SD2_1V8_3V3 level;	SOC.AB29
J1.83		CSI1_D0_N			SOC.E18
J1.84		SD2_DATA3	GPIO2_IO18	NVCC_SD2_1V8_3V3 level;	SOC.AA25
J1.85		GND		Digital Ground	GND
J1.86		SD2_DATA0	GPIO2_IO15	NVCC_SD2_1V8_3V3 level;	SOC.AC28
J1.87		CSI1_CLK_P			SOC.D22
J1.88		SD2_CMD	GPIO2_IO14	NVCC_SD2_1V8_3V3 level;	SOC.AB28
J1.89		CSI1_CLK_N			SOC.E22
J1.90		NVCC_SD2_1V8_3V3		Power output from SOM; Power the SD2 interface IO pins; Will change 1.8V/3.3V according to SD capabilities.	NVCC_SD2_1V8_3V3

7.3.2 DART-MX8M-PLUS J2 Pin-out

Table 4: DART-MX8M-PLUS J2 Pinout

PIN#	ASSY	BALL NAME	GPIO	NOTES	BALL
J2.1		JTAG_TCK		Include PD of 8.2K Ohm	SOC.G18
J2.2	No AC	SAI3_RXD	GPIO4_IO30	With “AC” configuration do not alter PINMUX function.	SOC.AF18
J2.2	AC	HPLOUT		Signal source is Audio Codec.	WM8904.13
J2.3		JTAG_TMS			SOC.G14
J2.4	No AC	SAI3_TXC	GPIO5_IO00	With “AC” configuration do not alter PINMUX function.	SOC.AH19
J2.4	AC	HPROUT		Signal source is Audio Codec.	WM8904.15
J2.5		JTAG_MOD		Exposed on DT8m & DT8MM JTAG_TRST pin; PD 8.2K Ohm included on DART;	SOC.G20
J2.6	No AC	SAI3_RXFS	GPIO4_IO28	With “AC” configuration do not alter PINMUX function.	SOC.AJ19
J2.6	AC	HPOUTFB		Signal source is Audio Codec.	WM8904.14
J2.7		JTAG_TDI			SOC.G16
J2.8	No AC	SAI3_RXC	GPIO4_IO29	With “AC” configuration do not alter PINMUX function.	SOC.AJ18
J2.8	AC	LINEIN1_LP		Signal source is Audio Codec.	WM8904.26
J2.9		JTAG_TDO			SOC.F14
J2.10	No AC	SAI3_TXFS	GPIO4_IO31	With “AC” configuration do not alter PINMUX function.	SOC.AC16
J2.10	AC	LINEIN1_RP		Signal source is Audio Codec.	WM8904.24
J2.11		BOOT_MODE1		PD in SOC; Requires 4.7K pull up on Carrier;	SOC.F8
J2.12		AGND		Audio Ground	AGND
J2.13		BOOT_MODE2		PD in SOC; Connected on DT8M & DT8MM boot mode0 pin; For compatibility to DT8M and DT8MM include 4.7K pull down on Carrier;	SOC.G8
J2.14	No AC	SAI3_TXD	GPIO5_IO01	With “AC” configuration do not alter PINMUX function.	SOC.AH18
J2.14	AC	DMIC_CLK		Signal source is Audio Codec.	WM8904.1
J2.15		HDMI_DDC_SCL	GPIO3_IO26	3.3V levels	SOC.AC22
J2.16	No AC	SAI3_MCLK	GPIO5_IO02	With “AC” configuration do not alter PINMUX function.	SOC.AJ20
J2.16	AC	DMIC_DATA		Signal source is Audio Codec.	WM8904.27
J2.17		HDMI_DDC_SDA	GPIO3_IO27	3.3V levels	SOC.AF22
J2.18		GND		Digital Ground	GND
J2.19		HDMI_CEC	GPIO3_IO28	3.3V levels	SOC.AD22
J2.20	WBD	ECSPI2_MOSI	GPIO5_IO11	Used internally with "WBD"; Function can be released if Buffer disabled.	SOC.AJ21
J2.21		HDMI_HPD	GPIO3_IO29	3.3V levels	SOC.AE22
J2.22	WBD	ECSPI2_MISO	GPIO5_IO12	Used internally with "WBD"; Function can be released if Buffer disabled.	SOC.AH20
J2.23		GND		Digital Ground	GND

PIN#	ASSY	BALL NAME	GPIO	NOTES	BALL
J2.24	WBD	ECSPI2_SCLK	GPIO5_IO10	Used internally with "WBD"; Function can be released if Buffer disabled.	SOC.AH21
J2.25		EARC_P_UTIL		Equal to HDMI_AUX_P	SOC.AJ23
J2.26	WBD	ECSPI2_SS0	GPIO5_IO13	Used internally with "WBD"; Function can be released if Buffer disabled.	SOC.AJ22
J2.27		EARC_N_HPD		Equal to HDMI_AUX_N	SOC.AH22
J2.28		GPIO1_IO02	GPIO1_IO02	Alternate function of WDOG_B; Can be tied on Custom to: POR_B - for Warm reset PMIC_ON_REQ - for cold reset	SOC.B6
J2.29		HDMI_TX1_N			SOC.AJ26
J2.30		I2C2_SDA	GPIO5_IO17		SOC.AE8
J2.31		HDMI_TX1_P			SOC.AH26
J2.32		I2C2_SCL	GPIO5_IO16		SOC.AH6
J2.33		HDMI_TX0_P			SOC.AH25
J2.34		SAI5_RXFS	GPIO3_IO19	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AC14
J2.35		HDMI_TX0_N			SOC.AJ25
J2.36		SAI5_RXD0	GPIO3_IO21	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AE16
J2.37		NC		Not Connected	NC
J2.38		SAI5_RXD2	GPIO3_IO23	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AF16
J2.39		NC		Not Connected	NC
J2.40		SAI5_RXC	GPIO3_IO20	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AD14
J2.41		NVCC_SAI1_SAI5		Power output for SAI1_SAI5 pads; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	NVCC_SAI1_SAI5
J2.42		SAI5_RXD1	GPIO3_IO22	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AD16
J2.43		HDMI_TX2_P			SOC.AH27
J2.44		SAI5_RXD3	GPIO3_IO24	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AE14
J2.45		HDMI_TX2_N			SOC.AJ27
J2.46		SAI5_MCLK	GPIO3_IO25	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AF14
J2.47		GND		Digital Ground	GND
J2.48		SAI2_RXFS	GPIO4_IO21		SOC.AH17
J2.49		HDMI_TXC_P			SOC.AH24
J2.50		SAI2_RXC	GPIO4_IO22		SOC.AJ16
J2.51		HDMI_TXC_N			SOC.AJ24
J2.52		SAI2_TXFS	GPIO4_IO24		SOC.AJ17
J2.53		GND		Digital Ground	GND
J2.54		SAI2_MCLK	GPIO4_IO27		SOC.AJ15
J2.55		SAI1_RXFS	GPIO4_IO00	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AJ9
J2.56		SAI2_TXC	GPIO4_IO25		SOC.AH15

PIN#	ASSY	BALL NAME	GPIO	NOTES	BALL
J2.57		SAI1_RXC	GPIO4_IO01	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AH8
J2.58		SAI2_RXD0	GPIO4_IO23		SOC.AJ14
J2.59		SAI1_RXD1	GPIO4_IO03	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AF10
J2.60		SAI2_TXD0	GPIO4_IO26		SOC.AH16
J2.61		SAI1_RXD0	GPIO4_IO02	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AC10
J2.62		SAI1_RXD3	GPIO4_IO05	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AJ8
J2.63		SAI1_RXD2	GPIO4_IO04	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AH9
J2.64		SAI1_TXFS	GPIO4_IO10	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AF12
J2.65		SAI1_RXD4	GPIO4_IO06	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AD10
J2.66		SAI1_RXD6	GPIO4_IO08	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AH10
J2.67		SAI1_TXD1	GPIO4_IO13	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AJ10
J2.68		SAI1_RXD7	GPIO4_IO09	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AH12
J2.69		SAI1_RXD5	GPIO4_IO07	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AE10
J2.70		SAI1_TXD0	GPIO4_IO12	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AJ11
J2.71		SAI1_TXD5	GPIO4_IO17	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AH14
J2.72		SAI1_TXC	GPIO4_IO11	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AJ12
J2.73		SAI1_TXD3	GPIO4_IO15	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AD12
J2.74		SAI1_TXD4	GPIO4_IO16	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AH13
J2.75		GND		Digital Ground	GND
J2.76		SAI1_TXD7	GPIO4_IO19	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AJ13
J2.77		ECSPI1_SCLK	GPIO5_IO06		SOC.AF20
J2.78		SAI1_TXD2	GPIO4_IO14	Connected internally to boot logic input. **Drives BOOT_MODE0;** Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AH11
J2.79		ECSPI1_SS0	GPIO5_IO09		SOC.AE20
J2.80		SAI1_TXD6	GPIO4_IO18	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AC12
J2.81		ECSPI1_MISO	GPIO5_IO08		SOC.AD20
J2.82		SAI1_MCLK	GPIO4_IO20	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AE12
J2.83		ECSPI1_MOSI	GPIO5_IO07		SOC.AC20
J2.84		GND		Digital Ground	GND
J2.85		UART2_RXD	GPIO5_IO24		SOC.AF6

PIN#	ASSY	BALL NAME	GPIO	NOTES	BALL
J2.86		UART2_TXD	GPIO5_IO25		SOC.AH4
J2.87		UART3_RXD	GPIO5_IO26		SOC.AE6
J2.88		UART1_RXD	GPIO5_IO22	Used as debug UART on Variscite base board.	SOC.AD6
J2.89		UART3_TXD	GPIO5_IO27		SOC.AJ4
J2.90		UART1_TXD	GPIO5_IO23	Used as debug UART on Variscite base board.	SOC.AJ3

7.3.3 DART-MX8M-PLUS J3 Pin-out

Table 5: DART-MX8M-PLUS J3 Pinout

PIN#	ASSY	BALL NAME	GPIO	NOTES	BALL
J3.1		UART4_TXD	GPIO5_IO29		SOC.AH5
J3.2		LVDS0_D0_P			SOC.D29
J3.3		UART4_RXD	GPIO5_IO28		SOC.AJ5
J3.4		LVDS0_D0_N			SOC.E28
J3.5		LVDS0_D2_P			SOC.G29
J3.6		LVDS0_D1_P			SOC.E29
J3.7		LVDS0_D2_N			SOC.H28
J3.8		LVDS0_D1_N			SOC.F28
J3.9		GND		Digital Ground	GND
J3.10		GND		Digital Ground	GND
J3.11		LVDS0_CLK_P			SOC.F29
J3.12	No DSCM	LVDS1_D0_P			SOC.A26
J3.12	DSCM	DSI1_D0_P		Two alternative location exist!	SOC.A16
J3.13		LVDS0_CLK_N			SOC.G28
J3.14	No DSCM	LVDS1_D0_N			SOC.B26
J3.14	DSCM	DSI1_D0_N		Two alternative location exist!	SOC.B16
J3.15		GND		Digital Ground	GND
J3.16	No DSCM	LVDS1_D1_P			SOC.A27
J3.16	DSCM	DSI1_D1_P		Two alternative location exist!	SOC.A17
J3.17		LVDS0_D3_P			SOC.H29
J3.18	No DSCM	LVDS1_D1_N			SOC.B27
J3.18	DSCM	DSI1_D1_N		Two alternative location exist!	SOC.B17
J3.19		LVDS0_D3_N			SOC.J28
J3.20	No DSCM	LVDS1_D3_P			SOC.C29
J3.20	DSCM	DSI1_D3_P		Two alternative location exist!	SOC.A20
J3.21		GND		Digital Ground	GND
J3.22	No DSCM	LVDS1_D3_N			SOC.D28
J3.22	DSCM	DSI1_D3_N		Two alternative location exist!	SOC.B20
J3.23	No DSCM	LVDS1_CLK_P			SOC.A28
J3.23	DSCM	DSI1_D2_P		Two alternative location exist!	SOC.A19
J3.24		GND		Digital Ground	GND
J3.25	No DSCM	LVDS1_CLK_N			SOC.B28
J3.25	DSCM	DSI1_D2_N		Two alternative location exist!	SOC.B19
J3.26		USB2_VBUS		USB PHY power detect pin; 5V tolerant	SOC.D12

PIN#	ASSY	BALL NAME	GPIO	NOTES	BALL
J3.27		GND		Digital Ground	GND
J3.28		SPDIF_RX	GPIO5_IO04		SOC.AD18
J3.29	No DSCM	LVDS1_D2_N			SOC.C28
J3.29	DSCM	DSI1_CLK_N		Two alternative location exist!	SOC.B18
J3.30		GPIO1_IO11	GPIO1_IO11		SOC.D8
J3.31	No DSCM	LVDS1_D2_P			SOC.B29
J3.31	DSCM	DSI1_CLK_P		Two alternative location exist!	SOC.A18
J3.32		SPDIF_EXT_CLK	GPIO5_IO05		SOC.AC18
J3.33		GND		Digital Ground	GND
J3.34		GND		Digital Ground	GND
J3.35		USB2_RX_N			SOC.B12
J3.36		SPDIF_TX	GPIO5_IO03		SOC.AE18
J3.37		USB2_RX_P			SOC.A12
J3.38		GPIO1_IO15	GPIO1_IO15		SOC.B5
J3.39		GND		Digital Ground	GND
J3.40		GPIO1_IO13	GPIO1_IO13		SOC.A6
J3.41		USB2_TX_N			SOC.B13
J3.42		I2C3_SDA	GPIO5_IO19	5K internal PU included for backward compatibility;	SOC.AJ6
J3.43		USB2_TX_P			SOC.A13
J3.44		USB2_ID		USB PHY ID pin; No GPIO function. Requires kernel patches for using this pin; Usage not recommended;	SOC.E12
J3.45		GND		Digital Ground	GND
J3.46		I2C3_SCL	GPIO5_IO18	5K internal PU included for backward compatibility;	SOC.AJ7
J3.47		USB2_D_P			SOC.D14
J3.48		GPIO1_IO14	GPIO1_IO14		SOC.A4
J3.49		USB2_D_N			SOC.E14
J3.50		GPIO1_IO12	GPIO1_IO12		SOC.A5
J3.51		GND		Digital Ground	GND
J3.52		GPIO1_IO10	GPIO1_IO10		SOC.B7
J3.53		USB1_RX_N			SOC.B9
J3.54		GPIO1_IO07	GPIO1_IO07		SOC.F6
J3.55		USB1_RX_P			SOC.A9
J3.56		USB1_ID		USB PHY ID pin; No GPIO function. Requires kernel patches for using this pin; Usage not recommended;	SOC.B11
J3.57		GND		Digital Ground	GND
J3.58		GPIO1_IO06	GPIO1_IO06		SOC.A3
J3.59		USB1_TX_N			SOC.B10
J3.60		GPIO1_IO08	GPIO1_IO08		SOC.A8
J3.61		USB1_TX_P			SOC.A10
J3.62		GPIO1_IO05	GPIO1_IO05		SOC.B4
J3.63		GND		Digital Ground	GND

PIN#	ASSY	BALL NAME	GPIO	NOTES	BALL
J3.64		GPIO1_IO01	GPIO1_IO01		SOC.E8
J3.65		USB1_D_P		USB OTG capable	SOC.D10
J3.66		USB1_VBUS		USB PHY power detect pin; 5V tolerant	SOC.A11
J3.67		USB1_D_N		USB OTG capable	SOC.E10
J3.68		GND		Digital Ground	GND
J3.69		NC		Not Connected	NC
J3.70		CSI2_CLK_N			SOC.B23
J3.71		VBAT		SOM Power	VBAT
J3.72		CSI2_CLK_P			SOC.A23
J3.73		VBAT		SOM Power	VBAT
J3.74		GND		Digital Ground	GND
J3.75		VBAT		SOM Power	VBAT
J3.76		CSI2_D3_N			SOC.B21
J3.77		VBAT		SOM Power	VBAT
J3.78		CSI2_D3_P			SOC.A21
J3.79		VBAT		SOM Power	VBAT
J3.80		CSI2_D1_N			SOC.B24
J3.81		VBAT		SOM Power	VBAT
J3.82		CSI2_D1_P			SOC.A24
J3.83		VBAT		SOM Power	VBAT
J3.84		CSI2_D0_N			SOC.B25
J3.85		VBAT		SOM Power	VBAT
J3.86		CSI2_D0_P			SOC.A25
J3.87		VBAT		SOM Power	VBAT
J3.88		CSI2_D2_N			SOC.B22
J3.89		VBAT		SOM Power	VBAT
J3.90		CSI2_D2_P			SOC.A22

7.4 DART-MX8M-PLUS Connector Pin Mux

Table 6: DART-MX8M-PLUS J1 PINMUX

PIN	ASSY	BALL	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6
J1.1		SOC.A7	GPIO1_IO00	ENET_PHY_REF_CLK_ROOT		ISP_FL_TRIG_0		REF_CLK_32K	EXT_CLK1
J1.2	No EC	SOC.AE26	ENET_QOS_RGMII_TD1		SAI6_RXFS	PDM_BIT0		GPIO1_IO20	SD3_CD_B
J1.3	No EC	SOC.AF24	ENET_QOS_RGMII_TX_CTL		SAI6_MCLK	SPDIF1_OUT		GPIO1_IO22	SD3_D0
J1.4	No EC	SOC.AC25	ENET_QOS_RGMII_TD0		SAI6_RXC	PDM_CLK		GPIO1_IO21	SD3_WP
J1.5	No EC	SOC.AE24	ENET_QOS_RGMII_TXC	ENET_QOS_TX_ER	SAI7_TXD0			GPIO1_IO23	SD3_D1
J1.6	No EC	SOC.AF26	ENET_QOS_RGMII_TD2	ENET_QOS_TX_CLK_IN, ENET_QOS_REF_CLK_ROOT _OUT	SAI6_RXD0	PDM_BIT1		GPIO1_IO19	SD3_D7
J1.7	No EC	SOC.AE29	ENET_QOS_RGMII_RXC	ENET_QOS_RX_ER	SAI7_TXC	PDM_BIT2		GPIO1_IO25	SD3_D3
J1.8	No EC	SOC.AD24	ENET_QOS_RGMII_TD3		SAI6_TXC	PDM_BIT2		GPIO1_IO18	SD3_D6
J1.9	No EC	SOC.AE28	ENET_QOS_RGMII_RX_CTL		SAI7_TXFS	PDM_BIT3		GPIO1_IO24	SD3_D2
J1.10	No EC	SOC.AG29	ENET_QOS_RGMII_RD0		SAI7_RXD0	PDM_BIT1		GPIO1_IO26	SD3_D4
J1.11		SOC.AH29	ENET_QOS_MDIO		SAI6_TXFS	PDM_BIT3		GPIO1_IO17	SD3_D5
J1.12	No EC	SOC.AG28	ENET_QOS_RGMII_RD1		SAI7_RXFS	PDM_BIT0		GPIO1_IO27	SD3_RESET_B
J1.13		SOC.AH28	ENET_QOS_MDC		SAI6_TXD0			GPIO1_IO16	SD3_STROBE
J1.14	No EC	SOC.AF29	ENET_QOS_RGMII_RD2		SAI7_RXC	PDM_CLK		GPIO1_IO28	SD3_CLK
J1.16	No EC	SOC.AF28	ENET_QOS_RGMII_RD3		SAI7_MCLK	SPDIF1_IN		GPIO1_IO29	SD3_CMD
J1.17		SOC.AF8	I2C4_SCL	PWM2_OUT	PCIE1_CLKREQ_B	ECSPI2_MISO		GPIO5_IO20	
J1.19		SOC.AD8	I2C4_SDA	PWM1_OUT		ECSPI2_SS0		GPIO5_IO21	
J1.20		SOC.G22	ONOFF_1V8						
J1.24		SOC.J29	POR_B_1V8						
J1.26		SOC.J24	PMIC_STBY_REQ_1V8						
J1.28		SOC.AD28	SD2_RESET_B					GPIO2_IO19	SYSTEM_RESET

PIN	ASSY	BALL	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6
J1.29		SOC.W25	SD1_RESET_B	ENET1_TX_CLK_IN, ENET_REF_CLK_ROOT_OUT		I2C3_SCL	UART3_RTS_B	GPIO2_IO10	
J1.32		SOC.L25	NAND_D01_1V8	QSPI_A_D1_1V8	SAI3_TXFS_1V8	ISP_PRELIGHT_TRIG _0_1V8	UART4_TX_1V8	GPIO3_IO07_1V8	
J1.34		SOC.L26	NAND_CE0_B_1V8	QSPI_A_SS0_B_1V8	SAI3_TXD0_1V8	ISP_SHUTTER_TRIG _0_1V8	UART3_TX_1V8	GPIO3_IO01_1V8	
J1.35	No DSCM	SOC.B18	DSI1_CLK_N						
J1.37	No DSCM	SOC.A18	DSI1_CLK_P						
J1.38		SOC.R26	NAND_DQS_1V8	QSPI_A_DQS_1V8	SAI3_MCLK_1V8	ISP_SHUTTER_OPEN _0_1V8	I2C3_SCL_1V8	GPIO3_IO14_1V8	
J1.39	No DSCM	SOC.B16	DSI1_D0_N						
J1.40		SOC.N25	NAND_ALE_1V8	QSPI_A_SCLK_1V8	SAI3_TXC_1V8	ISP_FL_TRIG_0_1V8	UART3_RX_1V8	GPIO3_IO00_1V8	
J1.41	No DSCM	SOC.A16	DSI1_D0_P						
J1.42	No DSCM	SOC.B19	DSI1_D2_N						
J1.43	No DSCM	SOC.B17	DSI1_D1_N						
J1.44	No DSCM	SOC.A19	DSI1_D2_P						
J1.45	No DSCM	SOC.A17	DSI1_D1_P						
J1.46		SOC.N24	NAND_D03_1V8	QSPI_A_D3_1V8	SD3_WP_1V8	UART4_RTS_B_1V8	ISP_FL_TRIG_1_1V8	GPIO3_IO09_1V8	
J1.47		SOC.B8	GPIO1_IO09	ENET_QOS_1588_EVENT0_OUT	PWM2_OUT	ISP_SHUTTER_OPEN _1	SD3_RESET_B	SDMA2_EXT_EVENT0	
J1.48		SOC.R25	NAND_D00_1V8_1V8	QSPI_A_D0_1V8	SAI3_RXD0_1V8	ISP_FLASH_TRIG_0_1V8	UART4_RX_1V8	GPIO3_IO06_1V8	
J1.50		SOC.L24	NAND_D02_1V8	QSPI_A_D2_1V8	SD3_CD_B_1V8	UART4_CTS_B_1V8	I2C4_SDA_1V8	GPIO3_IO08_1V8	
J1.51		SOC.E16	PCIE1_REF_CLK_N						
J1.53		SOC.D16	PCIE1_REF_CLK_P						
J1.57		SOC.B15	PCIE1_TX_N						

PIN	ASSY	BALL	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6
J1.59		SOC.A15	PCIE1_TX_P						
J1.60		SOC.B14	PCIE1_RX_N						
J1.62		SOC.A14	PCIE1_RX_P						
J1.66	No DSCM	SOC.B20	DSI1_D3_N						
J1.68	No DSCM	SOC.A20	DSI1_D3_P						
J1.69		SOC.D26	CSI1_D3_P						
J1.71		SOC.E26	CSI1_D3_N						
J1.72		SOC.G12	BOOT_MODE3						
J1.73		SOC.D20	CSI1_D1_P						
J1.74		SOC.AD29	SD2_CD_B					GPIO2_IO12	
J1.75		SOC.E20	CSI1_D1_N						
J1.77		SOC.E24	CSI1_D2_N						
J1.78		SOC.AA26	SD2_D2		ECSPI2_SS0	SPDIF1_OUT	PDM_BIT2	GPIO2_IO17	
J1.79		SOC.D24	CSI1_D2_P						
J1.80		SOC.AC29	SD2_D1		I2C4_SCL	UART2_TX	PDM_BIT1	GPIO2_IO16	
J1.81		SOC.D18	CSI1_D0_P						
J1.82		SOC.AB29	SD2_CLK		ECSPI2_SCLK	UART4_RX		GPIO2_IO13	
J1.83		SOC.E18	CSI1_D0_N						
J1.84		SOC.AA25	SD2_D3		ECSPI2_MISO	SPDIF1_IN	PDM_BIT3	GPIO2_IO18	EARLY_RESET
J1.86		SOC.AC28	SD2_D0		I2C4_SDA	UART2_RX	PDM_BIT0	GPIO2_IO15	
J1.87		SOC.D22	CSI1_CLK_P						
J1.88		SOC.AB28	SD2_CMD		ECSPI2_MOSI	UART4_TX	PDM_CLK	GPIO2_IO14	
J1.89		SOC.E22	CSI1_CLK_N						

Table 7: DART-MX8M-PLUS J2 PINMUX

PIN	ASSY	BALL	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6
J2.1		SOC.G18	JTAG_TCK						
J2.2	No AC	SOC.AF18	SAI3_RXD0	SAI2_RXD3	SAI5_RXD0		UART2_RTS_B	GPIO4_IO30	PDM_BIT1
J2.3		SOC.G14	JTAG_TMS						
J2.4	No AC	SOC.AH19	SAI3_TXC	SAI2_TXD2	SAI5_RXD2	GPT1_CAPTURE1	UART2_TX	GPIO5_IO00	PDM_BIT2
J2.5		SOC.G20	JTAG_MODE						
J2.6	No AC	SOC.AJ19	SAI3_RXFS	SAI2_RXD1	SAI5_RXFS	SAI3_RXD1	SPDIF1_IN	GPIO4_IO28	PDM_BIT0
J2.7		SOC.G16	JTAG_TDI						
J2.8	No AC	SOC.AJ18	SAI3_RXC	SAI2_RXD2	SAI5_RXC	GPT1_CLK	UART2_CTS_B	GPIO4_IO29	PDM_CLK
J2.9		SOC.F14	JTAG_TDO						
J2.10	No AC	SOC.AC16	SAI3_TXFS	SAI2_TXD1	SAI5_RXD1	SAI3_TXD1	UART2_RX	GPIO4_IO31	PDM_BIT3
J2.11		SOC.F8	BOOT_MODE1						
J2.13		SOC.G8	BOOT_MODE2						
J2.14	No AC	SOC.AH18	SAI3_TXD0	SAI2_TXD3	SAI5_RXD3	GPT1_CAPTURE2	SPDIF1_EXT_CLK	GPIO5_IO01	BOOT_MODE5
J2.15		SOC.AC22	HDMI_DDC_SCL			I2C5_SCL	FLEXCAN1_TX	GPIO3_IO26	
J2.16	No AC	SOC.AJ20	SAI3_MCLK	PWM4_OUT	SAI5_MCLK		SPDIF1_OUT	GPIO5_IO02	SPDIF1_IN
J2.17		SOC.AF22	HDMI_DDC_SDA			I2C5_SDA	FLEXCAN1_RX	GPIO3_IO27	
J2.19		SOC.AD22	HDMI_CEC			I2C6_SCL	FLEXCAN2_TX	GPIO3_IO28	
J2.20	WBD	SOC.AJ21	ECSPI2_MOSI	UART4_TX	I2C3_SDA	SAI7_TXD0		GPIO5_IO11	
J2.21		SOC.AE22	HDMI_HPD	HDMI_HPD_O		I2C6_SDA	FLEXCAN2_RX	GPIO3_IO29	
J2.22	WBD	SOC.AH20	ECSPI2_MISO	UART4_CTS_B	I2C4_SCL	SAI7_MCLK	CLKO1	GPIO5_IO12	
J2.24	WBD	SOC.AH21	ECSPI2_SCLK	UART4_RX	I2C3_SCL	SAI7_TXC		GPIO5_IO10	
J2.25		SOC.AJ23	EARC_P_UTIL						
J2.26	WBD	SOC.AJ22	ECSPI2_SS0	UART4_RTS_B	I2C4_SDA		CLKO2	GPIO5_IO13	
J2.27		SOC.AH22	EARC_N_HPD						
J2.28		SOC.B6	GPIO1_IO02	WDOG1_WDOG_B		ISP_FLASH_TRIG_0		WDOG1_WDOG_ANY	
J2.29		SOC.AJ26	HDMI_TX1_N						
J2.30		SOC.AE8	I2C2_SDA	ENET_QOS_1588_EVENT1_OUT	SD3_WP	ECSPI1_SS0		GPIO5_IO17	
J2.31		SOC.AH26	HDMI_TX1_P						
J2.32		SOC.AH6	I2C2_SCL	ENET_QOS_1588_EVENT1_IN	SD3_CD_B	ECSPI1_MISO	ENET_QOS_1588_EVENT1_AUX_IN	GPIO5_IO16	
J2.33		SOC.AH25	HDMI_TX0_P						
J2.34		SOC.AC14	SAI5_RXFS	SAI1_TXD0	PWM4_OUT	I2C6_SCL		GPIO3_IO19	
J2.35		SOC.AJ25	HDMI_TX0_N						

PIN	ASSY	BALL	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6
J2.36		SOC.AE16	SAI5_RXD0	SAI1_TXD2	PWM2_OUT	I2C5_SCL	PDM_BIT0	GPIO3_IO21	
J2.38		SOC.AF16	SAI5_RXD2	SAI1_TXD4	SAI1_TXFS	SAI5_TXC	PDM_BIT2	GPIO3_IO23	FLEXCAN1_RX
J2.40		SOC.AD14	SAI5_RXC	SAI1_TXD1	PWM3_OUT	I2C6_SDA	PDM_CLK	GPIO3_IO20	
J2.42		SOC.AD16	SAI5_RXD1	SAI1_TXD3	SAI1_TXFS	SAI5_TXFS	PDM_BIT1	GPIO3_IO22	FLEXCAN1_TX
J2.43		SOC.AH27	HDMI_TX2_P						
J2.44		SOC.AE14	SAI5_RXD3	SAI1_TXD5	SAI1_TXFS	SAI5_TXD0	PDM_BIT3	GPIO3_IO24	FLEXCAN2_TX
J2.45		SOC.AJ27	HDMI_TX2_N						
J2.46		SOC.AF14	SAI5_MCLK	SAI1_TXC	PWM1_OUT	I2C5_SDA		GPIO3_IO25	FLEXCAN2_RX
J2.48		SOC.AH17	SAI2_RXFS	SAI5_TXFS	SAI5_TXD1	SAI2_RXD1	UART1_TX	GPIO4_IO21	PDM_BIT2
J2.49		SOC.AH24	HDMI_TXC_P						
J2.50		SOC.AJ16	SAI2_RXC	SAI5_TXC		FLEXCAN1_TX	UART1_RX	GPIO4_IO22	PDM_BIT1
J2.51		SOC.AJ24	HDMI_TXC_N						
J2.52		SOC.AJ17	SAI2_TXFS	SAI5_TXD1	ENET_QOS_1588_EVENT3_OUT	SAI2_TXD1	UART1_CTS_B	GPIO4_IO24	PDM_BIT2
J2.54		SOC.AJ15	SAI2_MCLK	SAI5_MCLK	ENET_QOS_1588_EVENT3_IN	FLEXCAN2_RX	ENET_QOS_1588_EVENT3_AUX_IN	GPIO4_IO27	SAI3_MCLK
J2.55		SOC.AJ9	SAI1_RXFS	SAI5_RXFS			ENET1_1588_EVENT0_IN	GPIO4_IO00	
J2.56		SOC.AH15	SAI2_TXC	SAI5_TXD2		FLEXCAN1_RX		GPIO4_IO25	PDM_BIT1
J2.57		SOC.AH8	SAI1_RXC	SAI5_RXC		PDM_CLK	ENET1_1588_EVENT0_OUT	GPIO4_IO01	
J2.58		SOC.AJ14	SAI2_RXD0	SAI5_TXD0	ENET_QOS_1588_EVENT2_OUT	SAI2_TXD1	UART1_RTS_B	GPIO4_IO23	PDM_BIT3
J2.59		SOC.AF10	SAI1_RXD1	SAI5_RXD1		PDM_BIT1	ENET1_1588_EVENT1_OUT	GPIO4_IO03	
J2.60		SOC.AH16	SAI2_TXD0	SAI5_TXD3	ENET_QOS_1588_EVENT2_IN	FLEXCAN2_TX	ENET_QOS_1588_EVENT2_AUX_IN	GPIO4_IO26	BOOT_MODE4
J2.61		SOC.AC10	SAI1_RXD0	SAI5_RXD0	SAI1_TXD1	PDM_BIT0	ENET1_1588_EVENT1_IN	GPIO4_IO02	
J2.62		SOC.AJ8	SAI1_RXD3	SAI5_RXD3		PDM_BIT3	ENET1_MDIO	GPIO4_IO05	
J2.63		SOC.AH9	SAI1_RXD2	SAI5_RXD2		PDM_BIT2	ENET1_MDC	GPIO4_IO04	
J2.64		SOC.AF12	SAI1_TXFS	SAI5_TXFS			ENET1_RGMII_RX_CTL	GPIO4_IO10	
J2.65		SOC.AD10	SAI1_RXD4	SAI6_TXC	SAI6_RXC		ENET1_RGMII_RD0	GPIO4_IO06	
J2.66		SOC.AH10	SAI1_RXD6	SAI6_TXFS	SAI6_RXFS		ENET1_RGMII_RD2	GPIO4_IO08	
J2.67		SOC.AJ10	SAI1_TXD1	SAI5_TXD1			ENET1_RGMII_TD1	GPIO4_IO13	
J2.68		SOC.AH12	SAI1_RXD7	SAI6_MCLK	SAI1_TXFS	SAI1_TXD4	ENET1_RGMII_RD3	GPIO4_IO09	
J2.69		SOC.AE10	SAI1_RXD5	SAI6_TXD0	SAI6_RXD0	SAI1_RXFS	ENET1_RGMII_RD1	GPIO4_IO07	
J2.70		SOC.AJ11	SAI1_TXD0	SAI5_TXD0			ENET1_RGMII_TD0	GPIO4_IO12	
J2.71		SOC.AH14	SAI1_TXD5	SAI6_RXD0	SAI6_TXD0		ENET1_RGMII_TXC	GPIO4_IO17	
J2.72		SOC.AJ12	SAI1_TXC	SAI5_TXC			ENET1_RGMII_RXC	GPIO4_IO11	
J2.73		SOC.AD12	SAI1_TXD3	SAI5_TXD3			ENET1_RGMII_TD3	GPIO4_IO15	
J2.74		SOC.AH13	SAI1_TXD4	SAI6_RXC	SAI6_TXC		ENET1_RGMII_TX_CTL	GPIO4_IO16	

PIN	ASSY	BALL	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6
J2.76		SOC.AJ13	SAI1_TXD7	SAI6_MCLK		PDM_CLK	ENET1_TX_ER	GPIO4_IO19	
J2.77		SOC.AF20	ECSPI1_SCLK	UART3_RX	I2C1_SCL	SAI7_RXFS		GPIO5_IO06	
J2.78		SOC.AH11	SAI1_TXD2	SAI5_TXD2			ENET1_RGMII_TD2	GPIO4_IO14	
J2.79		SOC.AE20	ECSPI1_SS0	UART3_RTS_B	I2C2_SDA	SAI7_TXFS		GPIO5_IO09	
J2.80		SOC.AC12	SAI1_TXD6	SAI6_RXFS	SAI6_TXFS		ENET1_RX_ER	GPIO4_IO18	
J2.81		SOC.AD20	ECSPI1_MISO	UART3_CTS_B	I2C2_SCL	SAI7_RXD0		GPIO5_IO08	
J2.82		SOC.AE12	SAI1_MCLK	SAI5_MCLK	SAI1_TXC		ENET1_TX_CLK_IN ENET_REF_CLK_ROOT_OUT	GPIO4_IO20	
J2.83		SOC.AC20	ECSPI1_MOSI	UART3_TX	I2C1_SDA	SAI7_RXC		GPIO5_IO07	
J2.85		SOC.AF6	UART2_RX	ECSPI3_MISO		GPT1_COMPARE3		GPIO5_IO24	
J2.86		SOC.AH4	UART2_TX	ECSPI3_SS0		GPT1_COMPARE2		GPIO5_IO25	
J2.87		SOC.AE6	UART3_RX	UART1_CTS_B	SD3_RESET_B	GPT1_CAPTURE2	FLEXCAN2_TX	GPIO5_IO26	
J2.88		SOC.AD6	UART1_RX	ECSPI3_SCLK				GPIO5_IO22	
J2.89		SOC.AJ4	UART3_TX	UART1_RTS_B	SD3_VSELECT	GPT1_CLK	FLEXCAN2_RX	GPIO5_IO27	
J2.90		SOC.AJ3	UART1_TX	ECSPI3_MOSI				GPIO5_IO23	

Table 8: DART-MX8M-PLUS J3 PINMUX

PIN	ASSY	BALL	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6
J3.1		SOC.AH5	UART4_TX	UART2_RTS_B		GPT1_CAPTURE1	I2C6_SDA	GPIO5_IO29	
J3.2		SOC.D29	LVDS0_D0_P						
J3.3		SOC.AJ5	UART4_RX	UART2_CTS_B	PCIE1_CLKREQ_B	GPT1_COMPARE1	I2C6_SCL	GPIO5_IO28	
J3.4		SOC.E28	LVDS0_D0_N						
J3.5		SOC.G29	LVDS0_D2_P						
J3.6		SOC.E29	LVDS0_D1_P						
J3.7		SOC.H28	LVDS0_D2_N						
J3.8		SOC.F28	LVDS0_D1_N						
J3.11		SOC.F29	LVDS0_CLK_P						
J3.12	No DSCM	SOC.A26	LVDS1_D0_P						
J3.12	DSCM	SOC.A16	DSI1_D0_P						
J3.13		SOC.G28	LVDS0_CLK_N						
J3.14	No DSCM	SOC.B26	LVDS1_D0_N						
J3.14	DSCM	SOC.B16	DSI1_D0_N						
J3.16	No DSCM	SOC.A27	LVDS1_D1_P						
J3.16	DSCM	SOC.A17	DSI1_D1_P						
J3.17		SOC.H29	LVDS0_D3_P						
J3.18	No DSCM	SOC.B27	LVDS1_D1_N						
J3.18	DSCM	SOC.B17	DSI1_D1_N						
J3.19		SOC.J28	LVDS0_D3_N						
J3.20	No DSCM	SOC.C29	LVDS1_D3_P						
J3.20	DSCM	SOC.A20	DSI1_D3_P						

PIN	ASSY	BALL	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6
J3.22	No DSCM	SOC.D28	LVDS1_D3_N						
J3.22	DSCM	SOC.B20	DSI1_D3_N						
J3.23	No DSCM	SOC.A28	LVDS1_CLK_P						
J3.23	DSCM	SOC.A19	DSI1_D2_P						
J3.25	No DSCM	SOC.B28	LVDS1_CLK_N						
J3.25	DSCM	SOC.B19	DSI1_D2_N						
J3.26		SOC.D12	USB2_VBUS						
J3.28		SOC.AD18	SPDIF1_IN	PWM2_OUT	I2C5_SDA	GPT1_COMPARE2	FLEXCAN1_RX	GPIO5_IO04	
J3.29	No DSCM	SOC.C28	LVDS1_D2_N						
J3.29	DSCM	SOC.B18	DSI1_CLK_N						
J3.30		SOC.D8	GPIO1_IO11	USB2_OTG_ID	PWM2_OUT		SD3_VSELECT		
J3.31	No DSCM	SOC.B29	LVDS1_D2_P						
J3.31	DSCM	SOC.A18	DSI1_CLK_P						
J3.32		SOC.AC18	SPDIF1_EXT_CLK	PWM1_OUT		GPT1_COMPARE3		GPIO5_IO05	
J3.35		SOC.B12	USB2_RX_N						
J3.36		SOC.AE18	SPDIF1_OUT	PWM3_OUT	I2C5_SCL	GPT1_COMPARE1	FLEXCAN1_TX	GPIO5_IO03	
J3.37		SOC.A12	USB2_RX_P						
J3.38		SOC.B5	GPIO1_IO15	USB2_OTG_OC			SD3_WP	PWM4_OUT	CLKO2
J3.40		SOC.A6	GPIO1_IO13	USB1_OTG_OC				PWM2_OUT	
J3.41		SOC.B13	USB2_TX_N						
J3.42		SOC.AJ6	I2C3_SDA	PWM3_OUT	GPT3_CLK	ECSPI2_MOSI		GPIO5_IO19	
J3.43		SOC.A13	USB2_TX_P						
J3.44		SOC.E12	USB2_ID						

PIN	ASSY	BALL	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6
J3.46		SOC.AJ7	I2C3_SCL	PWM4_OUT	GPT2_CLK	ECSPI2_SCLK		GPIO5_IO18	
J3.47		SOC.D14	USB2_D_P						
J3.48		SOC.A4	GPIO1_IO14	USB2_OTG_PWR			SD3_CD_B	PWM3_OUT	CLKO1
J3.49		SOC.E14	USB2_D_N						
J3.50		SOC.A5	GPIO1_IO12	USB1_OTG_PWR				SDMA2_EXT_EVENT1	
J3.52		SOC.B7	GPIO1_IO10	USB1_OTG_ID	PWM3_OUT				
J3.53		SOC.B9	USB1_RX_N						
J3.54		SOC.F6	GPIO1_IO07	ENET_QOS_MDIO		ISP_FLASH_TRIG_1		SD1_WP	EXT_CLK4
J3.55		SOC.A9	USB1_RX_P						
J3.56		SOC.B11	USB1_ID						
J3.58		SOC.A3	GPIO1_IO06	ENET_QOS_MDC		ISP_SHUTTER_TRIG_1		SD1_CD_B	EXT_CLK3
J3.59		SOC.B10	USB1_TX_N						
J3.60		SOC.A8	GPIO1_IO08	ENET_QOS_1588_EVENT0_IN	PWM1_OUT	ISP_PRELIGHT_TRIG_1	ENET_QOS_1588_EVENT0_AUX_IN	SD2_RESET_B	
J3.61		SOC.A10	USB1_TX_P						
J3.62		SOC.B4	GPIO1_IO05	M7_NMI		ISP_FL_TRIG_1		PMIC_READY	
J3.64		SOC.E8	GPIO1_IO01	PWM1_OUT		ISP_SHUTTER_TRIG_0		REF_CLK_24M	EXT_CLK2
J3.65		SOC.D10	USB1_D_P						
J3.66		SOC.A11	USB1_VBUS						
J3.67		SOC.E10	USB1_D_N						
J3.70		SOC.B23	CSI2_CLK_N						
J3.72		SOC.A23	CSI2_CLK_P						
J3.76		SOC.B21	CSI2_D3_N						
J3.78		SOC.A21	CSI2_D3_P						
J3.80		SOC.B24	CSI2_D1_N						
J3.82		SOC.A24	CSI2_D1_P						

PIN	ASSY	BALL	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6
J3.84		SOC.B25	CSI2_D0_N						
J3.86		SOC.A25	CSI2_D0_P						
J3.88		SOC.B22	CSI2_D2_N						
J3.90		SOC.A22	CSI2_D2_P						

8. SOM's Interfaces

8.1 Acronym for Section 8 Tables:

Table 9: Interface Tables Mnemonics

Column Heading		Meaning
PIN#	**Jx.YY**	Pin number on a connector: Jx: Can be J1 J2 or J3 YY: Can be 1 to 90
ALT NAME		Pin type & direction
ALT#		Alternate number for the function. Blank in case the function origin is a PHY pin.
NOTES		This column displays any special note related to the specific pin with the specific ASSY.
BALL	**XX.YY**	Source device and its pin number; See Table 2.

8.2 Trace Impedance

DART traces are designed with the below table impedance list per signal group.
Table is a reference when you are updating or creating constraints in the PCB design tool to set up the impedances/trace widths.

Table 10: DART Signal Group Traces Impedance

Signal Group	Impedance
All single ended signals	50 Ω Single ended
PCIe Clock, TX/RX data pairs	85 Ω Differential
USB Differential signals	90 Ω Differential
Differential signals including: Ethernet, MIPI (CSI and DSI), LVDS, HDMI	100 Ω Differential

8.3 Display Interfaces

the i.MX 8M Plus SoC has the following display support

- Three LCDIF Display Controllers:
  - One LCDIF drives MIPI DSI
  - One LCDIF drives LVDS Tx
  - One LCDIF drives HDMI Tx

Support up to 1080p60 display per LCDIF if no more than 2 instances used simultaneously, or 1x 1080p60 + 2x 720p60 if all 3 instances used simultaneously

The DART-MX8M-PLUS supports all display interfaces HDMI, MIPI DSI and LVDS display available by the i.MX 8M Plus SoC

8.3.1 HDMI

The following features are supported:

HDMI 2.0a Tx supporting one display

- Resolutions of: 740x480p60, 720x480p60, 1280x720p60, 1920x1080p60
- HDCP 2.2 and HDCP 1.4

Audio support

- 32 channel audio output support
- 1 S/PDIF audio eARC input support

8.3.1.1 HDMI Signals

Table 11: HDMI Signals

PIN#	ASSY	ALT NAME	ALT#	NOTES	BALL
J2.19		HDMI_CEC	0	3.3V levels Has other alternate functions;	SOC.AD22
J2.15		HDMI_DDC_SCL	0	3.3V levels Has other alternate functions;	SOC.AC22
J2.17		HDMI_DDC_SDA	0	3.3V levels Has other alternate functions;	SOC.AF22
J2.21		HDMI_HPD	0	3.3V levels Has other alternate functions;	SOC.AE22
J2.21		HDMI_HPD_O	1	3.3V levels Has other alternate functions;	SOC.AE22
J2.35		HDMI_TX0_N		Differential Pair Negative side Requires DC coupling to HDMI connector.	SOC.AJ25
J2.33		HDMI_TX0_P		Differential Pair Positive side Requires DC coupling to HDMI connector.	SOC.AH25
J2.29		HDMI_TX1_N		Differential Pair Negative side Requires DC coupling to HDMI connector.	SOC.AJ26
J2.31		HDMI_TX1_P		Differential Pair Positive side Requires DC coupling to HDMI connector.	SOC.AH26
J2.45		HDMI_TX2_N		Differential Pair Negative side Requires DC coupling to HDMI connector.	SOC.AJ27
J2.43		HDMI_TX2_P		Differential Pair Positive side Requires DC coupling to HDMI connector.	SOC.AH27
J2.51		HDMI_TXC_N		Differential Pair Negative side Requires DC coupling to HDMI connector.	SOC.AJ24
J2.49		HDMI_TXC_P		Differential Pair Positive side Requires DC coupling to HDMI connector.	SOC.AH24

Table 12: HDMI eARC Signals

PIN#	ASSY	ALT NAME	ALT#	NOTES	BALL
J2.25		EARC_P_UTIL	0	Differential Pair Positive side Equal to HDMI_AUX_P on DT8M	SOC.AJ23
J2.27		EARC_N_HPD	0	Differential Pair Negative side Equal to HDMI_AUX_N on DT8M	SOC.AH22

8.3.2 LVDS

he LVDS Display Bridge (LDB) connects the CPU internal LCDIF to External LVDS Display. The purpose of the LDB is to support flow of synchronous RGB data to external display devices through the LVDS interface.

The LVDS ports can be used as follows:

- Single channel (4 lanes) output at up to 80MHz pixel clock and LVDS clock. This supports resolutions up to 1366x768p60.
- Dual asynchronous channels (8 data, 2 clocks). This is intended for a single panel with two interfaces, transferring across two channels (even pixel/odd pixel). This is supported at up to 160MHz pixel clock, which is up to 80MHz LVDS clock (due to 2 pixels per LVDS clock). This supports resolutions above 1366x768p60, up to 1080p60.

The Pixel Mapper splits and reorders the pixels from the single LCDIF display output into an odd and even pixel stream. Splitting and reordering is required to match the LVDS Displays speed and channel requirements. Both VESA and JEIDA pixel mapping is supported.

8.3.2.1 LVDS0 Signals

Table 13: LVDS0 Signals

PIN#	ASSY	ALT NAME	ALT#	NOTES	BALL
J3.13		LVDS0_CLK_N	0	Differential Pair Negative side Always Exposed	SOC.G28
J3.11		LVDS0_CLK_P	0	Differential Pair Positive side Always Exposed	SOC.F29
J3.4		LVDS0_D0_N	0	Differential Pair Negative side Always Exposed	SOC.E28
J3.2		LVDS0_D0_P	0	Differential Pair Positive side Always Exposed	SOC.D29
J3.8		LVDS0_D1_N	0	Differential Pair Negative side Always Exposed	SOC.F28
J3.6		LVDS0_D1_P	0	Differential Pair Positive side Always Exposed	SOC.E29
J3.7		LVDS0_D2_N	0	Differential Pair Negative side Always Exposed	SOC.H28
J3.5		LVDS0_D2_P	0	Differential Pair Positive side Always Exposed	SOC.G29
J3.19		LVDS0_D3_N	0	Differential Pair Negative side Always Exposed	SOC.J28
J3.17		LVDS0_D3_P	0	Differential Pair Positive side Always Exposed	SOC.H29

8.3.2.2 LVDS1 Signals

Table 14: LVDS1 Signals

PIN#	ASSY	ALT NAME	ALT#	NOTES	BALL
J3.25	No DSCM	LVDS1_CLK_N	0	Differential Pair Negative side With DSCM exposes DSI	SOC.B28
J3.23	No DSCM	LVDS1_CLK_P	0	Differential Pair Positive side With DSCM exposes DSI	SOC.A28
J3.14	No DSCM	LVDS1_D0_N	0	Differential Pair Negative side With DSCM exposes DSI	SOC.B26
J3.12	No DSCM	LVDS1_D0_P	0	Differential Pair Positive side With DSCM exposes DSI	SOC.A26
J3.18	No DSCM	LVDS1_D1_N	0	Differential Pair Negative side With DSCM exposes DSI	SOC.B27
J3.16	No DSCM	LVDS1_D1_P	0	Differential Pair Positive side With DSCM exposes DSI	SOC.A27
J3.29	No DSCM	LVDS1_D2_N	0	Differential Pair Negative side With DSCM exposes DSI	SOC.C28
J3.31	No DSCM	LVDS1_D2_P	0	Differential Pair Positive side With DSCM exposes DSI	SOC.B29
J3.22	No DSCM	LVDS1_D3_N	0	Differential Pair Negative side With DSCM exposes DSI	SOC.D28
J3.20	No DSCM	LVDS1_D3_P	0	Differential Pair Positive side With DSCM exposes DSI	SOC.C29

8.3.3 DSI

The i.MX 8M Plus incorporates the MIPI DSI Host Controller.

The key features of the MIPI DSI include:

- Complies to MIPI DSI Standard Specification V1.01r11
  - Maximum resolution ranges up to WQHD (1920x1080p60, 24bpp)
    It should be decided on bandwidth between input clock (video clock) and output clock (D-PHY HS clock).
  - Supports 1, 2, 3, or 4 data lanes
  - Supports pixel format: 16bpp, 18bpp packed, 18bpp loosely packed (3 bytes format), and 24bpp
- Interfaces
  - Complies with Protocol-to-PHY Interface (PPI) in 1.0Gbps / 1.5Gbps MIPI DPHY
  - Supports RGB Interface for Video Image Input from general display controller

8.3.3.1 MIPI-DSI Signals Two Alternative Pinouts

DART-MX8M-PLUS exposes the MIPI-DSI on one of two alternative pinouts:

1. By default, MIPI-DSI will be exposed on a new pin location not compatible to DART-MX8M & DART-MX8M-MINI; With this option both LVDS channels and MIPI-DSI exposed.

2. With "***DSCM***" configuration the MIPI-DSI exposed instead of LVDS1 location; This will be compatible to DART-MX8M & DART-MX8M-MINI; With this option LVDS0 channel will still be exposed.

8.3.3.2 DSI Signals

Table 15: MIPI DSI Signals

PIN#	ASSY	ALT NAME	ALT#	NOTES	BALL
J1.35	No DSCM	DSI1_CLK_N	0	Differential Pair Negative side	SOC.B18
J1.37	No DSCM	DSI1_CLK_P	0	Differential Pair Positive side	SOC.A18
J1.39	No DSCM	DSI1_D0_N	0	Differential Pair Negative side	SOC.B16
J1.41	No DSCM	DSI1_D0_P	0	Differential Pair Positive side	SOC.A16
J1.43	No DSCM	DSI1_D1_N	0	Differential Pair Negative side	SOC.B17
J1.45	No DSCM	DSI1_D1_P	0	Differential Pair Positive side	SOC.A17
J1.42	No DSCM	DSI1_D2_N	0	Differential Pair Negative side	SOC.B19
J1.44	No DSCM	DSI1_D2_P	0	Differential Pair Positive side	SOC.A19
J1.66	No DSCM	DSI1_D3_N	0	Differential Pair Negative side	SOC.B20
J1.68	No DSCM	DSI1_D3_P	0	Differential Pair Positive side	SOC.A20
J3.29	DSCM	DSI1_CLK_N	0	Differential Pair Negative side	SOC.B18
J3.31	DSCM	DSI1_CLK_P	0	Differential Pair Positive side	SOC.A18
J3.14	DSCM	DSI1_D0_N	0	Differential Pair Negative side	SOC.B16
J3.12	DSCM	DSI1_D0_P	0	Differential Pair Positive side	SOC.A16
J3.18	DSCM	DSI1_D1_N	0	Differential Pair Negative side	SOC.B17
J3.16	DSCM	DSI1_D1_P	0	Differential Pair Positive side	SOC.A17
J3.25	DSCM	DSI1_D2_N	0	Differential Pair Negative side	SOC.B19
J3.23	DSCM	DSI1_D2_P	0	Differential Pair Positive side	SOC.A19
J3.22	DSCM	DSI1_D3_N	0	Differential Pair Negative side	SOC.B20
J3.20	DSCM	DSI1_D3_P	0	Differential Pair Positive side	SOC.A20

8.4 Camera Interface

8.4.1 MIPI CSI-2

The DART-MX8M-PLUS consists of 2x MIPI CSI-2 Host Controller which implements the protocol functions defined in the MIPI CSI-2 specification, allowing communication with an MIPI CSI-2 compliant camera sensor.

The MIPI CSI-2 controller supports the following features:

- MIPI D-PHY specification V1.2 (Board Approved)
- Compliant to MIPI CSI2 Specification V1.3 except for C-PHY feature (Board Approved)
- Support primary and secondary Image format
  - YUV420, YUV420 (Legacy), YUV420 (CSPS), YUV422 of 8-bits and 10-bits
  - RGB565, RGB666, RGB888
  - RAW6, RAW7, RAW8, RAW10, RAW12, RAW14
  - All of User defined Byte-based Data packet
- Support up to 4 lanes of D-PHY operating up to a maximum bit rate of 1.5 Gbps
- Interfaces
  - Compatible to PPI (Protocol-to-PHY Interface) in MIPI D-PHY Specification
  - AMBA3.0 APB Slave for Register configuration.
  - Image output data bus width: 32 bits
- Image memory size of SRAM is 4KB
- Pixel clock can be gated when no PPI data is coming

8.4.1.1 MIPI-CSI2 #1 Signals

Table 16: MIPI-CSI2 #1 Signals

PIN#	ASSY	ALT NAME	ALT#	NOTES	BALL
J1.89		CSI1_CLK_N	0	Differential Pair Negative side	SOC.E22
J1.87		CSI1_CLK_P	0	Differential Pair Positive side	SOC.D22
J1.83		CSI1_D0_N	0	Differential Pair Negative side	SOC.E18
J1.81		CSI1_D0_P	0	Differential Pair Positive side	SOC.D18
J1.75		CSI1_D1_N	0	Differential Pair Negative side	SOC.E20
J1.73		CSI1_D1_P	0	Differential Pair Positive side	SOC.D20
J1.77		CSI1_D2_N	0	Differential Pair Negative side	SOC.E24
J1.79		CSI1_D2_P	0	Differential Pair Positive side	SOC.D24
J1.71		CSI1_D3_N	0	Differential Pair Negative side	SOC.E26
J1.69		CSI1_D3_P	0	Differential Pair Positive side	SOC.D26

8.4.1.2 MIPI-CSI2 #2 Signals

Table 17: MIPI-CSI2 #2 Signals

PIN#	ASSY	ALT NAME	ALT#	NOTES	BALL
J3.70		CSI2_CLK_N	0	Differential Pair Negative side	SOC.B23
J3.72		CSI2_CLK_P	0	Differential Pair Positive side	SOC.A23
J3.84		CSI2_D0_N	0	Differential Pair Negative side	SOC.B25
J3.86		CSI2_D0_P	0	Differential Pair Positive side	SOC.A25
J3.80		CSI2_D1_N	0	Differential Pair Negative side	SOC.B24
J3.82		CSI2_D1_P	0	Differential Pair Positive side	SOC.A24
J3.88		CSI2_D2_N	0	Differential Pair Negative side	SOC.B22
J3.90		CSI2_D2_P	0	Differential Pair Positive side	SOC.A22
J3.76		CSI2_D3_N	0	Differential Pair Negative side	SOC.B21
J3.78		CSI2_D3_P	0	Differential Pair Positive side	SOC.A21

8.4.2 ISP

The Image Signal Processors (ISP) receive an image from the camera sensor and converts it from raw Bayer to YUV so it can be processed by the chip. The ISP also provides additional processing to improve the image quality. Supported image quality processes include:

- HDR to retain image details in high contrast scenes
- Dewarp to correct the image geometry caused by lens distortion (e.g. fisheye lens)
- Image enhancements (e.g. AWB, Denoise, AE, etc)

There are two instances of ISP on the chip and each is connected to separate instances of MIPI CSI. Both ISP instances support YCbCr420, YCbCR422, RAW8, RAW10, and RAW12 output pixel formats.

8.4.2.1 High-Dynamic Range (HDR)

The ISP supports the following HDR generation for high-quality on-the-fly dynamic range compression (DRC):

- Native HDR Sensor with compound output (max 14-bit compressed input)
- Digital Overlap High-Dynamic Range Sensor (DOL-HDR), staggered HDR For Native HDR sensors, the multi-exposure stitching is done internally and has line buffers.

Table 18: ISP0 & ISP1 Signals

PIN#	ASSY	ALT NAME	ALT#	NOTES	BALL
J1.1		ISP_FL_TRIG_0	3		SOC.A7
J1.40		ISP_FL_TRIG_0_1V8	3	1.8V Level	SOC.N25
J3.62		ISP_FL_TRIG_1	3		SOC.B4
J1.46		ISP_FL_TRIG_1_1V8	4	1.8V Level	SOC.N24
J2.28		ISP_FLASH_TRIG_0	3	Alternate function of WDOG_B;	SOC.B6
J1.48		ISP_FLASH_TRIG_0_1V8	3	1.8V Level	SOC.R25
J3.54		ISP_FLASH_TRIG_1	3		SOC.F6
J1.32		ISP_PRELIGHT_TRIG_0_1V8	3	1.8V Level	SOC.L25
J3.60		ISP_PRELIGHT_TRIG_1	3		SOC.A8
J1.38		ISP_SHUTTER_OPEN_0_1V8	3	1.8V Level	SOC.R26
J1.47		ISP_SHUTTER_OPEN_1	3		SOC.B8
J3.64		ISP_SHUTTER_TRIG_0	3		SOC.E8
J1.34		ISP_SHUTTER_TRIG_0_1V8	3	1.8V Level	SOC.L26
J3.58		ISP_SHUTTER_TRIG_1	3		SOC.A3

8.5 Ethernet Interface

The iMX 8M Plus implements Two Ethernet controllers both capable of simultaneous operation.

ENET_QOS (Ethernet Quality of Service) - Gigabit Ethernet controller based on Synopsys Proprietary with support for TSN (time-sensitive networking) in addition to EEE, Ethernet AVB, and IEEE 1588

ENET1 - Gigabit Ethernet controller with support for Energy Efficient Ethernet (EEE), Ethernet AVB (Audio Video Bridging, IEEE 802.1Qav), and IEEE 1588 time-stamping module which provides accurate clock synchronization for distributed control nodes for industrial automation applications.

8.5.1 ENET_QOS (Ethernet Quality of Service)

The SOM can be ordered in one of the following configurations:

- **"EC" configuration** – The DART-MX8M-PLUS includes an on SOM a Gigabit PHY (Atheros AR8033/Analog Devices ADIN1300) connected to ENET_QOS RGMII interface signals. External connector and magnetics should be implemented on carrier board to complete the interface to the media.

  "no EC" configuration - The DART-MX8M-PLUS exposes the ENET_QOS RGMII/RMII interface signals to the connector and ENET_QOS pins are referenced to pin J1.31 NVCC_ENET. Reference voltage should be supplied to pin J1.31:
  For RMII – 1.8V/3.3, For RGMII - 1.8V.

8.5.1.1 Ethernet PHY

The on SOM Atheros AR8033 / Analog Devices ADIN1300 Gigabit PHY in conjunction with external magnetics on carrier board complete the interface to the media.

The Following External Gigabit magnetics are required to complete the Ethernet PHY interface to the media.

Table 19: Gigabit Ethernet Magnetics

Vendor	P/N	Package	Cores	Configuration
Pulse	H5007NL	Transformer	8	Auto-MDX
TDK	TLA-7T101LF	Transformer	8	Auto-MDX
Pulse	J0G-0009NL	Integrated RJ45	8	Auto-MDX

Table 20: Ethernet PHY Signals

PIN#	ASSY	ALT NAME	ALT#	NOTES	BALL
J1.9	EC	ETH_LED_ACT		Signal source is Ethernet PHY.	AR8033.23/ ADIN1300.21 (via inv. FET)
J1.5	EC	ETH_LED_LINK10_100		Signal source is Ethernet PHY.	AR8033.26/ GND
J1.7	EC	ETH_LED_LINK1000		Signal source is Ethernet PHY.	AR8033.24/ ADIN1300.26 (via level shifter)
J1.6	EC	ETH_TRX0_N		Differential Pair Negative side Signal source is Ethernet PHY.	AR8033.12/ ADIN1300.13
J1.8	EC	ETH_TRX0_P		Differential Pair Positive side Signal source is Ethernet PHY.	AR8033.11/ ADIN1300.12
J1.4	EC	ETH_TRX1_N		Differential Pair Negative side Signal source is Ethernet PHY.	AR8033.15/ ADIN1300.15
J1.2	EC	ETH_TRX1_P		Differential Pair Positive side Signal source is Ethernet PHY.	AR8033.14/ ADIN1300.14
J1.12	EC	ETH_TRX2_N		Differential Pair Negative side Signal source is Ethernet PHY.	AR8033.18/ ADIN1300.17
J1.10	EC	ETH_TRX2_P		Differential Pair Positive side Signal source is Ethernet PHY.	AR8033.17/ ADIN1300.16
J1.16	EC	ETH_TRX3_N		Differential Pair Negative side Signal source is Ethernet PHY.	AR8033.21/ ADIN1300.19
J1.14	EC	ETH_TRX3_P		Differential Pair Positive side Signal source is Ethernet PHY.	AR8033.20/ ADIN1300.18

Table 21: Ethernet PHY LED Behavior

AR8033 Ethernet PHY LED Behavior

Symbol	10M link	10M active	100M link	100M active	1000M link	1000M active
LED_LINK_10_100	OFF	OFF	ON	ON	OFF	OFF
LED_LINK_1000	OFF	OFF	OFF	OFF	ON	ON
LED_ACT	ON	BLINK	ON	BLINK	ON	BLINK
ON = active; OFF = inactive						

ADIN1300 Ethernet PHY LED Behavior

Symbol	10M link	10M active	100M link	100M active	1000M link	1000M active
LED_LINK_10_100	OFF	OFF	OFF	OFF	OFF	OFF
LED_LINK_1000	ON	ON	ON	ON	ON	ON
LED_ACT	ON	BLINK	ON	BLINK	ON	BLINK
ON = active; OFF = inactive						

8.5.1.2 ENET_QOS Signals

Table 22: ENET_QOS Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J1.1		ENET_PHY_REF_CLK_ROOT	1		SOC.A7
J3.60		ENET_QOS_1588_EVENT0_AUX_IN	4		SOC.A8
J3.60		ENET_QOS_1588_EVENT0_IN	1		SOC.A8
J1.47		ENET_QOS_1588_EVENT0_OUT	1		SOC.B8
J2.32		ENET_QOS_1588_EVENT1_AUX_IN	4		SOC.AH6
J2.32		ENET_QOS_1588_EVENT1_IN	1		SOC.AH6
J2.30		ENET_QOS_1588_EVENT1_OUT	1		SOC.AE8
J2.60		ENET_QOS_1588_EVENT2_AUX_IN	4		SOC.AH16
J2.60		ENET_QOS_1588_EVENT2_IN	2		SOC.AH16
J2.58		ENET_QOS_1588_EVENT2_OUT	2		SOC.AJ14
J2.54		ENET_QOS_1588_EVENT3_AUX_IN	4		SOC.AJ15
J2.54		ENET_QOS_1588_EVENT3_IN	2		SOC.AJ15
J2.52		ENET_QOS_1588_EVENT3_OUT	2		SOC.AJ17
J1.13		ENET_QOS_MDC	0	Shared on SOM with "EC"; Signal after bidirectional open drain level translator; 3.3V level; Do not alter pinmux with "EC" configuration	SOC.AH28
J3.58		ENET_QOS_MDC	1		SOC.A3
J1.11		ENET_QOS_MDIO	0	Shared on SOM with "EC"; Signal after bidirectional open drain level translator; 3.3V level; Include 2.37K pull up on DART; Do not alter pinmux with "EC" configuration	SOC.AH29
J3.54		ENET_QOS_MDIO	1		SOC.F6
J1.10	No EC	ENET_QOS_RGMII_RD0	0	Powered by NVCC_ENET pin RGMII Data in	SOC.AG29
J1.12	No EC	ENET_QOS_RGMII_RD1	0	Powered by NVCC_ENET pin RGMII Data in	SOC.AG28
J1.14	No EC	ENET_QOS_RGMII_RD2	0	Powered by NVCC_ENET pin RGMII Data in	SOC.AF29
J1.16	No EC	ENET_QOS_RGMII_RD3	0	Powered by NVCC_ENET pin RGMII Data in	SOC.AF28
J1.9	No EC	ENET_QOS_RGMII_RX_CTL	0	Powered by NVCC_ENET pin RGMII Receive data Control	SOC.AE28
J1.7	No EC	ENET_QOS_RGMII_RXC	0	Powered by NVCC_ENET pin; Includes series EMI filter ENET RGMII Receive Clock: 125MHz @ 1000Mbps / 25MHz @ 100Mbps / 2.5MHz @ 10Mbps Samples RD[3:0] and RX_CTL	SOC.AE29
J1.4	No EC	ENET_QOS_RGMII_TD0	0	Powered by NVCC_ENET pin RGMII Data out	SOC.AC25
J1.2	No EC	ENET_QOS_RGMII_TD1	0	Powered by NVCC_ENET pin RGMII Data out	SOC.AE26
J1.6	No EC	ENET_QOS_RGMII_TD2	0	Powered by NVCC_ENET pin RGMII Data out	SOC.AF26
J1.8	No EC	ENET_QOS_RGMII_TD3	0	Powered by NVCC_ENET pin RGMII Data out	SOC.AD24

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J1.3	No EC	ENET_QOS_RGMII_TX_CTL	0	Powered by NVCC_ENET pin RGMII Transmit data Control	SOC.AF24
J1.5	No EC	ENET_QOS_RGMII_TXC	0	Powered by NVCC_ENET pin; Includes series EMI filter ENET RGMII Transmit Clock: 125MHz @ 1000Mbps / 25MHz @ 100Mbps / 2.5MHz @ 10Mbps Samples TD [3:0] and TX_CTL	SOC.AE24
J1.7	No EC	ENET_QOS_RX_ER	1	Powered by NVCC_ENET pin; Includes series EMI filter	SOC.AE29
J1.6	No EC	ENET_QOS_TX_CLK_IN ENET_QOS_REF_CLK_ROOT_OUT	1	Powered by NVCC_ENET pin RMII clock - can be used in 2 schemes: • MAC generates output 50M reference clock for PHY, also MAC uses this 50M clock. • MAC uses external 50M clock.	SOC.AF26
J1.5	No EC	ENET_QOS_TX_ER	1	Powered by NVCC_ENET pin; Includes series EMI filter	SOC.AE24

8.5.2 ENET1

ENET1 RGMII/RMII interface signals are always exported.
Signals, in conjunction to MDIO signals exported from connectors, can be used to interface an external Ethernet PHY or ethernet switch.

NOTE

ENET1 signals (with pad names SAI1_*) signal levels are referenced to **J2.41 (NVCC_SAI1_SAI5).** **See section 8.21.1.1**

8.5.2.1 ENET1 Signals

Table 23: ENET1 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.55		ENET1_1588_EVENT0_IN	4	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AJ9
J2.57		ENET1_1588_EVENT0_OUT	4	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AH8
J2.61		ENET1_1588_EVENT1_IN	4	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AC10
J2.59		ENET1_1588_EVENT1_OUT	4	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AF10
J2.63		ENET1_MDC	4	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AH9
J2.62		ENET1_MDIO	4	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AJ8
J2.65		ENET1_RGMII_RD0	4	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AD10
J2.69		ENET1_RGMII_RD1	4	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AE10
J2.66		ENET1_RGMII_RD2	4	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AH10
J2.68		ENET1_RGMII_RD3	4	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AH12
J2.64		ENET1_RGMII_RX_CTL	4	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AF12
J2.72		ENET1_RGMII_RXC	4	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AJ12
J2.70		ENET1_RGMII_TD0	4	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AJ11
J2.67		ENET1_RGMII_TD1	4	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AJ10
J2.78		ENET1_RGMII_TD2	4	Connected internally to boot logic input. **Drives BOOT_MODE0;** Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AH11
J2.73		ENET1_RGMII_TD3	4	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AD12
J2.74		ENET1_RGMII_TX_CTL	4	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AH13

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.71		ENET1_RGMII_TXC	4	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AH14
J2.80		ENET1_RX_ER	4	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AC12
J1.29		ENET1_TX_CLK_IN ENET_REF_CLK_ROOT_OUT	1	WBD: 1V8 Level; WB: 3.3V Level	SOC.W25
J2.82		ENET1_TX_CLK_IN ENET_REF_CLK_ROOT_OUT	4	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AE12
J2.76		ENET1_TX_ER	4	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AJ13

8.6 Wi-Fi & BT

The DART-MX8M-PLUS contains a certified high-performance Wi-Fi (Single or Dual Band option) and Bluetooth (BT) module:

- IEEE 802.11 ac/a/b/g/n (Dual Band Option)
- IEEE 802.11 b/g/n (Single Band Option)
- Bluetooth 2.1+EDR
- BLE 4.2 capabilities
- Modules have an antenna connection through a U. FL JACK connector
- Antenna cable connected to module must have 50-Ω impedance

Figure 3 illustrates the DART-MX8M-PLUS internal Wi-Fi and BT connectivity.

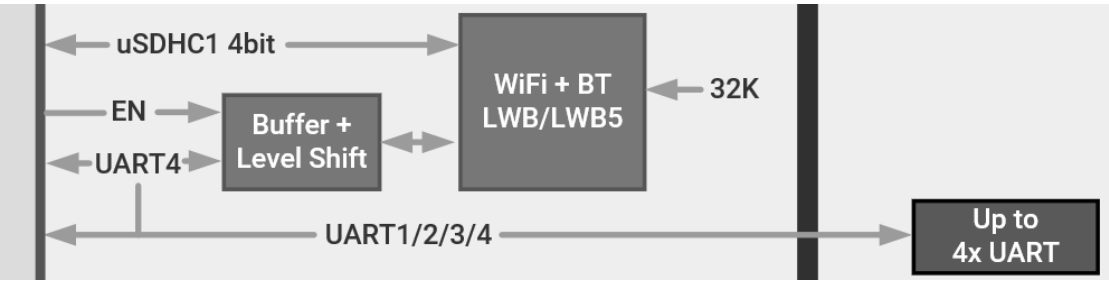


Figure 3: DART-MX8M-PLUS Wi-Fi & BT Internal Connection

To allow the most flexible solution the following elements are added to the DART-MX8M-PLUS:

- Buffer with tristate on the BT link based on UART interface.
  Will allow isolation from the BT module and the use by external circuity via the DART-MX8M-PLUS connector.
- Dedicated uSDHC channel for the Wi-Fi module interface.

NOTE

BT UART tristate buffer controlled using GPIO2_IO09.

- Logic "Low" enables the buffer.
- Logic "High" disable it and releases the signals to be used via DART connector.

8.6.1 Interface Implementation Options

8.6.1.1 Module Configuration with "WBD" or "WB" Option

- System use: Wi-Fi and Bluetooth.
  - BT UART external interface pins should be left floating.
- System use: **Wi-Fi and no BT**.
  - In this case, disable the BT buffer and BT function.
  - BT UART interface pins can be used externally with any of the alternate functions.
- System use: **BT and no Wi-Fi.**
  - Disable Wi-Fi function.
  - Enable the BT buffer and BT function.

8.6.1.2 Module Configuration without "WBD" or "WB" Option

- System use: **no Wi-Fi and no BT**.
  - BT UART interface accessible externally with any of its alternative functions. Buffer not included on module.

8.6.2 Bluetooth Interface Signals

Table 24: BT UART Interface Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.20	WBD/WB	UART4_TX	1	Used internally with "WBD" or "WB"; Function can be released if Buffer disabled. Always exposed;	SOC.AJ21
J2.22	WBD/WB	UART4_CTS_B	1	Used internally with "WBD" or "WB"; Function can be released if Buffer disabled. Always exposed;	SOC.AH20
J2.24	WBD/WB	UART4_RX	1	Used internally with "WBD" or "WB"; Function can be released if Buffer disabled.	SOC.AH21
J2.26	WBD/WB	UART4_RTS_B	1	Used internally with "WBD" or "WB"; Function can be released if Buffer disabled. Always exposed;	SOC.AJ22

8.6.3 WIFI & BT Host Wake Signals

Table 25: Host wake Interface Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J1.23	WBD	BT_HOST_WAKE		Output from the LWB5 module; Signal level is 1.8V.	LWB5.46
J1.23	WB	BT_HOST_WAKE		Output from the LWB module; Signal level is 3.3V.	LWB.57
J1.25	WBD	WIFI_HOST_WAKE		Output from the LWB5 module; Signal level is 1.8V.	LWB5.17
J1.25	WB	WIFI_HOST_WAKE		Output from the LWB module; Signal level is 3.3V.	LWB.131
J1.29		SD1_RESET_B	0	Exposed for interfacing to WIFI & BT Host wake function OR as GPIO; Usage: SD1_RESET_B(CARRIER_WIFI_BT_HOST_WAKE) "WB": 3.3V Level; Other configurations 1V8 Level	SOC.W25

8.7 Ultra-Secured Digital Host Controller

The DART-MX8M-PLUS exposes the uSDHC2 controller 4-bit interface for supporting interface between the host system and the SD/SDIO/MMC cards.
Key features of uSDHC2:

- SD/SDIO standard, up to version 3.0.
- MMC standard, up to version 5.1.
- 1.8 V and 3.3 V operation
- 1-bit/4-bit SD and SDIO modes, 1-bit/4-bit MMC mode
- Up to SDR104 rate

8.7.1 uSDHC1 Signals

uSDHC controller, uSDHC1, is used internally for the Wi-Fi SDIO interface on the SOM as 4-bits, other interface signals used for DART internal controls.

8.7.2 uSDHC2 Signals

Table 26: uSDHC2 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J1.90		NVCC_SD2_1V8_3V3		Power output from SOM; Power the SD2 interface IO pins; Will change 1.8V/3.3V according to SD capabilities. Use for PU resistor on SD2_CD_B and SD2_CMD lines.	
J1.74		SD2_CD_B	0	NVCC_SD2_1V8_3V3 level;	SOC.AD29
J1.82		SD2_CLK	0	NVCC_SD2_1V8_3V3 level;	SOC.AB29
J1.88		SD2_CMD	0	NVCC_SD2_1V8_3V3 level;	SOC.AB28
J1.86		SD2_D0	0	NVCC_SD2_1V8_3V3 level;	SOC.AC28
J1.80		SD2_D1	0	NVCC_SD2_1V8_3V3 level;	SOC.AC29
J1.78		SD2_D2	0	NVCC_SD2_1V8_3V3 level;	SOC.AA26
J1.84		SD2_D3	0	NVCC_SD2_1V8_3V3 level;	SOC.AA25
J1.28		SD2_RESET_B	0	Alt function "SD2_RESET_B" can be used to control the SD card power in order to perform SD RESET function; NVCC_SD2_1V8_3V3 level;	SOC.AD28
J3.60		SD2_RESET_B	5		SOC.A8

8.7.3 uSDHC3 Signals

uSDHC controller, uSDHC3, is used internally for the eMMC interface on the SOM.
Not exposed externally.

8.8 USB 3.0

The DART-MX8M-PLUS consists Two USB controllers and PHYs that support USB 3.0 and 2.0.

Each USB 3.0 module includes the following features:

- Up to SDR104 rate
- Complies with USB specification rev 3.0 (xHCI compatible)
- Supports operation as a standalone USB host controller
  USB dual-role operation and can be configured as host or device
- Super-speed (5 Gbit/s), high-speed (480 Mbit/s), full-speed (12 Mbit/s), and low speed (1.5 Mbit/s) operations.
- Supports operation as a standalone single port USB
- Supports four programmable, bidirectional USB endpoints
- Supports system memory interface with -bit addressing capability

The USB 3.0 module operates in following modes.

- Host Mode: SS/HS/FS/LS
- Device Mode: SS/HS/FS

NOTE

USB1_ID on pin J3.56 and USB2_ID on pin J3.44 are USB PHY signals with no other alternate function. Using them for OTG implementation requires special kernel patches which are not included on NXP releases.
NXP recommends using any GPIO for USB_ID function required to implement OTG interface.

8.8.1 USB Port1 Interface Signals

Table 27: USB 3.0/2.0 Port 1 Interface signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J3.67		USB1_D_N	0	Differential Pair Negative side USB OTG capable	SOC.E10
J3.65		USB1_D_P	0	Differential Pair Positive side USB OTG capable	SOC.D10
J3.53		USB1_RX_N	0	Differential Pair Negative side	SOC.B9
J3.55		USB1_RX_P	0	Differential Pair Positive side	SOC.A9
J3.59		USB1_TX_N	0	Differential Pair Negative side	SOC.B10
J3.61		USB1_TX_P	0	Differential Pair Positive side	SOC.A10
J3.66		USB1_VBUS	0	USB PHY power detect pin; 5V tolerant	SOC.A11

8.8.2 USB Port2 Interface Signals

Table 28: USB 3.0/2.0 Port 2 Interface signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J3.49		USB2_D_N	0	Differential Pair Negative side	SOC.E14
J3.47		USB2_D_P	0	Differential Pair Positive side	SOC.D14
J3.35		USB2_RX_N	0	Differential Pair Negative side	SOC.B12
J3.37		USB2_RX_P	0	Differential Pair Positive side	SOC.A12
J3.41		USB2_TX_N	0	Differential Pair Negative side	SOC.B13
J3.43		USB2_TX_P	0	Differential Pair Positive side	SOC.A13
J3.26		USB2_VBUS	0	USB PHY power detect pin; 5V tolerant	SOC.D12

8.8.3 USB OTG Interface Signals

The DART-MX8M-PLUS exposes pins, which can be optionally used for additional functions.

Table 29: USB Port 1 & 2 OTG Interface signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J3.52		USB1_OTG_ID	1		SOC.B7
J3.56		USB1_ID	0	USB PHY ID pin; No GPIO function. Requires kernel patches for using this pin; Usage not recommended; USB OTG ID alternative signal location. "Low" means the SoC is Host role "High" means the SoC is Peripheral role. NXP recommends using any GPIO to implement OTG function.	SOC.B11
J3.40		USB1_OTG_OC	1	USB OTG OC signal indicates that an overcurrent condition from an external current monitor on the downstream port occurred.	SOC.A6
J3.50		USB1_OTG_PWR	1	Differential Pair Positive side USB OTG PWR signal, active high control signal used to enable power to the downstream port	SOC.A5
J3.30		USB2_OTG_ID	1		SOC.D8
J3.44		USB2_ID	0	USB PHY ID pin; No GPIO function. Requires kernel patches for using this pin; Usage not recommended; USB OTG ID alternative signal location. "Low" means the SoC is Host role "High" means the SoC is Peripheral role. NXP recommends using any GPIO to implement OTG function.	SOC.E12
J3.38		USB2_OTG_OC	1		SOC.B5
J3.48		USB2_OTG_PWR	1		SOC.A4

8.9 PCIe

The DART-MX8M-PLUS exposes a single PCI Express Gen 3.0 single lane interface.
The PCI Express port requires an external 100MHz PCIe compliant reference clock if the function is enabled.

The SOM exports the PCIE differential clock. These pins are bi-directional which can either be used to feed 100 MHz reference clock to the PHY from external clock source, or to output an internal generated 100 MHz reference clock to PCIE connector or PCIE device.
On the DART-MX8M-PLUS carrier board, a PCIE clock generator chip is used to feed high-quality clock to both the PHY and connecter/device.
The internal clock of the chip can be used instead of clock generator (requires SW modification). However, the internal clock exhibits larger jitter than that from PCIE clock generator and does not meet Gen 3.0 specification requirements.

PCIe controller implements the following standards:

- PCI Express Base Specification, Revision 4.0, Version 0.7
- PCI Local Bus Specification, Revision 3.0
- PCI Bus Power Management Specification, Revision 1.2
- PCI Express Card Electromechanical Specification, Revision 1.1

Note: Access to the above specification requires membership in PCI-SIG.

The following list the key features of the Samsung PCIe PHY IP core used for PCI-Express (PCIe) applications:

- 2.5Gb/s, 5.0Gb/s, and 8.0Gb/s Serializer/De-serializer
- Serializes the 8b/10b encoded data for transmission for Gen1 and Gen2 operation, and 128b/130b encoded data for Gen3. De-serializes the received code groups
- PHY Interface for the PCI Express Architecture, Version 4.2 compliance
- Spread Spectrum Clocking in Transmitter and Receiver
- Separate Refclk Independent SSC (SRIS) Architecture
- Continuous-Time Linear Equalizer and 5-tap adaptive Decision-Feedback Equalizer

8.9.1 PCIE Signals

Table 30: PCIE Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J1.51		PCIE1_REF_CLK_N	0	Differential Pair Negative side	SOC.E16
J1.53		PCIE1_REF_CLK_P	0	Differential Pair Positive side	SOC.D16
J1.60		PCIE1_RX_N	0	Differential Pair Negative side	SOC.B14
J1.62		PCIE1_RX_P	0	Differential Pair Positive side	SOC.A14
J1.57		PCIE1_TX_N	0	Differential Pair Negative side	SOC.B15
J1.59		PCIE1_TX_P	0	Differential Pair Positive side	SOC.A15

8.9.2 PCIE Side Band Signals

Table 31: PCIE Side band Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J1.17		PCIE1_CLKREQ_B	2		SOC.AF8
J3.3		PCIE1_CLKREQ_B	2		SOC.AJ5

8.10 Audio

The DART-MX8M-PLUS features the following audio interfaces:

- WM8904CGEFL Audio codec interfaces:
  - Analog outputs & inputs: stereo line-in & Stereo HP out.
  - Digital microphone input
- Five external SAI (synchronous audio interface) modules supporting I2S, AC97, TDM, codec/DSP and DSD interfaces:
  - SAI-1 supports to up to 16-channels TX (8 lanes) and 16-channels RX (8 lanes) at 768KHz/32-bit
  - SAI-2/5 supports to up to 8-channels TX (4 lanes) and 8-channels RX (4 lanes) at 768KHz/32-bit
  - SAI-3 supports up to 4-channels TX (2 lanes) and 4-channels RX (2 lanes) at 768KHz/32-bit
  - SAI-6 supports to up to 2-channels TX (1 lanes) and 2-channels RX (1 lanes) at 768KHz/32-bit when multiplexed on SAI1, or up to 384kHz/32-bit when multiplexed on Ethernet primary pins
  - SAI-7 supports to up to 2-channels TX (1 lanes) and 2-channels RX (1 lanes) at 384KHz/32-bit
- PDM supporting up to 8-channels (4 lanes)
- S/PDIF Input and Output, including a new Raw Capture input mode
- Hifi4 Audio DSP, operating up to 800 MHz

Analog audio signals are part of the SOM WM8904 audio codec, available with **"AC" Configuration** only. The codec interfaces the SoC via SAI3 lines, when not assembled, SoC balls are exported to SOM connector instead of Analog codec interface pins.

The Codec features stereo ground-referenced headphone amplifiers using the Wolfson 'Class-W' amplifier techniques -incorporating an innovative dual-mode charge pump architecture - to optimize efficiency and power consumption during playback. The ground-referenced headphone and line outputs eliminate AC coupling capacitors, and both outputs include common mode feedback paths to reject ground noise.

The following figure illustrates the connectivity for no large AC coupling capacitors implemented on SOM.

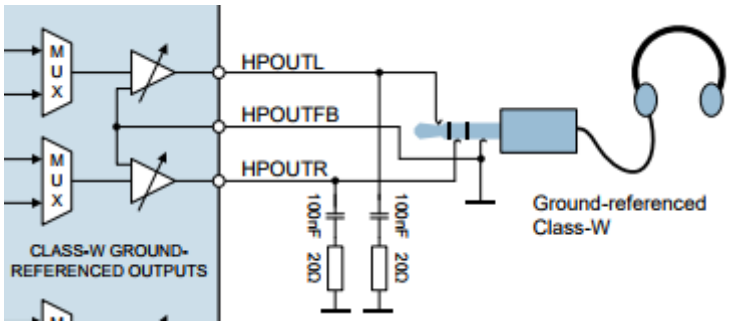


Figure 4: WM8904 Headphone connectivity

8.10.1 WM8904CGEFL Audio Codec

8.10.1.1 Audio Codec Signals

Table 32: Analog audio Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.12		AGND		Audio Ground	AGND
J2.14	AC	DMIC_CLK		Signal source is Audio Codec.	WM8904.1
J2.16	AC	DMIC_DATA		Signal source is Audio Codec.	WM8904.27
J2.2	AC	HPLOUT		Signal source is Audio Codec.	WM8904.13
J2.6	AC	HPOUTFB		Signal source is Audio Codec.	WM8904.14
J2.4	AC	HPROUT		Signal source is Audio Codec.	WM8904.15
J2.8	AC	LINEIN1_LP		Signal source is Audio Codec.	WM8904.26
J2.10	AC	LINEIN1_RP		Signal source is Audio Codec.	WM8904.24

8.10.2 Serial Audio Interface

The SAI module provides a synchronous audio interface that supports full duplex serial interfaces with frame synchronization, such as I2S, AC97, TDM, and codec/DSP interfaces.

The following table details the SAI interface signals definition.

Table 33: SAI interface signals definition

Name	Function	DIR
SAI_TXC	Transmit Bit Clock. The bit clock is an input when externally generated and an output when internally generated.	I/O
SAI_TXFS	Transmit Frame Sync. The frame sync is an input sampled synchronously by the bit clock when externally generated and an output generated synchronously by the bit clock when internally generated.	I/O
SAI_TXD	Transmit Data. The transmit data is generated synchronously by the bit clock and is tristate whenever not transmitting a word	O
SAI_RXC	Receive Bit Clock. The bit clock is an input when externally generated and an output when internally generated.	I/O
SAI_RXFS	Receive Frame Sync. The frame sync is an input sampled synchronously by the bit clock when externally generated and an output generated synchronously by the bit clock when internally generated.	I/O
SAI_RXD	Receive Data. The receive data is sampled synchronously by the bit clock.	I

8.10.2.1 SAI1 Signals

NOTE

ENET1 signals (with pad names SAI1_*) signal levels are referenced to **J2.41 (NVCC_SAI1_SAI5).** **See section 8.21.1.1**

Table 34: Serial Audio Interface 1 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.82		SAI1_MCLK	0	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AE12
J2.57		SAI1_RXC	0	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AH8
J2.61		SAI1_RXD0	0	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AC10
J2.59		SAI1_RXD1	0	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AF10
J2.63		SAI1_RXD2	0	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AH9
J2.62		SAI1_RXD3	0	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AJ8
J2.65		SAI1_RXD4	0	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AD10
J2.69		SAI1_RXD5	0	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AE10
J2.66		SAI1_RXD6	0	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AH10
J2.68		SAI1_RXD7	0	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AH12
J2.55		SAI1_RXFS	0	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AJ9
J2.69		SAI1_RXFS	3	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AE10
J2.46		SAI1_TXC	1	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AF14
J2.72		SAI1_TXC	0	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AJ12
J2.82		SAI1_TXC	2	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AE12
J2.34		SAI1_TXD0	1	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AC14
J2.70		SAI1_TXD0	0	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AJ11
J2.40		SAI1_TXD1	1	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AD14
J2.61		SAI1_TXD1	2	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AC10
J2.67		SAI1_TXD1	0	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AJ10
J2.36		SAI1_TXD2	1	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AE16

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.78		SAI1_TXD2	0	Connected internally to boot logic input. Drives BOOT_MODE0; Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1 As boot control with POR_B rise: High - External Boot (SD2) Low - Internal Boot (SD3 eMMC)	SOC.AH11
J2.42		SAI1_TXD3	1	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AD16
J2.73		SAI1_TXD3	0	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AD12
J2.38		SAI1_TXD4	1	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AF16
J2.68		SAI1_TXD4	3	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AH12
J2.74		SAI1_TXD4	0	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AH13
J2.44		SAI1_TXD5	1	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AE14
J2.71		SAI1_TXD5	0	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AH14
J2.80		SAI1_TXD6	0	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AC12
J2.76		SAI1_TXD7	0	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AJ13
J2.38		SAI1_TXFS	2	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AF16
J2.42		SAI1_TXFS	2	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AD16
J2.44		SAI1_TXFS	2	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AE14
J2.64		SAI1_TXFS	0	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AF12
J2.68		SAI1_TXFS	2	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AH12

8.10.2.2 SAI2 Signals

Table 35: Serial Audio Interface 2 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.54		SAI2_MCLK	0		SOC.AJ15
J2.50		SAI2_RXC	0		SOC.AJ16
J2.58		SAI2_RXD0	0		SOC.AJ14
J2.6	No AC	SAI2_RXD1	1	With “AC” configuration do not alter PINMUX function.	SOC.AJ19
J2.48		SAI2_RXD1	3		SOC.AH17
J2.8	No AC	SAI2_RXD2	1	With “AC” configuration do not alter PINMUX function.	SOC.AJ18
J2.2	No AC	SAI2_RXD3	1	With “AC” configuration do not alter PINMUX function.	SOC.AF18
J2.48		SAI2_RXFS	0		SOC.AH17
J2.56		SAI2_TXC	0		SOC.AH15
J2.60		SAI2_TXD0	0		SOC.AH16
J2.10	No AC	SAI2_TXD1	1	With “AC” configuration do not alter PINMUX function.	SOC.AC16
J2.52		SAI2_TXD1	3		SOC.AJ17
J2.58		SAI2_TXD1	3		SOC.AJ14
J2.4	No AC	SAI2_TXD2	1	With “AC” configuration do not alter PINMUX function.	SOC.AH19
J2.14	No AC	SAI2_TXD3	1	With “AC” configuration do not alter PINMUX function.	SOC.AH18
J2.52		SAI2_TXFS	0		SOC.AJ17

8.10.2.3 SAI3 Signals

Table 36: Serial Audio Interface 3 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.16	No AC	SAI3_MCLK	0	With "AC" configuration do not alter PINMUX function.	SOC.AJ20
J2.54		SAI3_MCLK	6		SOC.AJ15
J1.38		SAI3_MCLK_1V8	2	1.8V Level	SOC.R26
J2.8	No AC	SAI3_RXC	0	With "AC" configuration do not alter PINMUX function.	SOC.AJ18
J2.2	No AC	SAI3_RXD0	0	With "AC" configuration do not alter PINMUX function.	SOC.AF18
J1.48		SAI3_RXD0_1V8	2	1.8V Level	SOC.R25
J2.6	No AC	SAI3_RXD1	3	With "AC" configuration do not alter PINMUX function.	SOC.AJ19
J2.6	No AC	SAI3_RXFS	0	With "AC" configuration do not alter PINMUX function.	SOC.AJ19
J2.4	No AC	SAI3_TXC	0	With "AC" configuration do not alter PINMUX function.	SOC.AH19
J1.40		SAI3_TXC_1V8	2	1.8V Level	SOC.N25
J2.14	No AC	SAI3_TXD0	0	With "AC" configuration do not alter PINMUX function.	SOC.AH18
J1.34		SAI3_TXD0_1V8	2	1.8V Level	SOC.L26
J2.10	No AC	SAI3_TXD1	3	With "AC" configuration do not alter PINMUX function.	SOC.AC16
J2.10	No AC	SAI3_TXFS	0	With "AC" configuration do not alter PINMUX function.	SOC.AC16
J1.32		SAI3_TXFS_1V8	2	1.8V Level	SOC.L25

8.10.2.4 SAI5 Signals

NOTE

ENET1 signals (with pad names SAI1_*) signal levels are referenced to **J2.41 (NVCC_SAI1_SAI5).** **See section 8.21.1.1**

Table 37: Serial Audio Interface 5 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.16	No AC	SAI5_MCLK	2	With “AC” configuration do not alter PINMUX function.	SOC.AJ20
J2.46		SAI5_MCLK	0	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AF14
J2.54		SAI5_MCLK	1		SOC.AJ15
J2.82		SAI5_MCLK	1	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AE12
J2.8	No AC	SAI5_RXC	2	With “AC” configuration do not alter PINMUX function.	SOC.AJ18
J2.40		SAI5_RXC	0	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AD14
J2.57		SAI5_RXC	1	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AH8
J2.2	No AC	SAI5_RXD0	2	With “AC” configuration do not alter PINMUX function.	SOC.AF18
J2.36		SAI5_RXD0	0	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AE16
J2.61		SAI5_RXD0	1	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AC10
J2.10	No AC	SAI5_RXD1	2	With “AC” configuration do not alter PINMUX function.	SOC.AC16
J2.42		SAI5_RXD1	0	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AD16
J2.59		SAI5_RXD1	1	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AF10
J2.4	No AC	SAI5_RXD2	2	With “AC” configuration do not alter PINMUX function.	SOC.AH19
J2.38		SAI5_RXD2	0	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AF16
J2.63		SAI5_RXD2	1	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AH9
J2.14	No AC	SAI5_RXD3	2	With “AC” configuration do not alter PINMUX function.	SOC.AH18
J2.44		SAI5_RXD3	0	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AE14
J2.62		SAI5_RXD3	1	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AJ8
J2.6	No AC	SAI5_RXFS	2	With “AC” configuration do not alter PINMUX function.	SOC.AJ19
J2.34		SAI5_RXFS	0	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AC14
J2.55		SAI5_RXFS	1	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AJ9

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.38		SAI5_TXC	3	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AF16
J2.50		SAI5_TXC	1		SOC.AJ16
J2.72		SAI5_TXC	1	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AJ12
J2.44		SAI5_TXD0	3	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AE14
J2.58		SAI5_TXD0	1		SOC.AJ14
J2.70		SAI5_TXD0	1	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AJ11
J2.48		SAI5_TXD1	2		SOC.AH17
J2.52		SAI5_TXD1	1		SOC.AJ17
J2.67		SAI5_TXD1	1	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AJ10
J2.56		SAI5_TXD2	1		SOC.AH15
J2.78		SAI5_TXD2	1	Connected internally to boot logic input. **Drives BOOT_MODE0;** Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AH11
J2.60		SAI5_TXD3	1		SOC.AH16
J2.73		SAI5_TXD3	1	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AD12
J2.42		SAI5_TXFS	3	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AD16
J2.48		SAI5_TXFS	1		SOC.AH17
J2.64		SAI5_TXFS	1	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AF12
39		SAI5_TXFS	4		SOC.B6
63		SAI5_TXFS	1	Bank voltage set on SOM 1.8V/3.3V;	SOC.AB24
199	No AC	SAI5_TXFS	3	With “AC” configuration do not alter PINMUX function.	SOC.AC14

8.10.2.5 SAI6 Signals

Table 38: Serial Audio Interface 6 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J1.3	No EC	SAI6_MCLK	2	Powered by NVCC_ENET pin RGMII Transmit data Control	SOC.AF24
J2.68		SAI6_MCLK	1	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AH12
J2.76		SAI6_MCLK	1	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AJ13
J1.4	No EC	SAI6_RXC	2	Powered by NVCC_ENET pin RGMII Data out	SOC.AC25
J2.65		SAI6_RXC	2	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AD10
J2.74		SAI6_RXC	1	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AH13
J1.6	No EC	SAI6_RXD0	2	Powered by NVCC_ENET pin	SOC.AF26
J2.69		SAI6_RXD0	2	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AE10
J2.71		SAI6_RXD0	1	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AH14
J1.2	No EC	SAI6_RXFS	2	Powered by NVCC_ENET pin	SOC.AE26
J2.66		SAI6_RXFS	2	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AH10
J2.80		SAI6_RXFS	1	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AC12
J1.8	No EC	SAI6_TXC	2	Powered by NVCC_ENET pin	SOC.AD24
J2.65		SAI6_TXC	1	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AD10
J2.74		SAI6_TXC	2	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AH13
J1.13		SAI6_TXD0	2	Shared on SOM with "EC"; Signal after bidirectional open drain level translator; 3.3V level; Do not alter pinmux with "EC" configuration	SOC.AH28
J2.69		SAI6_TXD0	1	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AE10
J2.71		SAI6_TXD0	2	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AH14
J1.11		SAI6_TXFS	2	Shared on SOM with "EC"; Signal after bidirectional open drain level translator; 3.3V level; Include 2.37K pull up on DART; Do not alter pinmux with "EC" configuration	SOC.AH29
J2.66		SAI6_TXFS	1	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AH10
J2.80		SAI6_TXFS	2	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AC12

8.10.2.6 SAI7 Signals

Table 39: Serial Audio Interface 7 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J1.16	No EC	SAI7_MCLK	2	Powered by NVCC_ENET pin	SOC.AF28
J2.22	WBD	SAI7_MCLK	3	Used internally with "WBD"; Function can be released if Buffer disabled. Always exposed;	SOC.AH20
J1.14	No EC	SAI7_RXC	2	Powered by NVCC_ENET pin	SOC.AF29
J2.83		SAI7_RXC	3		SOC.AC20
J1.10	No EC	SAI7_RXD0	2	Powered by NVCC_ENET pin	SOC.AG29
J2.81		SAI7_RXD0	3		SOC.AD20
J1.12	No EC	SAI7_RXFS	2	Powered by NVCC_ENET pin	SOC.AG28
J2.77		SAI7_RXFS	3		SOC.AF20
J1.7	No EC	SAI7_TXC	2	Powered by NVCC_ENET pin; Includes series EMI filter	SOC.AE29
J2.24	WBD	SAI7_TXC	3	Used internally with "WBD"; Function can be released if Buffer disabled.	SOC.AH21
J1.5	No EC	SAI7_TXD0	2	Powered by NVCC_ENET pin; Includes series EMI filter	SOC.AE24
J2.20	WBD	SAI7_TXD0	3	Used internally with "WBD"; Function can be released if Buffer disabled. Always exposed;	SOC.AJ21
J1.9	No EC	SAI7_TXFS	2	Powered by NVCC_ENET pin	SOC.AE28
J2.79		SAI7_TXFS	3		SOC.AE20

8.10.3 PDM - Microphone Interface (MICFIL)

The PDM module of the i.MX 8M Plus SOC, provides a popular way to deliver audio from microphones to the processor in several applications, such as mobile phones.
Up to 8 channels can be implemented with 4 lanes.

The PDM Microphone Interface module is composed of:

- An input interface for each pair of PDM microphones.
- A decimation filter by channel.
- A FIFO by channel.
- A time generation unit.
- Shared interfaces to DMA, interrupts and SoC.
- One or more Hardware Voice Activity Detectors (HWVAD).

PDM block main features are:

- Decimation filters:
  - Fixed filtering characteristics for audio application.
  - 24-bit signed filter output.
  - Maximum dynamic range: 120dB.
  - Internal clock divider for a programmable PDM clock generation.
  - Full or partial set of channels operation with individual enable control.
  - Programmable decimation rate.
  - Programmable DC remover.
  - Range adjustment capability.
  - FIFOs with interrupt and DMA capability.
    - Each FIFO with 32 entries length.
- Hardware Voice Activity Detector (HWVAD).
  - Interrupt capability.
  - Zero-Crossing Detection (ZCD) option.

Table 40: PDM Interface Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J1.2	No EC	PDM_BIT0	3	Powered by NVCC_ENET pin	SOC.AE26
J1.12	No EC	PDM_BIT0	3	Powered by NVCC_ENET pin	SOC.AG28
J1.86		PDM_BIT0	4	NVCC_SD2_1V8_3V3 level;	SOC.AC28
J2.6	No AC	PDM_BIT0	6	With “AC” configuration do not alter PINMUX function.	SOC.AJ19
J2.36		PDM_BIT0	4	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AE16
J2.61		PDM_BIT0	3	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AC10
J1.6	No EC	PDM_BIT1	3	Powered by NVCC_ENET pin	SOC.AF26
J1.10	No EC	PDM_BIT1	3	Powered by NVCC_ENET pin	SOC.AG29
J1.80		PDM_BIT1	4	NVCC_SD2_1V8_3V3 level;	SOC.AC29
J2.2	No AC	PDM_BIT1	6	With “AC” configuration do not alter PINMUX function.	SOC.AF18

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.42		PDM_BIT1	4	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AD16
J2.50		PDM_BIT1	6		SOC.AJ16
J2.56		PDM_BIT1	6		SOC.AH15
J2.59		PDM_BIT1	3	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AF10
J1.7	No EC	PDM_BIT2	3	Powered by NVCC_ENET pin; Includes series EMI filter ENET RGMII Receive Clock: 125MHz @ 1000Mbps / 25MHz @ 100Mbps / 2.5MHz @ 10Mbps Samples RD[3:0] and RX_CTL	SOC.AE29
J1.8	No EC	PDM_BIT2	3	Powered by NVCC_ENET pin	SOC.AD24
J1.78		PDM_BIT2	4	NVCC_SD2_1V8_3V3 level;	SOC.AA26
J2.4	No AC	PDM_BIT2	6	With “AC” configuration do not alter PINMUX function.	SOC.AH19
J2.38		PDM_BIT2	4	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AF16
J2.48		PDM_BIT2	6		SOC.AH17
J2.52		PDM_BIT2	6		SOC.AJ17
J2.63		PDM_BIT2	3	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AH9
J1.9	No EC	PDM_BIT3	3	Powered by NVCC_ENET pin	SOC.AE28
J1.11		PDM_BIT3	3	Shared on SOM with "EC"; Signal after bidirectional open drain level translator; 3.3V level; Include 2.37K pull up on DART; Do not alter pinmux with "EC" configuration	SOC.AH29
J1.84		PDM_BIT3	4	NVCC_SD2_1V8_3V3 level;	SOC.AA25
J2.10	No AC	PDM_BIT3	6	With “AC” configuration do not alter PINMUX function.	SOC.AC16
J2.44		PDM_BIT3	4	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AE14
J2.58		PDM_BIT3	6		SOC.AJ14
J2.62		PDM_BIT3	3	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AJ8
J1.4	No EC	PDM_CLK	3	Powered by NVCC_ENET pin	SOC.AC25
J1.14	No EC	PDM_CLK	3	Powered by NVCC_ENET pin	SOC.AF29
J1.88		PDM_CLK	4	NVCC_SD2_1V8_3V3 level;	SOC.AB28
J2.8	No AC	PDM_CLK	6	With “AC” configuration do not alter PINMUX function.	SOC.AJ18
J2.40		PDM_CLK	4	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AD14
J2.57		PDM_CLK	3	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AH8
J2.76		PDM_CLK	3	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AJ13

8.10.4 SPDIF – Sony Philips Digital Interface Format

A standard audio file transfer format, developed jointly by the Sony and Phillips corporations. It supports Transmitter and Receiver functionality including frequency measurement block that allows the precise measurement of an incoming sampling frequency.
The SPDIF receiver extracts the audio data from each SPDIF frame and places the data in the SPDIF Rx left and right FIFOs with Channel Status and User bits.
For the SPDIF transmitter, the audio data is provided by the processor dedicated registers along with Channel Status and User bits.

Table 41: SPDIF Interface Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.14	No AC	SPDIF1_EXT_CLK	4	With “AC” configuration do not alter PINMUX function.	SOC.AH18
J3.32		SPDIF1_EXT_CLK	0		SOC.AC18
J1.16	No EC	SPDIF1_IN	3	Powered by NVCC_ENET pin	SOC.AF28
J1.84		SPDIF1_IN	3	NVCC_SD2_1V8_3V3 level;	SOC.AA25
J2.6	No AC	SPDIF1_IN	4	With “AC” configuration do not alter PINMUX function.	SOC.AJ19
J2.16	No AC	SPDIF1_IN	6	With “AC” configuration do not alter PINMUX function.	SOC.AJ20
J3.28		SPDIF1_IN	0		SOC.AD18
J1.3	No EC	SPDIF1_OUT	3	Powered by NVCC_ENET pin RGMII Transmit data Control	SOC.AF24
J1.78		SPDIF1_OUT	3	NVCC_SD2_1V8_3V3 level;	SOC.AA26
J2.16	No AC	SPDIF1_OUT	4	With “AC” configuration do not alter PINMUX function.	SOC.AJ20
J3.36		SPDIF1_OUT	0		SOC.AE18

8.11 UART

The DART-MX8M-PLUS exposes up to four UART interfaces some of which are multiplexed with other peripherals.
UART4 is used on SOM for Bluetooth interface and can be accessible only if the on SOM buffer is disabled or on SOM without ***"WBD" and "WB"*** Configuration.

The UART includes the following features:

- High-speed TIA/EIA-232-F compatible, up to 5 Mbit/s
- Serial IR interface low-speed, IrDA-compatible (up to 115.2 Kbit/s)
- 9-bit or Multidrop mode (RS-485) support (automatic slave address detection)
- 7 or 8 data bits for RS-232 characters, or 9 bit RS-485 format
- 1 or 2 stop bits
- Programmable parity (even, odd, and no parity)
- Hardware flow control support for request to send (RTS_B) and clear to send (CTS_B) signals
- RS-485 driver direction control via CTS_B signal
- Edge-selectable RTS_B and edge-detect interrupts
- Status flags for various flow control and FIFO states
- Voting logic for improved noise immunity (16x oversampling)
- Transmitter FIFO empty interrupt suppression
- UART internal clocks enable/disable
- Auto baud rate detection (up to 115.2 Kbit/s)
- Receiver and transmitter enable/disable for power saving
- RX_DATA input and TX_DATA output can be inverted respectively in RS-232/RS-485 mode
- DCE/DTE capability
- RTS_B, IrDA asynchronous wake (AIRINT), receive asynchronous wake (AWAKE) interrupts wake the processor from STOP mode
- Maskable interrupts
- Two DMA Requests (TxFIFO DMA Request and RxFIFO DMA Request)
- Escape character sequence detection
- Software reset (SRST_B)
- Two independent, 32-entry FIFOs for transmit and receive
- The peripheral clock can be totally asynchronous with the module clock. The module clock determines baud rate. This allows frequency scaling on peripheral clock (such as during DVFS mode) while remaining the module clock frequency and baud rate.

Table 42: UART I/O Configuration vs. mode

Port	DTE Mode		DCE Mode	
	Direction	Description	Direction	Description
UARTx_RTS_B	Output	UARTx_RTS_B from DTE to DCE	Input	UARTx_RTS_B from DTE to DCE
UARTx_CTS_B	Input	UARTx_CTS_B from DCE to DTE	Output	UARTx_CTS_B from DCE to DTE
UARTx_TX_ DATA	Input	Serial data from DCE to DTE	Output	Serial data from DCE to DTE
UARTx_RX _DATA	Output	Serial data from DTE to DCE	Input	Serial data from DTE to DCE

8.11.1.1 UART1 Signals

Table 43: UART1 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.52		UART1_CTS_B	4		SOC.AJ17
J2.87		UART1_CTS_B	1		SOC.AE6
J2.58		UART1_RTS_B	4		SOC.AJ14
J2.89		UART1_RTS_B	1		SOC.AJ4
J2.50		UART1_RX	4		SOC.AJ16
J2.88		UART1_RX	0	Used as debug UART on Variscite base board.	SOC.AD6
J2.48		UART1_TX	4		SOC.AH17
J2.90		UART1_TX	0	Used as debug UART on Variscite base board.	SOC.AJ3

8.11.1.2 UART2 Signals

Table 44: UART2 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.8	No AC	UART2_CTS_B	4	With “AC” configuration do not alter PINMUX function.	SOC.AJ18
J3.3		UART2_CTS_B	1		SOC.AJ5
J2.2	No AC	UART2_RTS_B	4	With “AC” configuration do not alter PINMUX function.	SOC.AF18
J3.1		UART2_RTS_B	1		SOC.AH5
J1.86		UART2_RX	3	NVCC_SD2_1V8_3V3 level;	SOC.AC28
J2.10	No AC	UART2_RX	4	With “AC” configuration do not alter PINMUX function.	SOC.AC16
J2.85		UART2_RX	0		SOC.AF6
J1.80		UART2_TX	3	NVCC_SD2_1V8_3V3 level;	SOC.AC29
J2.4	No AC	UART2_TX	4	With “AC” configuration do not alter PINMUX function.	SOC.AH19
J2.86		UART2_TX	0		SOC.AH4

8.11.1.3 UART3 Signals

Table 45: UART3 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.81		UART3_CTS_B	1		SOC.AD20
J1.29		UART3_RTS_B	4	***"WB"***: 3.3V Level; Other configuration 1V8 Level;	SOC.W25
J2.79		UART3_RTS_B	1		SOC.AE20
J2.77		UART3_RX	1		SOC.AF20
J2.87		UART3_RX	0		SOC.AE6
J1.40		UART3_RX_1V8	4	1.8V Level	SOC.N25
J2.83		UART3_TX	1		SOC.AC20
J2.89		UART3_TX	0		SOC.AJ4
J1.34		UART3_TX_1V8	4	1.8V Level	SOC.L26

8.11.1.4 UART4 Signals

Table 46: UART4 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.22	WBD/WB	UART4_CTS_B	1	Used internally with "WBD"; Function can be released if Buffer disabled. Always exposed;	SOC.AH20
J1.50		UART4_CTS_B_1V8	3	1.8V Level	SOC.L24
J2.26	WBD/WB	UART4_RTS_B	1	Used internally with "WBD"; Function can be released if Buffer disabled. Always exposed;	SOC.AJ22
J1.46		UART4_RTS_B_1V8	3	1.8V Level	SOC.N24
J1.82		UART4_RX	3	NVCC_SD2_1V8_3V3 level;	SOC.AB29
J2.24	WBD/WB	UART4_RX	1	Used internally with "WBD"; Function can be released if Buffer disabled.	SOC.AH21
J3.3		UART4_RX	0		SOC.AJ5
J1.48		UART4_RX_1V8	4	1.8V Level	SOC.R25
J1.88		UART4_TX	3	NVCC_SD2_1V8_3V3 level;	SOC.AB28
J2.20	WBD/WB	UART4_TX	1	Used internally with "WBD"; Function can be released if Buffer disabled. Always exposed;	SOC.AJ21
J3.1		UART4_TX	0		SOC.AH5
J1.32		UART4_TX_1V8	4	1.8V Level	SOC.L25

8.12 Flexible Controller Area Network

The Flexible Controller Area Network (FLEXCAN) module is a communication controller supporting CAN-FD (CAN Flexible Data Rate) and CAN2.0B specification.

Note: CAN-FD is supported only on Industrial variant of the SOM, Consumer variant of the SOM supports only CAN

Signal Description:

- CAN Rx: The receive pin from the CAN bus transceiver. Dominant state is represented by logic level '0'. Recessive state is represented by logic level '1'.
- CAN Tx: The transmit pin to the CAN bus transceiver. Dominant state is represented by logic level '0'. Recessive state is represented by logic level '1'.

8.12.1.1 FLEXCAN1 Signals

Table 47: FLEXCAN1 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.17		FLEXCAN1_RX	4	3.3V levels	SOC.AF22
J2.38		FLEXCAN1_RX	6	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AF16
J2.56		FLEXCAN1_RX	3		SOC.AH15
J3.28		FLEXCAN1_RX	4		SOC.AD18
J2.15		FLEXCAN1_TX	4	3.3V levels	SOC.AC22
J2.42		FLEXCAN1_TX	6	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AD16
J2.50		FLEXCAN1_TX	3		SOC.AJ16
J3.36		FLEXCAN1_TX	4		SOC.AE18

8.12.1.2 FLEXCAN2 Signals

Table 48: FLEXCAN2 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.21		FLEXCAN2_RX	4		SOC.AE22
J2.46		FLEXCAN2_RX	6	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AF14
J2.54		FLEXCAN2_RX	3		SOC.AJ15
J2.89		FLEXCAN2_RX	4		SOC.AJ4
J2.19		FLEXCAN2_TX	4	3.3V levels	SOC.AD22
J2.44		FLEXCAN2_TX	6	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AE14
J2.60		FLEXCAN2_TX	3		SOC.AH16
J2.87		FLEXCAN2_TX	4		SOC.AE6

8.13 ECSPI - Enhanced Configurable SPI

The DART-MX8M-PLUS exposes all ECSPI interfaces.

The Enhanced Configurable Serial Peripheral Interface (ECSPI) is a full-duplex, synchronous, four-wire serial communication block with full-duplex enhanced Synchronous Serial Interface and data rate up to 52 Mbit/s.

Key features of the ECSPI include:

- Full-duplex synchronous serial interface
- Master/Slave configurable
- One native Chip Select (SS) signal [see note below]
- Transfer continuation function allows unlimited length data transfers
- 32-bit wide by 64-entry FIFO for both transmit and receive data
- Polarity and phase of the Chip Select (SS) and SPI Clock (SCLK) are configurable
- Direct Memory Access (DMA) support
- Refer to the product data sheet for the maximum operating frequency

Note: Note: For interacting multiple peripherals on same SPI bus, one can define any GPIO to be used as chip select. Examples can be found in our DTS files.

8.13.1.1 ESCPI1 Signals

Table 49: ECSPI1 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.32		ECSPI1_MISO	3		SOC.AH6
J2.81		ECSPI1_MISO	0		SOC.AD20
J2.83		ECSPI1_MOSI	0		SOC.AC20
J2.77		ECSPI1_SCLK	0		SOC.AF20
J2.30		ECSPI1_SS0	3		SOC.AE8
J2.79		ECSPI1_SS0	0		SOC.AE20

8.13.1.2 ESCPI2 Signals

Table 50: ECSPI2 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J1.17		ECSPI2_MISO	3		SOC.AF8
J1.84		ECSPI2_MISO	2	NVCC_SD2_1V8_3V3 level;	SOC.AA25
J2.22	WBD	ECSPI2_MISO	0	Used internally with "WBD"; Function can be released if Buffer disabled. Always exposed;	SOC.AH20
J1.88		ECSPI2_MOSI	2	NVCC_SD2_1V8_3V3 level;	SOC.AB28
J2.20	WBD	ECSPI2_MOSI	0	Used internally with "WBD"; Function can be released if Buffer disabled. Always exposed;	SOC.AJ21
J3.42		ECSPI2_MOSI	3	5K internal PU included for backward compatibility;	SOC.AJ6
J1.82		ECSPI2_SCLK	2	NVCC_SD2_1V8_3V3 level;	SOC.AB29
J2.24	WBD	ECSPI2_SCLK	0	Used internally with "WBD"; Function can be released if Buffer disabled.	SOC.AH21
J3.46		ECSPI2_SCLK	3	5K internal PU included for backward compatibility;	SOC.AJ7
J1.19		ECSPI2_SS0	3		SOC.AD8
J1.78		ECSPI2_SS0	2	NVCC_SD2_1V8_3V3 level;	SOC.AA26
J2.26	WBD	ECSPI2_SS0	0	Used internally with "WBD"; Function can be released if Buffer disabled. Always exposed;	SOC.AJ22

8.13.1.3 ESCPI3 Signals

Table 51: ECSPI3 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.85		ECSPI3_MISO	1		SOC.AF6
J2.90		ECSPI3_MOSI	1	Used as debug UART on Variscite base board.	SOC.AJ3
J2.88		ECSPI3_SCLK	1	Used as debug UART on Variscite base board.	SOC.AD6
J2.86		ECSPI3_SS0	1		SOC.AH4

8.14 QSPI/FlexSPI - Quad Serial Peripheral Interface

The DART-MX8M-PLUS exposes one QSPI module which can be used to interface external serial flash devices.

The module contains the following features:

- Flexible sequence engine to support various flash vendor devices
- Single pad/Dual pad/Quad pad mode of operation
- Single Data Rate/Double Data Rate mode of operation
- Parallel Flash mode
- DMA support
- Memory mapped read access to connected flash devices
- Multi master access with priority and flexible and configurable buffer for each master

8.14.1 QSPIA Signals

Table 52: QSPIA Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J1.48		QSPI_A_D0_1V8	1	1.8V Level	SOC.R25
J1.32		QSPI_A_D1_1V8	1	1.8V Level	SOC.L25
J1.50		QSPI_A_D2_1V8	1	1.8V Level	SOC.L24
J1.46		QSPI_A_D3_1V8	1	1.8V Level	SOC.N24
J1.38		QSPI_A_DQS_1V8	1	1.8V Level	SOC.R26
J1.40		QSPI_A_SCLK_1V8	1	1.8V Level	SOC.N25
J1.34		QSPI_A_SS0_B_1V8	1	1.8V Level	SOC.L26

8.15 PWM

The DART-MX8M-PLUS exports up to 4 General purpose Pulse Width Modulators (PWM) signals.

PWM Features:

- 16-bit up-counter with clock source selection (bus clock, baud clock, or 32K)
- 4 x 16 FIFO to minimize interrupt overhead
- 12-bit prescaler for division of clock
- Sound and melody generation
- Active high or active low configured output
- Can be programmed to be active in low-power mode
- Can be programmed to be active in debug mode
- Interrupts at compare and rollover

8.15.1.1 PWM Signals

Table 53: PWM Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J1.19		PWM1_OUT	1		SOC.AD8
J2.46		PWM1_OUT	2	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AF14
J3.32		PWM1_OUT	1		SOC.AC18
J3.60		PWM1_OUT	2		SOC.A8
J3.64		PWM1_OUT	1		SOC.E8
J1.17		PWM2_OUT	1		SOC.AF8
J1.47		PWM2_OUT	2		SOC.B8
J2.36		PWM2_OUT	2	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AE16
J3.28		PWM2_OUT	1		SOC.AD18
J3.30		PWM2_OUT	2		SOC.D8
J3.40		PWM2_OUT	5		SOC.A6
J2.40		PWM3_OUT	2	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AD14
J3.36		PWM3_OUT	1		SOC.AE18
J3.42		PWM3_OUT	1	5K internal PU included for backward compatibility;	SOC.AJ6
J3.48		PWM3_OUT	5		SOC.A4
J3.52		PWM3_OUT	2		SOC.B7
J2.16	No AC	PWM4_OUT	1	With “AC” configuration do not alter PINMUX function.	SOC.AJ20
J2.34		PWM4_OUT	2	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AC14
J3.38		PWM4_OUT	5		SOC.B5
J3.46		PWM4_OUT	1	5K internal PU included for backward compatibility;	SOC.AJ7

8.16 I2C

The DART-MX8M-PLUS exposes up to 5x I2C Interface connectivity peripherals which provides serial interface for external devices. Data rates of up to 400 kbps are supported.

The Inter-Integrated Circuit (I2C) provides functionality of a standard I2C master and slave. I2C is a two-wire, bidirectional serial bus that provides a simple, efficient method of data exchange, minimizing the interconnection between devices.
This bus is suitable for applications requiring occasional communications over a short distance between many devices. The flexible I2C standard allows additional devices to be connected to the bus for expansion and system development.

The I2C has the following key features:

- Compatible with the I2C Bus Specification, version 2.1, by Philips Semiconductor (now NXP Semiconductors).
- Multi-master operation.
- After a reset, the I2C defaults to Slave Receive operations.
- Software programmability for one of 64 different serial clock frequencies:
    - Standard mode, I2C supports the data transfer rates up to 100 Kbits/s
    - In Fast mode, data transfer rates up to 400 Kbits/s can be achieved
- Software-selectable acknowledge bit
- Interrupt-driven, byte-by-byte data transfer
- Arbitration-lost interrupt with automatic mode switching from master to slave
- Calling address identification interrupt
- Start and stop signal generation/detection
- Repeated start signal generation
- Acknowledge bit generation/detection
- Bus-busy detection

8.16.1.1 I2C1 Signals

I2C1 is used internally by on-SOM EEPROM used for boot process and by Audio codec.
Exporting I2C1 signals from the SOM using different option of SoC pinmux capabilities, is not permitted.

8.16.1.2 I2C2 Signals

Table 54: I2C2 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.32		I2C2_SCL	0		SOC.AH6
J2.81		I2C2_SCL	2		SOC.AD20
J2.30		I2C2_SDA	0		SOC.AE8
J2.79		I2C2_SDA	2		SOC.AE20

8.16.1.3 I2C3 Signals

Table 55: I2C3 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J1.29		I2C3_SCL	3	***"WB"***: 3.3V Level; Other configurations 1.8V Level	SOC.W25
J2.24	WBD	I2C3_SCL	2	Used internally with "WBD"; Function can be released if Buffer disabled.	SOC.AH21
J3.46		I2C3_SCL	0	5K internal PU included for backward compatibility;	SOC.AJ7
J1.38		I2C3_SCL_1V8	4	1.8V Level	SOC.R26
J2.20	WBD	I2C3_SDA	2	Used internally with "WBD"; Function can be released if Buffer disabled. Always exposed;	SOC.AJ21
J3.42		I2C3_SDA	0	5K internal PU included for backward compatibility;	SOC.AJ6

8.16.1.4 I2C4 Signals

Table 56: I2C4 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J1.17		I2C4_SCL	0		SOC.AF8
J1.80		I2C4_SCL	2	NVCC_SD2_1V8_3V3 level;	SOC.AC29
J2.22	WBD	I2C4_SCL	2	Used internally with "WBD"; Function can be released if Buffer disabled. Always exposed;	SOC.AH20
J1.19		I2C4_SDA	0		SOC.AD8
J1.86		I2C4_SDA	2	NVCC_SD2_1V8_3V3 level;	SOC.AC28
J2.26	WBD	I2C4_SDA	2	Used internally with "WBD"; Function can be released if Buffer disabled. Always exposed;	SOC.AJ22
J1.50		I2C4_SDA_1V8	4	1.8V Level	SOC.L24

8.16.1.5 I2C5 Signals

Table 57: I2C5 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.15		I2C5_SCL	3	3.3V levels	SOC.AC22
J2.36		I2C5_SCL	3	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AE16
J3.36		I2C5_SCL	2		SOC.AE18
J2.17		I2C5_SDA	3	3.3V levels	SOC.AF22
J2.46		I2C5_SDA	3	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AF14
J3.28		I2C5_SDA	2		SOC.AD18

8.16.1.6 I2C6 Signals

Table 58: I2C6 Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.19		I2C6_SCL	3	3.3V levels	SOC.AD22
J2.34		I2C6_SCL	3	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AC14
J3.3		I2C6_SCL	4		SOC.AJ5
J2.21		I2C6_SDA	3	3.3V levels	SOC.AE22
J2.40		I2C6_SDA	3	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AD14
J3.1		I2C6_SDA	4		SOC.AH5

8.17 General Purpose Timer

The DART-MX8M-PLUS exposes the GPT interface to its connector.

GPT Features include:

- One 32-bit up-counter with clock source selection, including external clock
- Two input capture channels with a programmable trigger edge
- Three outputs compare channels with a programmable output mode. A "forced compare" feature is also available
- Can be programmed to be active in low power and debug modes
- Interrupt generation at capture, compare, and rollover events
- Restart or free-run modes for counter operations

8.17.1.1 GPT Signals

Table 59: General Purpose Timer Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.4	No AC	GPT1_CAPTURE1	3	With “AC” configuration do not alter PINMUX function.	SOC.AH19
J3.1		GPT1_CAPTURE1	3		SOC.AH5
J2.14	No AC	GPT1_CAPTURE2	3	With “AC” configuration do not alter PINMUX function.	SOC.AH18
J2.87		GPT1_CAPTURE2	3		SOC.AE6
J2.8	No AC	GPT1_CLK	3	With “AC” configuration do not alter PINMUX function.	SOC.AJ18
J2.89		GPT1_CLK	3		SOC.AJ4
J3.3		GPT1_COMPARE1	3		SOC.AJ5
J3.36		GPT1_COMPARE1	3		SOC.AE18
J2.86		GPT1_COMPARE2	3		SOC.AH4
J3.28		GPT1_COMPARE2	3		SOC.AD18
J2.85		GPT1_COMPARE3	3		SOC.AF6
J3.32		GPT1_COMPARE3	3		SOC.AC18
J3.46		GPT2_CLK	2	5K internal PU included for backward compatibility;	SOC.AJ7
J3.42		GPT3_CLK	2	5K internal PU included for backward compatibility;	SOC.AJ6

8.18 Reference Clocks

DART-MX8M-PLUS exposes several clock outputs from the internal CCM module which can be used to clock external devices.

8.18.1 Clock Signals

Table 60: Clock Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.22	WBD	CLKO1	4	Used internally with "WBD"; Function can be released if Buffer disabled. Always exposed;	SOC.AH20
J3.48		CLKO1	6		SOC.A4
J2.26	WBD	CLKO2	4	Used internally with "WBD"; Function can be released if Buffer disabled. Always exposed;	SOC.AJ22
J3.38		CLKO2	6		SOC.B5
J1.1		ENET_PHY_REF_CLK_ROOT	1		SOC.A7
J1.6	No EC	ENET_QOS_TX_CLK_IN ENET_QOS_REF_CLK_ROOT_OUT	1		SOC.AF26
J2.82		ENET1_TX_CLK_IN ENET_REF_CLK_ROOT_OUT	4	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AE12
J1.1		EXT_CLK1	6	Input clock for CCM	SOC.A7
J3.64		EXT_CLK2	6	Input clock for CCM	SOC.E8
J3.58		EXT_CLK3	6	Input clock for CCM	SOC.A3
J3.54		EXT_CLK4	6	Input clock for CCM	SOC.F6
J1.1		REF_CLK_32K	5		SOC.A7

8.19 JTAG

DART-MX8M-PLUS exposes System JTAG Controller (SJC) provides debug and test control with maximum security. The test access port (TAP) is designed to support features compatible with the IEEE standard 1149.1 v2001 (JTAG) and IEEE 1149.6 standards.

The JTAG port allows debug-related control and status, such as putting selected cores into reset and/or debug mode and the ability to monitor individual core status signals via JTAG. JTAG port interfaces the M7 and Cortex A53 Cores DAP - debug access port.
The DART-MX8M-PLUS JTAG MOD pin is hardware tied low and enables the Daisy chain ALL mode only, used for common SW debug (High speed and production).

8.19.1.1 JTAG Signals

Table 61: JTAG signals on 14-pin Header Connector

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.5		JTAG_MODE	0	Exposed on DT8M & DT8MM JTAG_TRST pin; PD 8.2K Ohm included on DART; Exposed for Boundary Scan	SOC.G20
J2.1		JTAG_TCK	0	Include PD of 8.2K Ohm	SOC.G18
J2.7		JTAG_TDI	0		SOC.G16
J2.9		JTAG_TDO	0		SOC.F14
J2.3		JTAG_TMS	0		SOC.G14
J2.28		SJC_DE_B	7	Alternate function of WDOG_B;	SOC.B6

8.20 General Purpose IO

The DART-MX8M-PLUS provides IO pins which can be used as GPIOs.

8.20.1.1 GPIO Signals

Table 62: GPIO Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J1.1		GPIO1_IO00	0		SOC.A7
J3.64		GPIO1_IO01	0		SOC.E8
J2.28		GPIO1_IO02	0	Alternate function of WDOG_B;	SOC.B6
J3.62		GPIO1_IO05	0		SOC.B4
J3.58		GPIO1_IO06	0		SOC.A3
J3.54		GPIO1_IO07	0		SOC.F6
J3.60		GPIO1_IO08	0		SOC.A8
J1.47		GPIO1_IO09	0		SOC.B8
J3.52		GPIO1_IO10	0		SOC.B7
J3.30		GPIO1_IO11	0		SOC.D8
J3.50		GPIO1_IO12	0		SOC.A5
J3.40		GPIO1_IO13	0		SOC.A6
J3.48		GPIO1_IO14	0		SOC.A4
J3.38		GPIO1_IO15	0		SOC.B5
J1.13		GPIO1_IO16	5	Shared on SOM with "EC"; Signal after bidirectional open drain level translator; 3.3V level; Do not alter pinmux with "EC" configuration	SOC.AH28
J1.11		GPIO1_IO17	5	Shared on SOM with "EC"; Signal after bidirectional open drain level translator; 3.3V level; Include 2.37K pull up on DART; Do not alter pinmux with "EC" configuration	SOC.AH29
J1.8	No EC	GPIO1_IO18	5	Powered by NVCC_ENET pin	SOC.AD24
J1.6	No EC	GPIO1_IO19	5	Powered by NVCC_ENET pin	SOC.AF26
J1.2	No EC	GPIO1_IO20	5	Powered by NVCC_ENET pin	SOC.AE26
J1.4	No EC	GPIO1_IO21	5	Powered by NVCC_ENET pin	SOC.AC25
J1.3	No EC	GPIO1_IO22	5	Powered by NVCC_ENET pin	SOC.AF24
J1.5	No EC	GPIO1_IO23	5	Powered by NVCC_ENET pin; Includes series EMI filter	SOC.AE24
J1.9	No EC	GPIO1_IO24	5	Powered by NVCC_ENET pin	SOC.AE28
J1.7	No EC	GPIO1_IO25	5	Powered by NVCC_ENET pin; Includes series EMI filter	SOC.AE29
J1.10	No EC	GPIO1_IO26	5	Powered by NVCC_ENET pin	SOC.AG29
J1.12	No EC	GPIO1_IO27	5	Powered by NVCC_ENET pin	SOC.AG28
J1.14	No EC	GPIO1_IO28	5	Powered by NVCC_ENET pin	SOC.AF29
J1.16	No EC	GPIO1_IO29	5	Powered by NVCC_ENET pin	SOC.AF28
J1.29		GPIO2_IO10	5	"WB": 3.3V Level; Other configurations 1V8 Level	SOC.W25

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J1.74		GPIO2_IO12	5	NVCC_SD2_1V8_3V3 level;	SOC.AD29
J1.82		GPIO2_IO13	5	NVCC_SD2_1V8_3V3 level;	SOC.AB29
J1.88		GPIO2_IO14	5	NVCC_SD2_1V8_3V3 level;	SOC.AB28
J1.86		GPIO2_IO15	5	NVCC_SD2_1V8_3V3 level;	SOC.AC28
J1.80		GPIO2_IO16	5	NVCC_SD2_1V8_3V3 level;	SOC.AC29
J1.78		GPIO2_IO17	5	NVCC_SD2_1V8_3V3 level;	SOC.AA26
J1.84		GPIO2_IO18	5	NVCC_SD2_1V8_3V3 level;	SOC.AA25
J1.28		GPIO2_IO19	5	NVCC_SD2_1V8_3V3 level;	SOC.AD28
J1.40		GPIO3_IO00_1V8	5	1.8V Level	SOC.N25
J1.34		GPIO3_IO01_1V8	5	1.8V Level	SOC.L26
J1.48		GPIO3_IO06_1V8	5	1.8V Level	SOC.R25
J1.32		GPIO3_IO07_1V8	5	1.8V Level	SOC.L25
J1.50		GPIO3_IO08_1V8	5	1.8V Level	SOC.L24
J1.46		GPIO3_IO09_1V8	5	1.8V Level	SOC.N24
J1.38		GPIO3_IO14_1V8	5	1.8V Level	SOC.R26
J2.34		GPIO3_IO19	5	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AC14
J2.40		GPIO3_IO20	5	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AD14
J2.36		GPIO3_IO21	5	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AE16
J2.42		GPIO3_IO22	5	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AD16
J2.38		GPIO3_IO23	5	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AF16
J2.44		GPIO3_IO24	5	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AE14
J2.46		GPIO3_IO25	5	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AF14
J2.15		GPIO3_IO26	5	3.3V levels	SOC.AC22
J2.17		GPIO3_IO27	5	3.3V levels	SOC.AF22
J2.19		GPIO3_IO28	5	3.3V levels	SOC.AD22
J2.21		GPIO3_IO29	5	3.3V levels	SOC.AE22
J2.55		GPIO4_IO00	5	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AJ9
J2.57		GPIO4_IO01	5	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AH8
J2.61		GPIO4_IO02	5	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AC10
J2.59		GPIO4_IO03	5	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AF10
J2.63		GPIO4_IO04	5	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AH9
J2.62		GPIO4_IO05	5	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AJ8
J2.65		GPIO4_IO06	5	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AD10

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.69		GPIO4_IO07	5	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AE10
J2.66		GPIO4_IO08	5	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AH10
J2.68		GPIO4_IO09	5	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AH12
J2.64		GPIO4_IO10	5	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AF12
J2.72		GPIO4_IO11	5	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AJ12
J2.70		GPIO4_IO12	5	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AJ11
J2.67		GPIO4_IO13	5	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AJ10
J2.78		GPIO4_IO14	5	Connected internally to boot logic input. **Drives BOOT_MODE0;** Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AH11
J2.73		GPIO4_IO15	5	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AD12
J2.74		GPIO4_IO16	5	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AH13
J2.71		GPIO4_IO17	5	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AH14
J2.80		GPIO4_IO18	5	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AC12
J2.76		GPIO4_IO19	5	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AJ13
J2.82		GPIO4_IO20	5	Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1	SOC.AE12
J2.48		GPIO4_IO21	5		SOC.AH17
J2.50		GPIO4_IO22	5		SOC.AJ16
J2.58		GPIO4_IO23	5		SOC.AJ14
J2.52		GPIO4_IO24	5		SOC.AJ17
J2.56		GPIO4_IO25	5		SOC.AH15
J2.60		GPIO4_IO26	5		SOC.AH16
J2.54		GPIO4_IO27	5		SOC.AJ15
J2.6	No AC	GPIO4_IO28	5	With “AC” configuration do not alter PINMUX function.	SOC.AJ19
J2.8	No AC	GPIO4_IO29	5	With “AC” configuration do not alter PINMUX function.	SOC.AJ18
J2.2	No AC	GPIO4_IO30	5	With “AC” configuration do not alter PINMUX function.	SOC.AF18
J2.10	No AC	GPIO4_IO31	5	With “AC” configuration do not alter PINMUX function.	SOC.AC16
J2.4	No AC	GPIO5_IO00	5	With “AC” configuration do not alter PINMUX function.	SOC.AH19
J2.14	No AC	GPIO5_IO01	5	With “AC” configuration do not alter PINMUX function.	SOC.AH18
J2.16	No AC	GPIO5_IO02	5	With “AC” configuration do not alter PINMUX function.	SOC.AJ20

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J3.36		GPIO5_IO03	5		SOC.AE18
J3.28		GPIO5_IO04	5		SOC.AD18
J3.32		GPIO5_IO05	5		SOC.AC18
J2.77		GPIO5_IO06	5		SOC.AF20
J2.83		GPIO5_IO07	5		SOC.AC20
J2.81		GPIO5_IO08	5		SOC.AD20
J2.79		GPIO5_IO09	5		SOC.AE20
J2.24	WBD/WB	GPIO5_IO10	5	Used internally with ***"WBD"*** or ***"WB"***; Function can be released if Buffer disabled.	SOC.AH21
J2.20	WBD/WB	GPIO5_IO11	5	Used internally with ***"WBD"*** or ***"WB"***; Function can be released if Buffer disabled.	SOC.AJ21
J2.22	WBD/WB	GPIO5_IO12	5	Used internally with ***"WBD"*** or ***"WB"***; Function can be released if Buffer disabled.	SOC.AH20
J2.26	WBD/WB	GPIO5_IO13	5	Used internally with ***"WBD"*** or ***"WB"***; Function can be released if Buffer disabled.	SOC.AJ22
J2.32		GPIO5_IO16	5		SOC.AH6
J2.30		GPIO5_IO17	5		SOC.AE8
J3.46		GPIO5_IO18	5	5K internal PU included for backward compatibility;	SOC.AJ7
J3.42		GPIO5_IO19	5	5K internal PU included for backward compatibility;	SOC.AJ6
J1.17		GPIO5_IO20	5		SOC.AF8
J1.19		GPIO5_IO21	5		SOC.AD8
J2.88		GPIO5_IO22	5	Used as debug UART on Variscite base board.	SOC.AD6
J2.90		GPIO5_IO23	5	Used as debug UART on Variscite base board.	SOC.AJ3
J2.85		GPIO5_IO24	5		SOC.AF6
J2.86		GPIO5_IO25	5		SOC.AH4
J2.87		GPIO5_IO26	5		SOC.AE6
J2.89		GPIO5_IO27	5		SOC.AJ4
J3.3		GPIO5_IO28	5		SOC.AJ5
J3.1		GPIO5_IO29	5		SOC.AH5

8.21 Power

8.21.1 Power

Table 63: Power

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J1.27		NVCC_3V3		Power output from SOM; Rises with last power rail; Can be used to control base board power. Check out Section 9.3 for maximum current.	
J1.31	No EC	NVCC_ENET		Power IN: supply power for ENET pins group **"EC"** configuration: * DO NOT CONNECT! **No "EC"** configuration: Must supply one option (Max. 50mA required) - * RMII uses 1.8 or 3.3V. * RGMII uses 1.8V. * GPIO 1.8V/3.3V	
J2.41		NVCC_SAI1_SAI5		Power output for SAI1_SAI5 pads; Connected to PMIC LDO4 Programmable output 1.8V/3.3V; On power up will start at 1.8V; After power up Set by SPL by Default to 1.8V; **See section 8.21.1.1** On DART-MX8M was VDD_PHY_1V8 to be used for HDMI termination control; As the HDMI changes to DC coupled this change should not conflict.	
J1.90		NVCC_SD2_1V8_3V3		Power output from SOM; Power the SD2 interface IO pins; Will change 1.8V/3.3V according to SD capabilities. Use for PU resistor on SD2_CD_B and SD2_CMD lines.	
J1.15		NVCC_SNVS_1V8		1.8V Power output from SOM for SNVS domain; Valid with VBAT. Max. 1mA draw allowed;	
J3.66		USB1_VBUS		USB PHY power detect pin; Included 31.6K series resistor on DART to be 5V tolerant	SOC.A11
J3.26		USB2_VBUS		USB PHY power detect pin; Included 31.6K series resistor on DART to be 5V tolerant	SOC.D12
J3.71		VBAT		SOM Power	VBAT
J3.73		VBAT		SOM Power	VBAT
J3.75		VBAT		SOM Power	VBAT
J3.77		VBAT		SOM Power	VBAT
J3.79		VBAT		SOM Power	VBAT
J3.81		VBAT		SOM Power	VBAT
J3.83		VBAT		SOM Power	VBAT
J3.85		VBAT		SOM Power	VBAT
J3.87		VBAT		SOM Power	VBAT

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J3.89		VBAT		SOM Power	VBAT

8.21.1.1 NVCC_SAI1_SAI5

The NVCC_SAI1_SAI5 rail source on SOM is shown in the below diagram.
PMIC LDO4 is a programmable LDO which is OFF on power up.
After power up, LDO4 can be powered in SW (SPL/U-boot/Kernel) on and programmed to output 1.8V/3.3V.

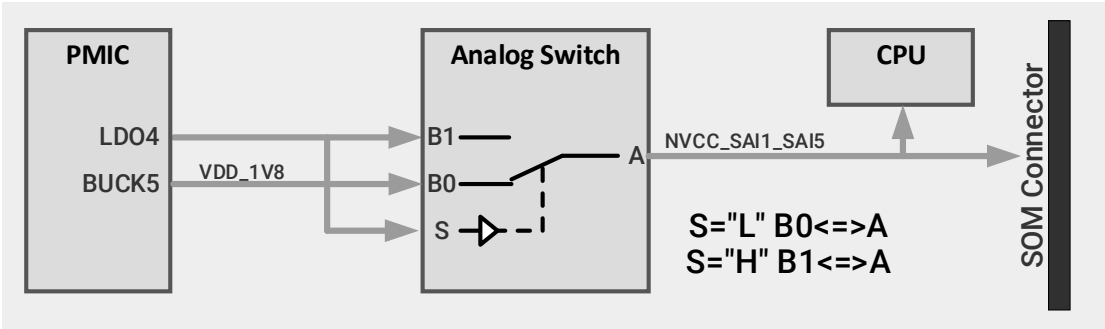
For compatibility to DART-MX8M and DART-MX8M-MINI,
Pin J2.78 SAI1_TXD2 is connected internally via buffer to BOOT_MODE0 of DART-MX8M-PLUS and used as boot source selection.
J2.78 SAI1_TXD2 power bank on CPU side is powered by NVCC_SAI1_SAI5 rail.

In order to provide power to NVCC_SAI1_SAI5 rail during boot, an analog switch is used:

B0<=>A
On power up, LDO4 is OFF -
Switch is set Low and BUCK5 VDD_1V8 is selected as NVCC_SAI1_SAI5 source.

B1<=>A
After power up, LDO4 is powered on in SW (SPL) to default 1.8v -
Switch is set High and LDO4 is selected as NVCC_SAI1_SAI5 source.

Attention should be given to pins which are referenced to NVCC_SAI1_SAI5.
These pins can be shorted to 3.3V only after power up and when LDO is set to 3.3V.
Alternatively, these pins can be connected to 3.3V using a series resistor limiting the current to a maximum of 1mA.



NOTE

NVCC_SAI1_SAI5 should be used as supply power source only when LDO4 is powered and not when it is powered by BUCK5. In addition, adding 4.7uF to 20uF ceramic capacitor rated higher than 6.3V is required.

8.21.2 Ground

Table 64: Digital Ground Pins

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.12		AGND		Audio Ground	
J1.18		GND		Digital Ground	
J1.21		GND		Digital Ground	
J1.30		GND		Digital Ground	
J1.33		GND		Digital Ground	
J1.49		GND		Digital Ground	
J1.52		GND		Digital Ground	
J1.55		GND		Digital Ground	
J1.58		GND		Digital Ground	
J1.61		GND		Digital Ground	
J1.64		GND		Digital Ground	
J1.67		GND		Digital Ground	
J1.70		GND		Digital Ground	
J1.76		GND		Digital Ground	
J1.85		GND		Digital Ground	
J2.18		GND		Digital Ground	
J2.23		GND		Digital Ground	
J2.47		GND		Digital Ground	
J2.53		GND		Digital Ground	
J2.75		GND		Digital Ground	
J2.84		GND		Digital Ground	
J3.9		GND		Digital Ground	
J3.10		GND		Digital Ground	
J3.15		GND		Digital Ground	
J3.21		GND		Digital Ground	
J3.24		GND		Digital Ground	
J3.27		GND		Digital Ground	
J3.33		GND		Digital Ground	
J3.34		GND		Digital Ground	
J3.39		GND		Digital Ground	
J3.45		GND		Digital Ground	
J3.51		GND		Digital Ground	
J3.57		GND		Digital Ground	
J3.63		GND		Digital Ground	
J3.68		GND		Digital Ground	
J3.74		GND		Digital Ground	

8.21.3 Not Connected

Table 65: Not Connected Pins

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J1.3	EC	NC		With "EC" configuration this pin in Not Connected.	
J1.23	NO WBD	NC		With "No WBD" or "No WB" configuration this pin in Not Connected.	
J1.25	NO WBD	NC		With "No WBD" or "No WB" configuration this pin in Not Connected.	
J1.35	DSCM	NC		Pin not connected with DSCM configuration!	
J1.36		NC		Not Connected	
J1.37	DSCM	NC		Pin not connected with DSCM configuration!	
J1.39	DSCM	NC		Pin not connected with DSCM configuration!	
J1.41	DSCM	NC		Pin not connected with DSCM configuration!	
J1.42	DSCM	NC		Pin not connected with DSCM configuration!	
J1.43	DSCM	NC		Pin not connected with DSCM configuration!	
J1.44	DSCM	NC		Pin not connected with DSCM configuration!	
J1.45	DSCM	NC		Pin not connected with DSCM configuration!	
J1.54		NC		Not Connected	
J1.56		NC		Not Connected	
J1.63		NC		Not Connected	
J1.65		NC		Not Connected	
J1.66	DSCM	NC		Pin not connected with DSCM configuration!	
J1.68	DSCM	NC		Pin not connected with DSCM configuration!	
J2.37		NC		Not Connected	
J2.39		NC		Not Connected	
J3.69		NC		Not Connected	

8.22 System Control

8.22.1 System Control Signals

Table 66: System Control Signals

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J1.20		ONOFF_1V8	0	SOC input with internal 100K PU; SNVS_1V8 level; ***In OFF mode:*** brief connection to GND causes the internal power management state machine to change state to ON. ***In ON mode:*** brief connection to GND generates an interrupt (intended to initiate a software-controllable power-down). ***To Force OFF***: approximate 5 second or more connection to GND Not used leave Floating;	SOC.G22
J1.22		PMIC_RST_B		PMIC input to control SOM power rails and assertion of POR_B; Active-low input for triggering the system to cold or warm reset. Include 100K pull up to SNVS_1V8; On 1st power up will cause cold reset on SOM; After 1st power up, PMIC can be programmed to Cold or Warm or no reset; on input event; Cold/Warm reset will also assert internal POR_B signal; If held low will prevent from DART from powering up. **DART-MX8MP-V1.0A engineering samples version: this pin connected to SOC.F22 PMIC_ON_REQ, which cannot be pulled low externally and cannot be used for Cold reset externally.**	PMIC.8
J1.26		PMIC_STBY_REQ_1V8	0	SOC output; Can be used externally to control carrier board power for standby state; Active-high output for going to SUSPEND state; SNVS_1V8 level; ***Transition 0 to 1***: Enter Standby ***Transition 1 to 0***: Wake up from standby Not used leave Floating;	SOC.J24
J1.24		POR_B_1V8	0	PMIC output (OD with PU) connected to SOC; Can be pulled low externally to cause warm reset. SNVS_1V8 level; Not used leave Floating; Either POR_B or PMIC_RST_B should be driven by Base power up reset circuit;	SOC.J29
J2.28		WDOG1_WDOG_ANY	5	Alternate function of WDOG_B; Can be tied on Custom to: POR_B - for Warm reset PMIC_RST - for cold reset	SOC.B6
J2.28		WDOG1_WDOG_B	1	Alternate function of WDOG_B; Can be tied on Custom to: POR_B - for Warm reset PMIC_RST - for cold reset	SOC.B6

8.22.2 Boot Configuration

The DART-MX8M-PLUS can be boot from the following sources:

- Internal source - eMMC Flash memory
- External source - SD Card

The BOOT_MODE pins determine the boot source.

NOTE

For compatibility to DART-MX8M and DART-MX8M-MINI pin J2.78 SAI1_TXD2 (BOOT_CONFIG [10]), is connected internally via buffer to BOOT_MODE0 of DART-MX8M-PLUS as boot source selection.

Table 67: BOOT_SEL signal SOM-DIMM 200 pin connector

PIN#	ASSY	ALT_NAME	ALT#	NOTES	BALL
J2.78		BOOT_MODE0	8	Connected internally to boot logic input. Drives BOOT_MODE0; Powered by NVCC_SAI1_SAI5; 1.8V at power up; Programmable 1.8V/3.3V; See section 8.21.1.1 As boot control with POR_B rise: High - External Boot (SD2) Low - Internal Boot (SD3 eMMC)	SOC.AH11
J2.11		BOOT_MODE1	0	PD in SOC; Requires 4.7K pull up on Carrier;	SOC.F8
J2.13		BOOT_MODE2	0	PD in SOC; Connected on DT8M & DT8MM boot mode0 pin; For compatibility to DT8M and DT8MM include 4.7K pull down on Carrier; If not required can float;	SOC.G8
J1.72		BOOT_MODE3	0	PD in SOC; Can be left floating if not used;	SOC.G12
J2.60		BOOT_MODE4	6	Not driven as part of boot configuration!	SOC.AH16
J2.14	No AC	BOOT_MODE5	6	Not driven as part of boot configuration! With “AC” configuration do not alter PINMUX function.	SOC.AH18

8.22.3 Boundary Scan

In order to enter Boundary Scan BOOT_MODE0, BOOT_MODE1, BOOT_MODE2, BOOT_MODE3, JTAG_MOD and POR_B must be pulled to "111111" for i.MX8M Plus to enter Boundary Scan mode.

9. Electrical Specifications

9.1 Absolute Maximum Ratings

Table 68: Absolute Maximum Ratings

Parameter	Min	Max	Unit
VBAT	-0.3	5.5	V
USB_VBUS	-0.3	5.25	V
NVCC_ENET [1]	-0.3	3.6	V

[1] Power input applicable only when “EC” not part of DART hardware configuration

9.2 Operating Conditions

Table 69: Operating Ranges

Parameter	Min.	Typ.	Max.	Unit
VBAT	3.5	3.7	5	V
USB_VBUS	4.75	5	5.25	V
NVCC_ENET [1]	1.8	1.8	3.3	V
NVCC_SAI1_SAI5 [2]	1.8		3.3	V
NVCC_SD2_1V8_3V3 [3]	1.8	3.3	3.3	V

[1] Power input applicable only when “EC” not part of DART hardware configuration
[2] Power output from DART as reference for SAI1 and SAI5 pads.
[3] Power output from DART as reference for SD2 pads.

9.3 NVCC_3V3 output power supply capabilities

Table 70: NVCC_3V3 Maximum Current

Parameter	NVCC_3V3 Maximum current	Units
VBAT < 3.7V	100	mA
VBAT > 3.7V	300	mA

9.4 Peripheral Voltage Levels

Most of the peripheral interface lines used as inputs or output to the DART-MX8M-PLUS uses 3.3V LVCMOS levels, except the following interfaces: SD2, ENET_QOS, SAI1, SAI5, HDMI, PCIe, USB, MIPI-DSI, MIPI-CSI, LVDS.

***PCIe/HDMI/USB/MIPI-DSI/MIPI-CSI/LVDS*:** Interfaces follow a different standard since they are high-speed signals.

uSDHC2: (SDIO lines) interface IOs will change voltage between 3.3V and 1.8V depending on the SD card capabilities.
With other alternative function user can determine the voltage uSDHC2 IOs bank will be 1.8V or 3.3V;

ENET_QOS: interface available in case SOM is ordered **without "EC"** configuration. IOs will run according to the power fed to NVCC_ENET pin.

SAI1/SAI5: IOs will run according to the power output on NVCC_SAI1_SAI5 pin. ENET1 RGMII/RMII pins are alternate function of SAI1 pins.

9.5 Power Consumption

Table 71: DART-MX8M-PLUS Power Consumption

Mode	Voltage [V]	Current [A]	Power [W]	Conditions
Run	3.826V	0.730A	2.79W	Linux up, Wi-Fi connected and Iperf is running 802.11 ac 5GHz (Dual Band Module)
Run	3.826V	0.650A	2.48W	Linux up, Wi-Fi connected and Iperf is running 802.11 n 2.4GHz (Dual Band Module)
Run	3.826V	0.625A	2.39W	Linux up, Wi-Fi connected and Iperf is running 802.11 n 2.4GHz (Single Band Module)
Run	3.826V	0.480A	1.83W	Linux up
FHD video playback	3.826V	0.630A	2.41W	On 800x400 LCD
Standby	3.826V	~7.9mA	~30.22mW	Memory retention mode (Measured after 3 min)
Off (RTC)	3.826V	0.21mA	0.8mW	All power rails are Off, only Internal SoC RTC is powered

NOTE

Setup:
HW:

Wi-Fi iperf test Single Band module –
DART-MX8MPQ_1800C_4096R_16G_AC_EC_WB_CT_REV1.1; CPU Rev A0
Other tests:
DART-MX8MPQ_1800C_4096R_16G_AC_EC_WBD_CT_REV1.1B; CPU Rev A1

SW: gatesgarth-fsl-5.10.9_1.0.0-mx8mp-v1.0

DISCLAIMER:
Power consumption measurements apply only to limited operation scenarios. Actual power consumption may vary depending on the interfacing peripherals and user application modes; Users must conduct testing per their specific operation scenarios.

Depending on the specific use cases and end product system design, an appropriate thermal solution should be applied.

10. Environmental Specifications

Table 72: Environmental Specifications

Parameter	Min	Max
Commercial Operating Temperature Range	0°C	70°C
Extended Operating Temperature Range	-25°C	85°C
Industrial Operating Temperature Range	-40°C	85°C
Prediction Method Model: Telcordia Technologies Special Report SR-332, Issue 4 50°C, GB	> 6183 Khrs	

NOTES

Industrial Temperature is based on the operating temperature grade of the DART components.

11. Mechanical

11.1 Carrier Board Mounting

The SOM has four mounting holes for mounting it to the carrier board which are plated holes and connected to GND.

NOTE

The size and footprint of SOM 90-pin connectors Hirose P/N: DF40C-90DP-0.4V(51) are different from mating carrier board 90-pin connectors (see section 7.1).

To ensure correct positioning of the carrier board connectors and holes please refer to VAR-DT8MCustomBoard DXF available here (under documentation tab):
http://www.variscite.com/products/single-board-computers/var-dt8mcustomboard

It is recommended NOT to place any components under the SOM.

11.2 Standoffs

Customers requiring a mechanical solution for mounting in harsh vibration environments can use the following standoff:

Manufacturer: **MAC8**

PN: **TH-1.6-1.5-M2**

Link: https://mac8usa.com/threaded-spacer.php

NOTE: The M2 screws head diameter must be smaller than 4mm.

11.3 SOM Dimensions

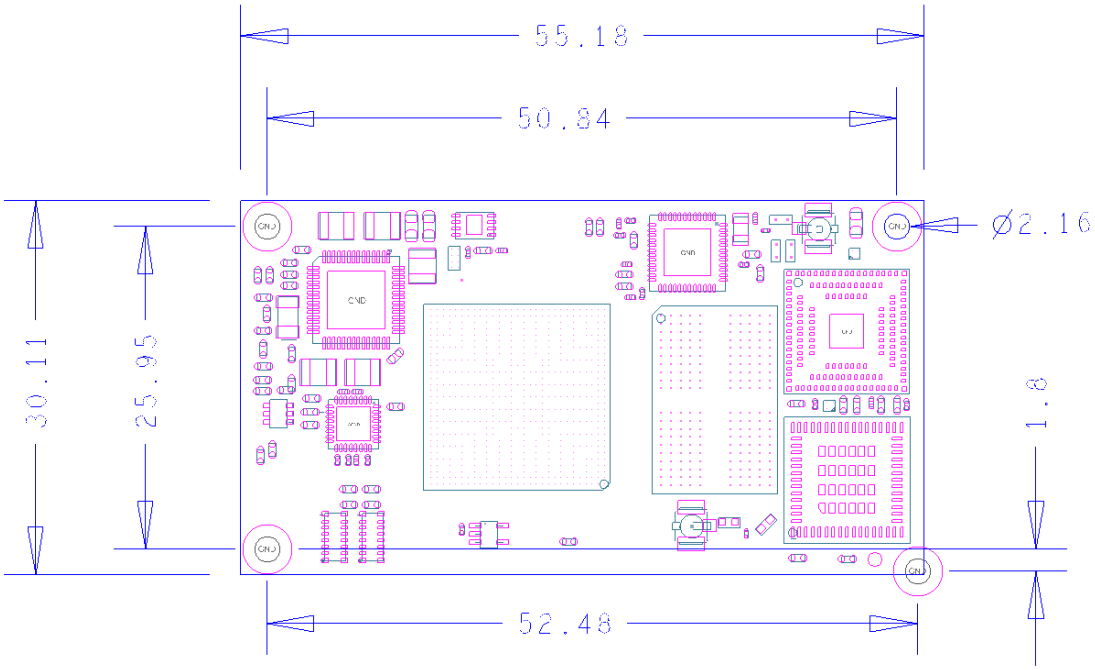


Figure 5: DART-MX8M-PLUS Mechanics in mm

Dimensioning:

Width: 55.18 mm

Length: 30.11 mm

Height: 5.13 mm (Carrier PCB to highest component on SOM)

11.3.1 CAD Files

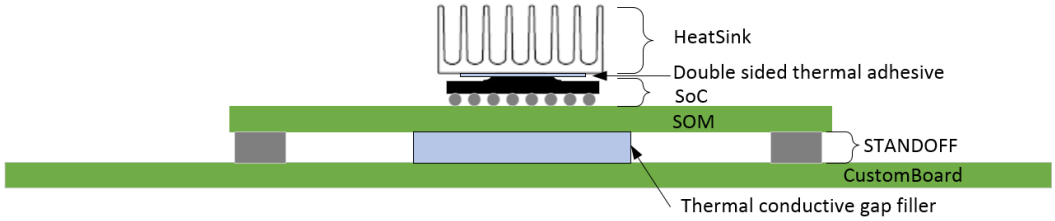
CAD files are available for download at http://www.variscite.com/

11.4 Thermal Management

Certain operation scenarios may prompt the use of an external heat dissipation solution.

The implemented solution design may vary depending on the device operation scenario as well as its mechanical design.

The following solution was implemented in the DART-MX8M evaluation kits.



Thermal conductive gap filler with similar performance to " TIF™700 Series Thermally Gap Filler "; appropriate thickness PN: TIF760P (1.5mm):

Link: http://www.ziitek.com/en/products/2/201403011972.html

The heat gap filler will allow a moderate heat generation on the SOM board to dissipate through the carrier board. In this case, it is recommended to have an exposed copper pad in the location of the thermal heat gap filler, on the top layer of the CustomBoard. The copper pad should follow thermal pad design rules.

Heat sink with an embedded double-sided adhesive with similar performance as ATS-55250W-C1-R0:

Link: https://www.qats.com/Product/Heat-Sinks/BGA-Heat-Sink---High-Performance/Cross-Cut-Tape-On/ATS-55250W-C1-R0/609.aspx

DISCLAIMER:
Thermal solution must be evaluated and depends on the application requirement.

12. Legal Notice

Variscite Ltd. ("Variscite") products and services are sold subject to Variscite terms and conditions of sale, delivery and payment supplied at the time of order acknowledgement.

Variscite warrants performance of its products to the specifications in effect at the date of shipment. Variscite reserves the right to make changes to its products and specifications or to discontinue any product or service without notice. Customers should therefore obtain the latest version of relevant product information from Variscite to verify that their reference is current.

Testing and other quality control techniques are utilized to the extent that Variscite deems necessary to support its warranty.

Specific testing of all parameters of each device is not necessarily performed unless required by law or regulation.

In order to minimize risks associated with customer applications, the customer must use adequate design and operating safeguards to minimize inherent or procedural hazards. Variscite is not liable for applications assistance or customer product design. The customer is solely responsible for its selection and use of Variscite products. Variscite is not liable for such selection or use or for use of any circuitry other than circuitry entirely embodied in a Variscite product.

Variscite products are not intended for use in life support systems, appliances, nuclear systems or systems where malfunction can reasonably be expected to result in personal injury, death or severe property or environmental damage. Any use of products by the customer for such purposes is at the customer's own risk.

Variscite does not grant any license (express or implied) under any patent right, copyright, mask work right or other intellectual property right of Variscite covering or relating to any combination, machine, or process in which its products or services might be or are used. Any provision or publication of any third party's products or services does not constitute Variscite's approval, license, warranty or endorsement thereof. Any third-party trademarks contained in this document belong to the respective third-party owner.

Reproduction of information from Variscite datasheets is permissible only if reproduction is without alteration and is accompanied by all associated copyright, proprietary and other notices (including this notice) and conditions. Variscite is not liable for any un-authorized alteration of such information or for any reliance placed thereon.

Any representations made, warranties given, and/or liabilities accepted by any person which differ from those contained in this datasheet or in Variscite's standard terms and conditions of sale, delivery and payment are made, given and/or accepted at that person's own risk. Variscite is not liable for any such representations, warranties or liabilities or for any reliance placed thereon by any person.

13. Warranty Terms

Variscite guarantees hardware products against defects in workmanship and material for a period of one (1) year from the date of shipment. Your sole remedy and Variscite's sole liability shall be for Variscite, at its sole discretion, to either repair or replace the defective hardware product at no charge or to refund the purchase price. Shipment costs in both directions are the responsibility of the customer. This warranty is void if the hardware product has been altered or damaged by accident, misuse or abuse.

Disclaimer of Warranty

THIS WARRANTY IS MADE IN LIEU OF ANY OTHER WARRANTY, WHETHER EXPRESSED, OR IMPLIED, OF MERCHANTABILITY, FITNESS FOR A SPECIFIC PURPOSE, NON-INFRINGEMENT OR THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION, EXCEPT THE WARRANTY EXPRESSLY STATED HEREIN. THE REMEDIES SET FORTH HEREIN SHALL BE THE SOLE AND EXCLUSIVE REMEDIES OF ANY PURCHASER WITH RESPECT TO ANY DEFECTIVE PRODUCT.

Limitation on Liability

UNDER NO CIRCUMSTANCES SHALL VARISCITE BE LIABLE FOR ANY LOSS, DAMAGE OR EXPENSE SUFFERED OR INCURRED WITH RESPECT TO ANY DEFECTIVE PRODUCT. IN NO EVENT SHALL VARISCITE BE LIABLE FOR ANY INCIDENTAL OR CONSEQUENTIAL DAMAGES THAT YOU MAY SUFFER DIRECTLY OR INDIRECTLY FROM USE OF ANY PRODUCT. BY ORDERING THE SOM, THE CUSTOMER APPROVES THAT THE VARISCITE SOM, HARDWARE AND SOFTWARE, WAS THOROUGHLY TESTED AND HAS MET THE CUSTOMER'S REQUIREMETS AND SPECIFICATIONS.

14. Contact Information

Headquarters:
Variscite Ltd.

9, Hamelacha Street
Lod
P.O.B 1121
Airport City, 70100
ISRAEL

Tel: +972 (9) 9562910
Fax: +972 (9) 9589477

Sales: sales@variscite.com

Technical Support: support@variscite.com

Corporate Website: www.variscite.com