Data Hazards in Pipe line Structure

Data hazard means operand conflicts When we exercise instructions.

in pipe line what we do! we parallely execute the instructions.

But as if first instructions is having few operands and second instructions is having few operands and as if operands dependency is there Till you dan't have answer on where and anot well your connot well your connot well then we can say there is data

Iz: ADD RY, (R), R5

Considering & Stage pipe line.

I I I I EX M WN ROUMER,

IF ID EX M WN

IF (ID) EX M WN Rewin

output of first instructions is input to 2nd Instructions

Result is depending in frevious mustructions

By operant forwarding we can

Resolve that

Resolve that

Resolve that

Resolve that

Resolve to Resolve of Ri 4 parent Large

TI TEDID EXD (WB) -> Resolve of Ri 4 parent Large

TI TEDID EX M WB

TI TEDID EX M WB

Ru

Correct rough after forwarding.

in operand forwarding there will be to butter Registers in between the stages.

Execute is having result but it is updated the value at R, at WB stage.

The bubble register will be holding the value ab Rescuet.

In examination they can give statement like

Here we are using operand forwarding.

Mean by defaut there is no data hazard.

but if it is not given we have to consider

data hazard.

if data hazard is happening and operand forwarding is not given in that case we can not execute is not given in that case we will have to delay ID stage at and cloth. We will have to start execution by this cycles and we have to start execution from 6th chock cycles. So if we start execution from 6th cycle means we have to start preceding stages.

Data Dependency is Ray
Data Dependency is RAW dependency RAW -> Read after write
in true dependency we will reading after
ADP (R), R2, R3
ADD Ry, (R), R6 Readin
ADD RI, Rz, RZ
ADD RY, RI, RE
How to calculate no of RAW dependency.
710 (NE) 1002 PF > \$ \$
war write after Read (Anti dependency)
ADD RI, Rz, RS
ADD Re, RI, R3 OIP IIO
IO(13+) 1 0.0 (NI § # 4
WAW - write afker write (output dependency)
APP (R), R2, R7
A1212 (RT) RY, R5
00 \$ 12+ \$ TO.0 \$NT 8 + \$

WAW output detendency.