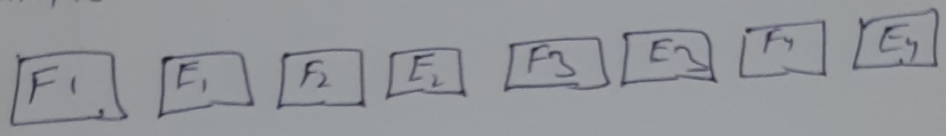
Pipelining in computer organisation & Architecture

→ Pipeline defines the overlapping stage for instruction execution.

→ Pipeline is done to improve execution speed of programs.

Example

8085:- 

instruction Execution

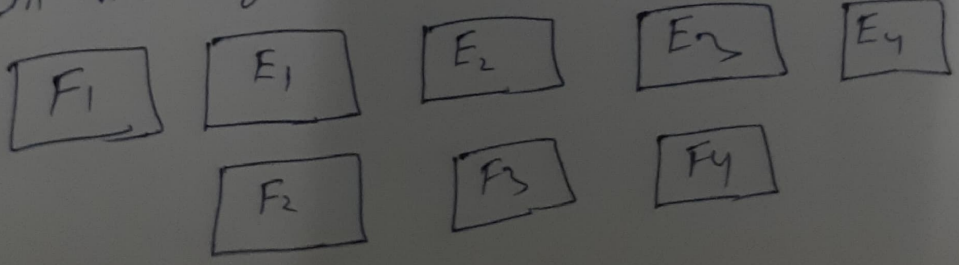
In pipelining instruction of execution bisected into stages. and performed in parallel.

8086 same instruction is done with 2 stage Pipelining

in 8086 2 stage pipelining

Execution is happening in parallel.

First it is fetching first instruction and in second cycle when it is executing First instruction in parallel with that it is feteching 2nd instruction in next cycle.



Execution speed is increasing almost 2 times in 2 stage pipe line as compare to without pipeline.

In CPU more was feted after feted there were decoding it and after that executing it.

When feted is ~~fetching~~ completed and decode is happening

at that time unit of feter is free.

and when decoded instruction i.e getting executed at that time decode as well as feted units are free.

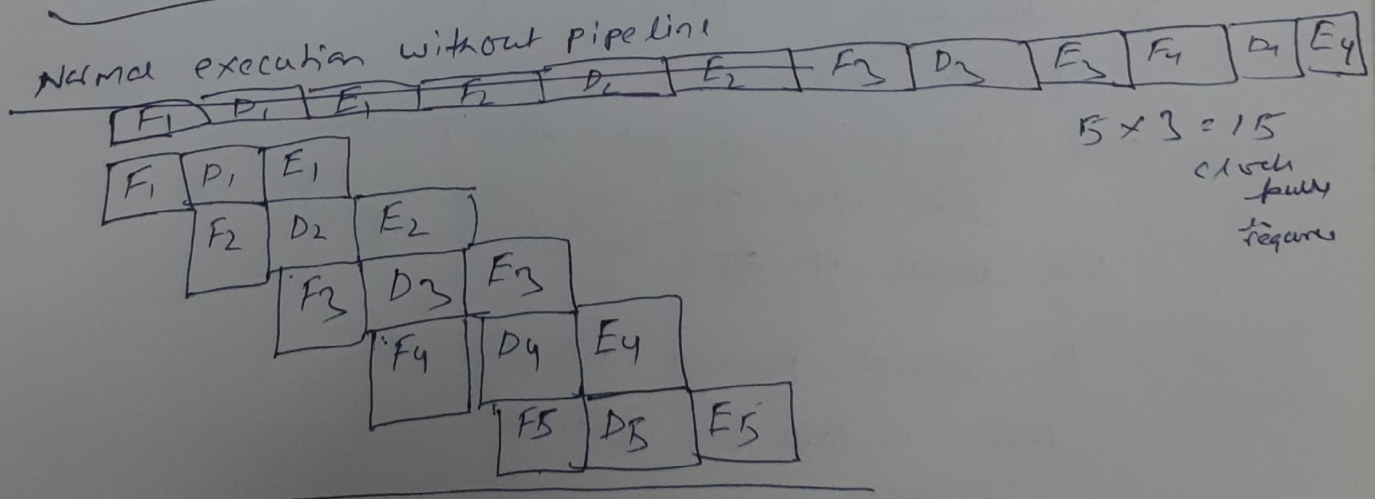
instead of having more unit free they make there unit active

in pipelining all the states are busy while executing the instruction

i.e Refer as parallel execution of instruction.

There are various computer which are available with various stages of pipelining.

In ARM7 TDMI There is 3 stages pipelining.



all unit of CPU is kept to busy.

Because of parallel processing entire speed is boosted.

in pipeling all the units are busy.

Parameters of Pipelining in execution of Program. (Problems)

Consider 5 stage pipe lining, 8 instruction executed along with 5 stage pipe line.

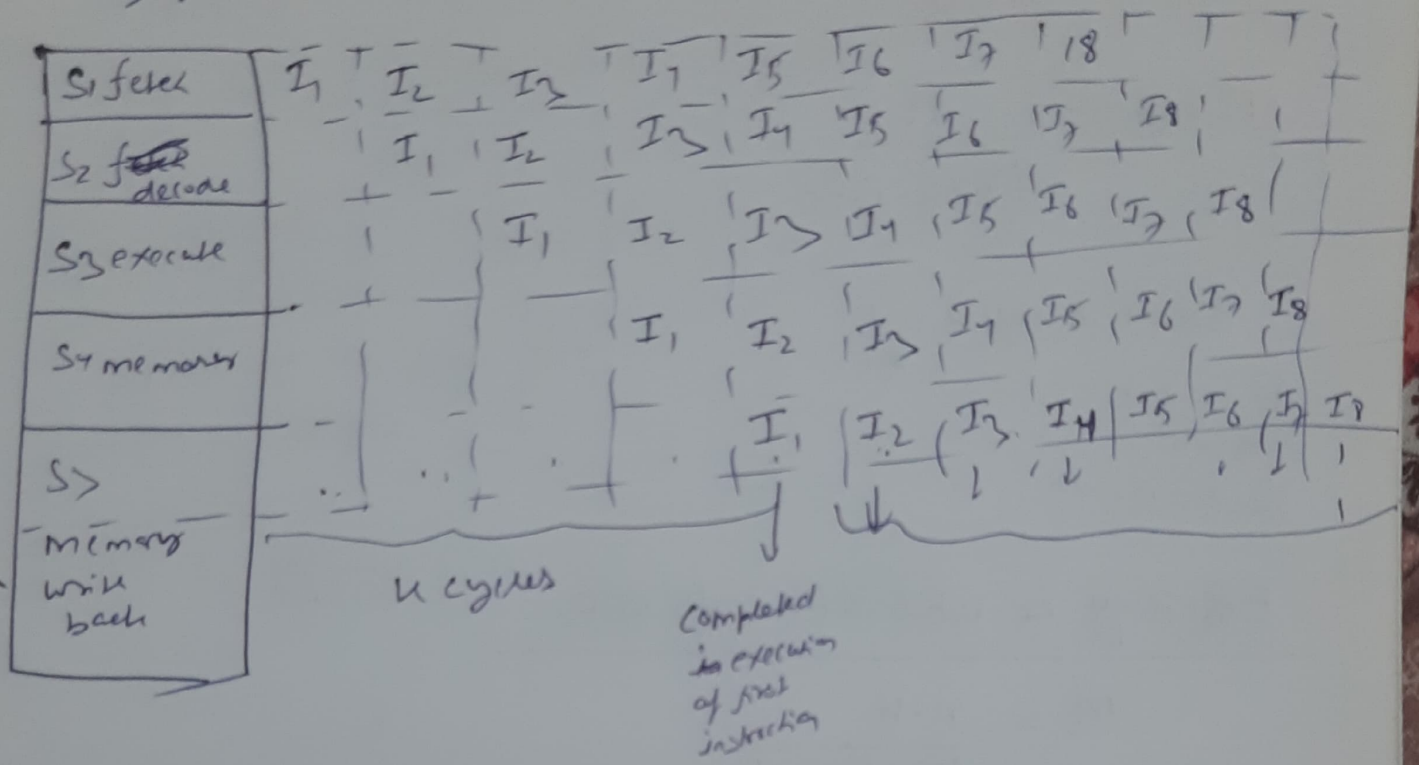
let us assume ARM9 architecture for 5 stage pipeline.

→ Fetch (IF)
→ Decode (ID)
→ execute (instruction)
→ memory (write)
→ write back (Register write)

Lets have 8 Instructions execution from I1 to I8

Instruction space timing diagram with pipeline.

stages = k



one stage cycle time period is tc

without pipeline

$\rightarrow T_{wp} = \underline{nk\,tc}$

with pipe line

~~1st k cycle~~

first instruction will take ~~k~~ k cycle

for (n-1) inst no of cycle = (n-1)

$T_p = (k + n - 1) = (n + k - 1)\,tc$

$\text{Speedup} = \frac{T_{wp}}{T_p} = \frac{nk\,tc}{(n+k-1)\,tc} = \frac{nk}{(n+k-1)}$

Throughput: How many instruction i.e getting executed with respect to time

$$\text{Throughput} = \frac{n}{(n+k-1)tc}$$

$$\text{Ideal throughput} = \frac{1}{tc}$$

if n not given ideal = n = ∞

Efficiency or utilisation of CPU

$$\eta = \frac{n \cdot k}{(n+k-1) \times k}$$

Total no of block and utilised block ratio

$$\eta = \frac{(n \cdot k)}{(k+n-1) \times k} \quad \text{— utilised}$$

→ Speedup

$$S = k\eta$$

Gate PS

Consider 5 stage pipeline with cycle time of 5 ns. Calculate the execution time of 100 instructions and speed up due to pipeline. Also find utilisation

→ $k = 5$

$tc = 5ns$

$n = 100$

$T_p = (n+k-1)tc = (100+5-1) \times 5 = 620 ns$