Structural Hazards in pipe line

Let us take 4 different stages of pipeline

(1.) Instruction fetch (IF)

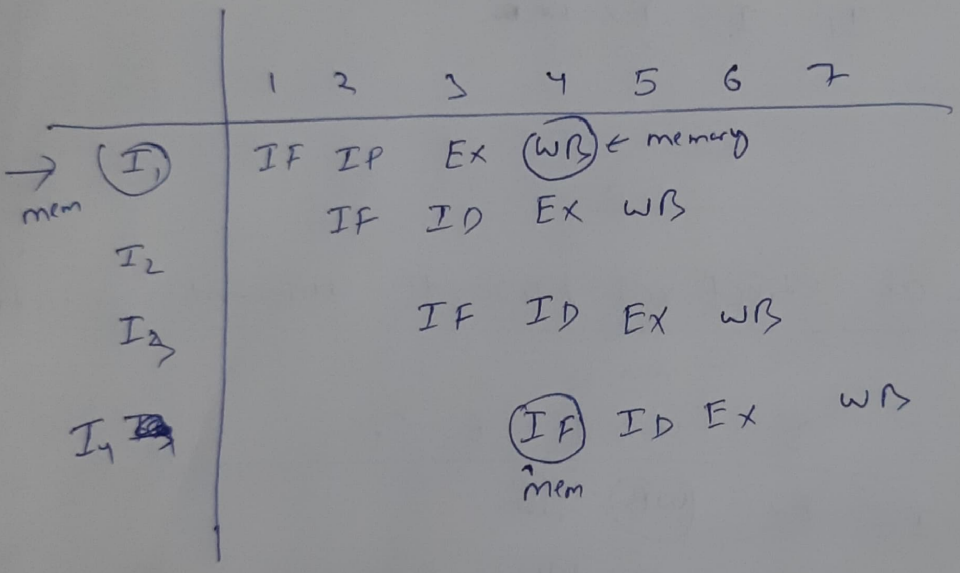
(2.) Instruction decode + operand decode

(3.) Execute instruction

(4.) write back.

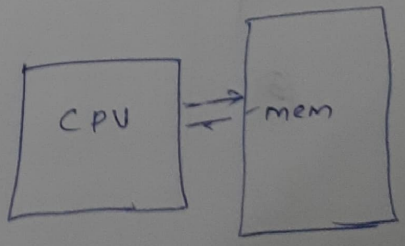
Example of structural hazards

Let no hazards



Let I_1 is memory instruction

We can see both I_1 and I_4 using memory at 4th cycle. It can not execute this instruction by this time period. because both instruction needs memory.



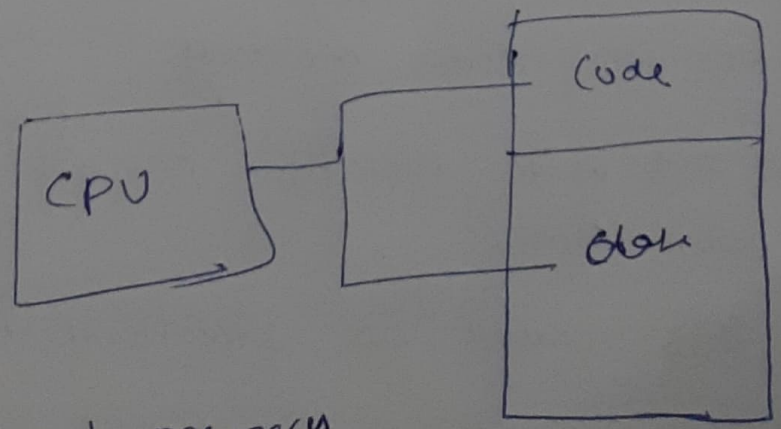
Read and write operation can not happens at same time.

So this called as structural hazards.

Structural hazards means same resources can not utilize by different instructions at same time.

Solution of Structural hazards Harvard architecture

	1	2	3	4	5	6	7
mem → I_1	I_F	I_D	Ex	WB – mem data			
I_2		I_F	I_D	Ex	WB		
I_3			I_F	I_D	Ex	WB	
I_4				I_F mem code	I_D	Ex	WB



we are having different memory

means at same time data write and instruction fetch (read) is possible.

It is not structural hazard with memory only.
There can be other structural hazards as well.

If we have instruction which is having multiple cycles for execution then we will be observing in pipeline there can be an issue.

Example

		1	2	3	4	5	6	7	8
(MUL)	I_1	IF	ID	Ex	Ex	Ex	WB		
(ADD)	I_2		IF	ID	—	—	Ex	WB	

2 clock cycles are stalled because we have only one ALU
Solution is multiple ALU

let first instruction regarding multiplication
2nd " " addition.

Generally when structural hazards come at that time some time we can resolve some problems by having compiler as well as by having Harvard structure.
But when it comes to complex instruction at a time definately there will be issue of Structural Hazards