Gate CS

Consider a pipeline having 5 stages with duration 10ns, 30ns, 45ns, 80ns, 35ns if buffer delay is 20ns, calculate the Speed up of the pipe line processor

$$S = \frac{T_{WP}}{T_P} = \frac{[10+30+45+80+35]}{[80+20]}$$

we have to identify maximum delay of stage.

$$= \frac{200}{100} = 2$$

without pipe line does not need buffer. but with pipe line there is need of buffer

(2) Gate CS.

Assume we have two pipeline P_1 and P_2 respectively. P_1 has 6 stages each having execution time of 12ns, 14ns, 19ns, 20ns, 22ns, 25ns. P_2 has 4 stages each having execution time of 10ns. calculate the time that can be saved while using P_2 pipeline over P_1 pipe line, if 2000 instructions are executed.

→ P_1, $K = 6$, $t_{c_1} = 25ns$

→ P_2, $K = 4$, $t_{c_2} = 10nsec$

We have to calculate difference of execution time.

$n = 2000$

execution

$\Rightarrow T_{P_1} = (n+k-1)t_c$

$= (2000+5-1) \times 25$

$= 50125$ ns.

$T_{P_2} = (n+k_2-1)t_{c_2}$

$= (2000+4-1) 10 = 20050$

$\Delta T = 50125 - 20050$

$= 30075$ ns.

if you execute same program with processor P_2 you will be saving 30075 ns.

Q) Qn:-

Assume a pipeline P which operates at 3 GHz clock rate. It has speed up factor of 10 and efficiency of 40%. calculate no of stages in the above pipe line.

$\rightarrow$ $f_{clock} = 3$ GHz

$S = 10$

$\eta = 40\% = 0.4$

The basic relation between no of stages and efficiency

$S = k\eta$

$k = \frac{10}{0.4} = 25$

Examples on Pipelining Hazards in COA

GATE 2018 CS – The Instruction pipeline of a RISC processor has the following stages: Instruction (IF), Instruction Decode (ID), Operand Fetch (OF), Perform Operation (PO) and Writeback (WB). The IF, ID, OF and WB stages take 1 clock cycle each for every instruction. Consider a sequence of 100 instructions. In the PO stage, 40 instructions take 3 clock cycles each, 35 instructions take 2 clock cycles each and the remaining 25 instructions take 1 clock cycle each. Assume that there are no data hazards and no control hazards. The number of clock cycles required for completion of execution of the sequence of instruction is .....219.....

→ No of Cycles = Normal pipeline Cycles + Cycles due to Structural Hazard

$= (n+k-1) + 35 \times 1 + 40 \times 2$

$= (100+5-1) + 35 + 80$

Examples on Pipelining in COA

- **GATE 2009 CS** – Consider an instruction pipeline with five stages without any branch prediction: Fetch Instruction (FI), Decode Instruction (DI), Fetch Operand (FO), Execute Instruction (EI) and Write Operand (WO). The stage delay for FI, DI, FO, EI and WO are 5ns, 7ns, 10ns, 8ns and 6ns, respectively. There are intermediate storage buffer after each stage and the delay of each buffer is 1ns. A program consisting of 12 instructions I1, I2, I3, … , I12 is executed in this pipelined processor. Instruction I4 is only the branch instruction and its branch target is I9. If the branch is taken during the execution of this program, the time needed to complete the program is?

- $I_1, I_2, I_3, I_4, I_9, I_{10}, I_{11}, I_{12}$

  $n = 8$

- FI, DI, FO, EI, WO

  ↑

  4th Stage.

- No of stalled cycles = 4 − 1 = 3

- $T_p = t_p + t_s$

  $= (n + k - 1)\, t_c + x\, t_c$

  $= (8 + 5 - 1)\, 11 + 3 \times 11$

  $= 15 \times 11$

  $= 165$ nsec