Mirrored Diode ESD Protection Design Project

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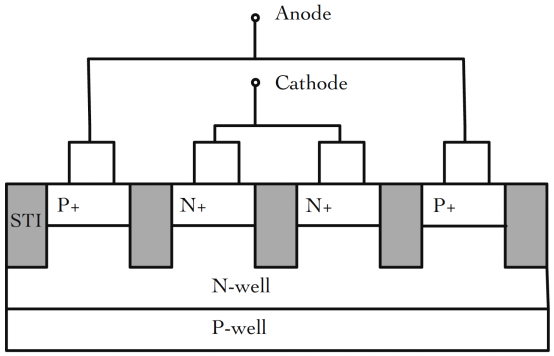
Introduction

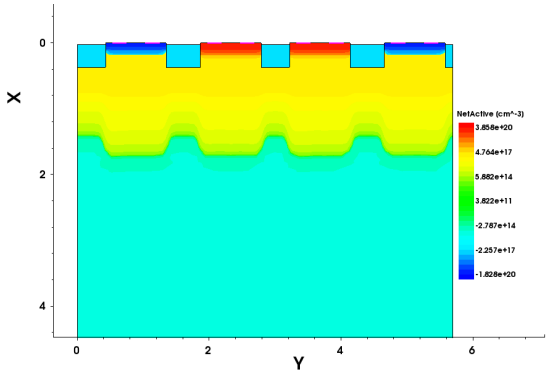
For this project, we wanted to modify the base of the diode that was given to us in Lab 2, in order to see how those modifications affect the performance. The goal of the changes was to make an ESD protection device that works based on the parameters of the labs from class, and then improving that model as much as we can. The main parameter that we are looking for in the new device is a decrease in the maximum temperature that it reaches.

Design Process

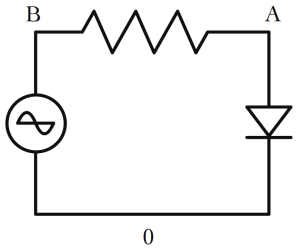
The first device that we are proposing is doubling and flipping the p and n active regions. We are hoping that by adding more regions to the device, the maximum temperature will be lower for the same width, taking into account the increased size of the device. This would improve the ESD performance of the device by decreasing the occurrence of gate blowout and other ESD failure mechanisms due to the current crowding at the corner of the n-plus diffusion. The structure of the proposed device is shown in the schematic below.



The reason that we chose this layout was because in lecture we were shown a series of diodes where the pn-junctions were alternating. We wanted to create a version that was symmetrical instead, and see how it compared to the diode from the previous lab. The closest device we found to the one we created was a diode-connected BJT, only ours as an STI region connecting the center. After modifying the file containing the structure of the diode, the layout was as follows:

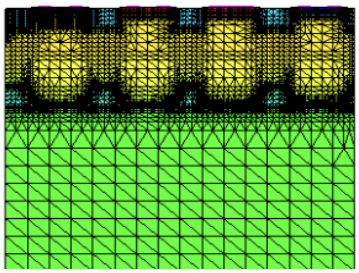


The change in layout structure required us to alter the HBM simulation file so that the active regions were connected to each other. This was done by adding more electrical connection points. The device being larger required that the boundaries in the file that created the mesh had to be adjusted as well. We doubled the values for all the maximum boundaries so that the mesh covered the full width. We are using the same simulation model as in Lab 2, so the circuit is connected like the figure below.

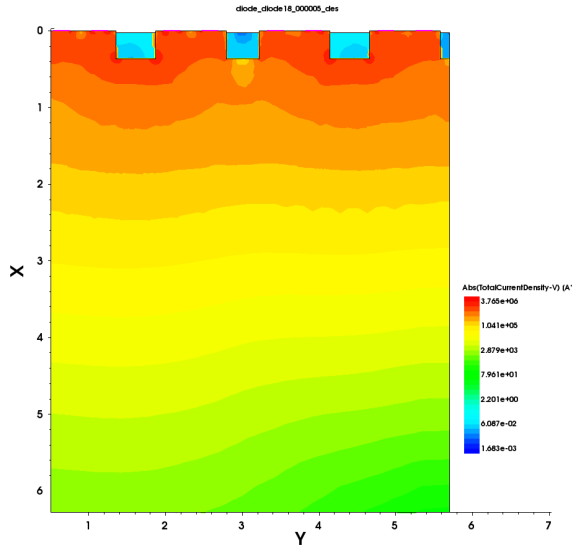


Results

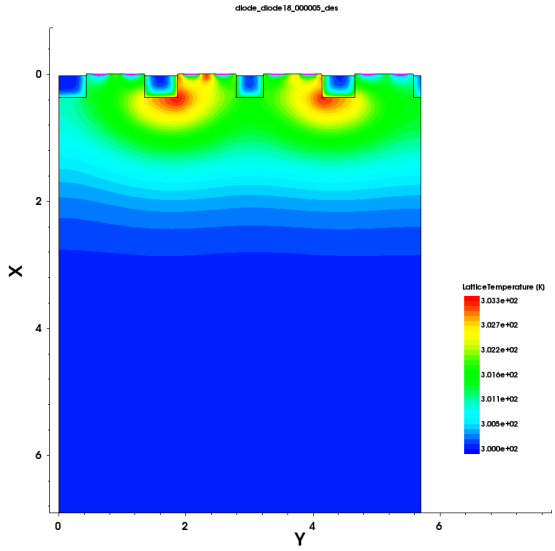
The device was able to run in the simulation, and we were able to build the mesh.



After we ensured that the simulation was running correctly and completed as expected, we wanted to look at the properties that the device was displaying, and compare them with the diode from Lab 2. This allows us to make sure we are on the right track with our design. Our device was simulated on 2kV HBM on 10 ns. Below we can see the results for the current density.



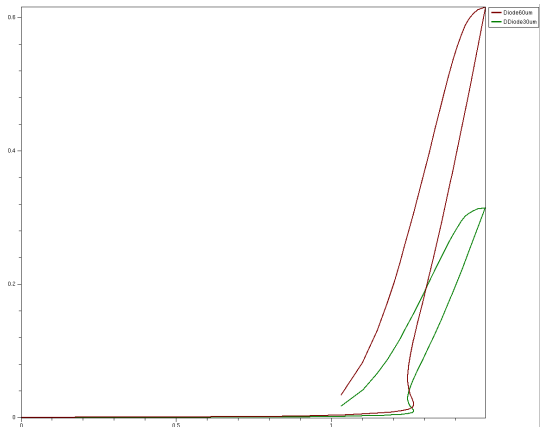
The current density values look similar to the ones in Lab 2, with the exception of the center, which has an area of low current density below the middle STI region. Other than that the intensity of the gradient downwards is very similar to the other diode. This means that while comparable, the extra active regions have affected the concentration in the middle somewhat. The other important value we wanted to look at was the lattice temperature, which is shown in the next figure.



Comparing the TCAD simulation lattice temperatures, the hotspots were still located at the lower corner of the STI regions closest to the n-plus diffusions. This new design introduced one small area of high temperature near the contacts of the left n-plus diffusion. Our diode did not overheat in this simulation, but the extra hotspot may be an issue when current density increases. The hotter temperatures seem to go further down the device, which could be a result of a more evenly distributed heat distribution in the rest of the device.

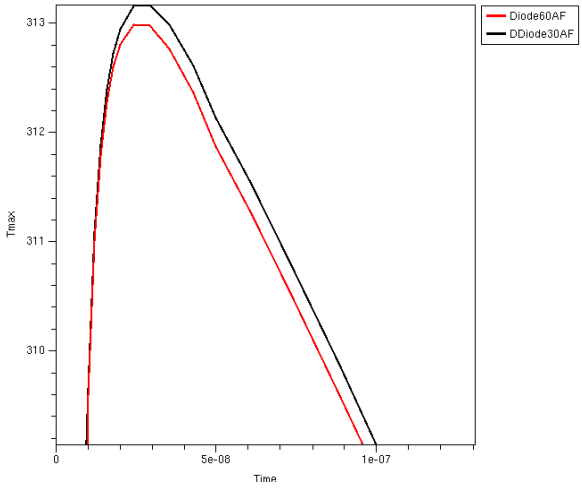
I. Diode 60AF and DDiode 30AF TCAD Simulation

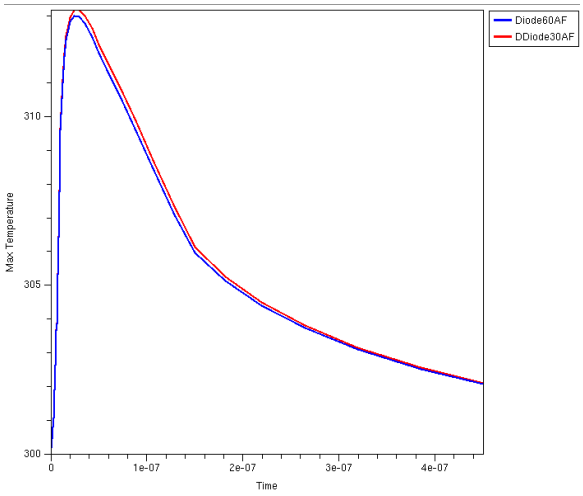
To compare the performance of the device, simulation results for the I-V curve and the maximum temperature were plotted on Sentaurus inspect. The parameters used are the I-V curve at the left pplus contact and the maximum temperature vs time across the entire device. In order to account for the increased width of the device, the area factor (AF) parameter in the hbm.cmd file was modified to half that of the regular p-plus n-well diode used in Lab 2. The following figure shows the I-V curve for the pplus1 contact for the 60 AF original diode and the 30 AF mirrored diode design.



The results shown in the figure above demonstrate the effect of the alternate design in reducing the absolute current load across the contacts. This is to be expected as there are additional contacts on the added pplus region that the current can be distributed across, cutting the value of the current seen by each of the contacts for the mirrored diode by approximately half. The trigger voltages remained identical across the two devices.

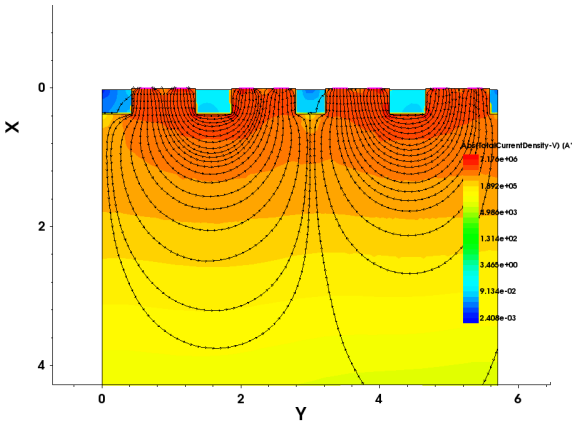
For a general view of the thermal comparison of our ESD protection device we used a simple plot of Tmax vs time, using definitions provided in the lab files.

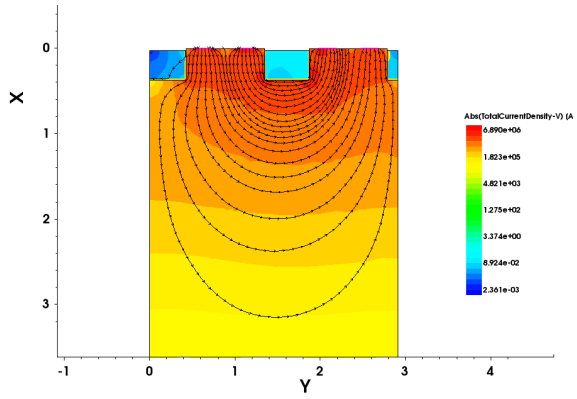




These graphs show the maximum temperature across the entire device for the duration of the simulation in both the original and mirrored diode. The plot shows an increase of 0.17K for the mirrored diode device. An enlarged view of the graph shows the temperature curve being larger than the standard diode at approximately the same width. This was a very slight relative increase which likely stems from the STI dimensions not being completely mirrored. In fact, the rightmost STI region was kept at the same dimension, y1-y2=0.1, as the p-plus n-well diode.

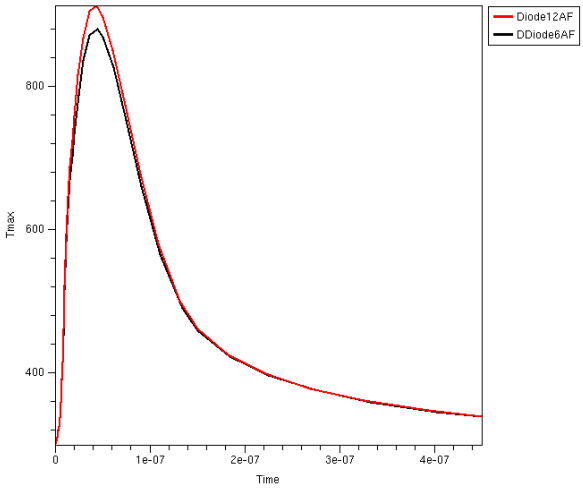
The following figures demonstrate the parity in current density across the two devices. The left part of the device, consisting of a one-to-one copy of the p-plus n-well diode layout, shows the same current density and streamlines. The difference occurs at the right half where the current travels deeper into the n-well. The layouts for both devices could be built with adjusted STI dimensions to increase the similarity for the purpose of simulation and comparison.



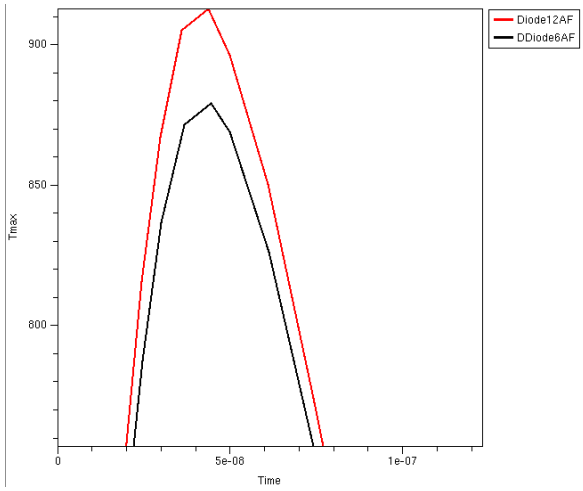


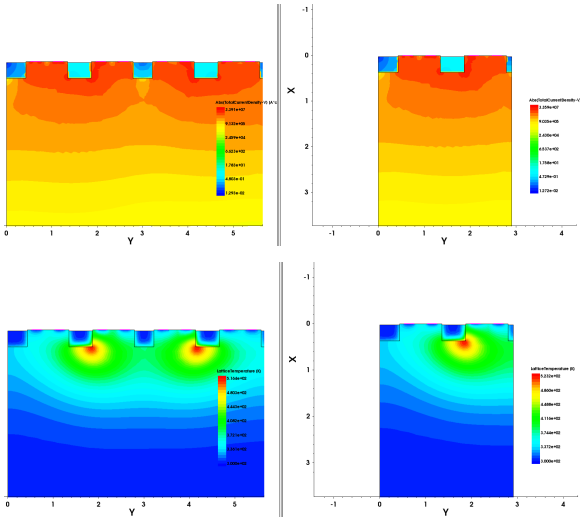
II. Minimum width Diode 12AF and DDiode 6AF TCAD Simulation

In order to further compare the temperature differences in the diodes, we plotted the results for the two devices at their respective minimum width passing 2kV HBM, 12 AF for the regular diode and 6 AF for the mirrored diode.



The figure above shows an enlarged view of the temperature curve for the new simulated widths. These results show a flipped outcome of the results acquired from the previous simulation. In the zoomed in view of the graph below, we can see that unlike the previous simulation, at minimum width the new design saw an improvement of 17K in the temperature peak over the equivalently sized regular diode. This could mean that the extra spot of high heat is actually helping slightly in this simulation, as it may act as an outlet for the excess heat.





Setbacks

There were some minor obstacles that we faced when doing the project, most of them stemming from our understanding of the code itself. When changing the layout of the device, we increased the width of the n-well. This meant the first time we tried to build the mesh, half of the device was not covered by the global reference box. After changing all of the dimensions in all the files that we were testing with, though, the device ran as expected. Another issue was with the area factor variable. Because we changed the width of the device dramatically, it was difficult to tell which area factors were comparable between our device and Lab 2. The first time we compared the current and temperature, we realized that a huge contributing factor was the size of the device. This led us to find what we believed were comparable area factors and analyze that way.

Conclusion

Overall, we were able to create a device that not only ran with the HBM 2kV model, but that saw slight improvements to the default diode that was given to us in Lab 2 at the minimum width. The results were as we expected based on the examples of mirrored devices that we analyzed in class. In the future, it would be interesting to see how the diodes we created fare in different types of tests. We could also compare it to more complex devices in order to see exactly how other changes affect the performance of ESD protection devices.