ECE2411: Logic Circuit II, Spring 2018

Lab2. Model, simulate and test a combinational logic circuit.

Objective: Improve the Verilog modeling, simulation and testbench writing skills. Design a 4 to 16 decoder using basic gates by drawing the schematic diagram. Then write a Verilog model that describe your 4 to 16 decoder design. Then write a Verilog testbench to test the decoder with all combinations of inputs, and check the decoder outputs. Simulate the decoder model using your testbench with ModelSim to verify your design.

1. Design a 4 to 16 decoder by drawing its schematic diagram using basic logic gates.
2. Write a Verilog model for the 4 to 16 decoder either by simply describing your basic logic gates design or by modeling the decoder functionality at higher abstraction level.
3. Create a testbench for the 4 to 16 decoder model.
4. Simulate the 4 to 16 model using the testbench to verify its functionality.
5. Capture the simulation results as waveform for your report.
6. Analyze the results and state if the model were fully verified and explain why so.
7. Comparing the two design processes employed for this lab, the schematic/circuit diagram approach and the Verilog modeling approach. Stating their advantages and disadvantages based on your experiences, and what was learned.
8. (Optional) Challenging yourself if you have time by writing another decoder model using the approach that you decided not to use in step 2. Then adding an instantiation of the second model in your testbench, so that both models can be simulated simultaneously. This is an optional step for this Lab.