

## ECE2411: Logic Circuit II, Spring 2018

### Lab3. Design and simulate an 8 bit adder

Objective: Being proficient with ModelSim in simulating Verilog models using testbench. Developing Verilog modeling, testbench writing and simulation skills further.

Design an 8 bit adder by writing a gate level ripple carry Verilog model. Then write a testbench for the adder model you wrote.

Simulate your adder model in ModelSim with the testbench. And demonstrate the adder model is operating correctly in following cases of addition operations:  $100+99$ ,  $22+33$ ,  $0+200$  and  $178+134$ , all numbers listed here are decimal numbers. Presenting your simulation results as waveforms in your report.

Analyze your simulation results and discuss any observations or issues during running the lab.

Make a statement to state what are the minimum operations needed in the testbench to verify the adder model fully.