ECE2411: Logic Circuit II, Spring 2017

Lab4. Design a FSM with Verilog

Objective: Learn to write a FSM model and simulate it in ModelSim.

A state machine can be designed using flip-lops. The state diagram for such a circuit is shown below. Write a behavioral model of the FSM described by the state diagram. Set the initial state to 001 state, and set the initial output to 0.

Write a testbench to stimulate the state machine. Simulate the model you have written in ModelSim with the testbench using following cases.

1) Given an input x as 011110011, (i.e. x is 0 at time 0 then it becomes a 1 next), simulate the state machine and report your results as output waveform, where inputs, the states and outputs are all shown.

2) Rerun the simulation using the same input sequence. This time assume an initial state of 010 instead of 001. Generate the output waveform in the same format as previously, and state what was done that initialized the state machine to start with a state of 010.

3) Based the discussion on your experiences how the FSM verification is different from that of a combinational logic.