ECE2411: Logic Circuit II, Spring 2018

Lab5. Design and simulate a BCD counter

Objective: Learn to write Verilog model with simple but specific requirements. Model a BCD (the binary-coded decimal, 8421 code) counter, the counting range is from 0 to 99 decimal. The counter has an asynchronous reset that set the output to all zeros. The counter is also capable of loading a number and then continue count from the loaded number.

The BCD counting sequence for one decimal digit is listed below. The model can either be a ripple counter or a synchronous counter, and at the abstract level of your choice.

Write a testbench for your BCD counter, and use it to simulate the model written in ModelSim. Make sure the scenario that your BCD counter counts over 99 is tested. Record the observed counter behavior and discuss if that is what you intended. Also a scenario while the counter is counting, the number 51 is loaded, and counting continued after the loading. This is to verify the loading function of your counter model.